NNT1 DIE
N-Channel JFET Pair

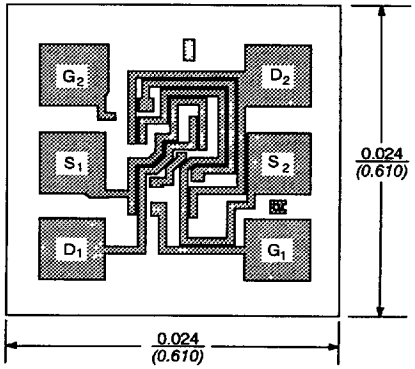
Siliconix incorporated

T-31-27

The NNT die is a monolithic pairs of n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250fA, high gain at low operating currents, and tight matching. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NNT1CHP*
U423
*Meets or exceeds specification for all part numbers listed below

For additional design information please consult the typical performance curves.



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Ultra-Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

FEATURES

- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate-Gate Voltage	V_{GG}	±40	
Gate Current	I_G	10	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

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SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1\ \mu A$, $V_{DS} = 0\ V$		-60	-40		V
Gate-Gate Breakdown Voltage	V_{GG}	$I_G = -1\ \mu A$, $I_D = 0$ nA, $I_S = 0$		±55	±40		
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = 10\ V$, $I_D = 1$ nA		-1.2	-0.4	-2	
Saturation Drain Current[c]	I_{DSS}	$V_{DS} = 10\ V$, $V_{GS} = 0\ V$		400	60	1000	µA
Gate Reverse Current	I_{GSS}	$V_{GS} = -20\ V$, $V_{DS} = 0\ V$		-0.6			pA
			$T_A = 125°C$	-0.3			nA
Gate Operating Current	I_G	$V_{DG} = 10\ V$, $I_D = 30\ \mu A$		-0.2			pA
			$T_A = 125°C$	-150			
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 0\ V$, $I_D = 10\ \mu A$		2000			Ω
Gate-Source Voltage	V_{GS}	$V_{DG} = 10\ V$, $I_D = 30\ \mu A$		-0.8			V
Gate-Source Forward Voltage	$V_{GS(F)}$	$V_{DS} = 0\ V$, $I_G = 1$ mA		0.7			
DYNAMIC							
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10\ V$, $V_{GS} = 0\ V$, f = 1 kHz		0.6			mS
Common-Source Output Conductance	g_{os}			4			µS
Common-Source Forward Transconductance	g_{fs}	$V_{DG} = 10\ V$, $I_D = 30\ \mu A$, f = 1 kHz		0.2			mS
Common-Source Output Conductance	g_{os}			0.4			µS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10\ V$, $V_{GS} = 0\ V$, f = 1 MHz		1.4			pF
Common-Source Reverse Transfer Capacitance	C_{rss}			0.7			
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DG} = 10\ V$, $I_D = 30\ \mu A$, f = 10 Hz		30			$nV/\sqrt{Hz}$
MATCHING							
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	$I_D = 30\ \mu A$, $V_{DG} = 10\ V$		14		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	$I_D = 30\ \mu A$, $V_{DG} = 10\ V$	T = -55 to 25°C	25			µV/°C
			T = 25 to 125°C	25			
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10$ to 20 V, $I_D = 30\ \mu A$		102			dB

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

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