# NNZ1 DIE
# N-Channel JFET Pair

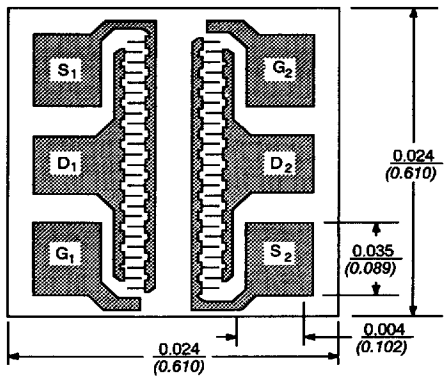
Siliconix incorporated

T-31-27

The NNZ1 Die is a monolithic pair of JFETs. The die features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

| NNZ1CHP* |
|---|
| SST440<br>SST441 |
| *Meets or exceeds specification for all part numbers listed below |

For additional design information please consult the typical performance curves NNZ.




Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

## DESIGNED FOR:

- High-Frequency Amplifiers
- Mixers
- Oscillators
- Hybrid Op Amps

## FEATURES

- High Gain
- Low Input Capacitance

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C Unless Otherwise Noted)

| PARAMETERS/TEST CONDITIONS | SYMBOL | LIMITS | UNITS |
|---|---|---|---|
| Gate-Drain Voltage | $V_{GD}$ | -25 | V |
| Gate-Source Voltage | $V_{GS}$ | -25 | |
| Gate Current | $I_G$ | 50 | mA |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | -55 to 150 | °C |

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# NNZ1 DIE

| SPECIFICATIONS[a] | | | LIMITS | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | TYP[b] | MIN | MAX | UNIT |
| **STATIC** | | | | | | |
| Gate-Source Breakdown Voltage | $V_{(BR)GSS}$ | $I_G$ = -1 µA, $V_{DS}$ = 0 V | -35 | -25 | | V |
| Gate-Source Cutoff Voltage | $V_{GS(OFF)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 nA | -3.5 | -1 | -5 | |
| Saturation Drain Current[c] | $I_{DSS}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V | 15 | 7 | 30 | mA |
| Gate Reverse Current | $I_{GSS}$ | $V_{GS}$ = -15 V, $V_{DS}$ = 0 V | -1 | | | pA |
| | | $T_A$ = 150°C | -2 | | | nA |
| Gate Operating Current | $I_G$ | $V_{DG}$ = 10 V, $I_D$ = 5 mA | -1 | | | pA |
| | | $T_A$ = 125°C | -0.3 | | | nA |
| Gate-Source Voltage | $V_{GS}$ | $V_{DG}$ = 10 V, $I_D$ = 5 mA | -1.5 | | | V |
| Gate-Source Forward Voltage | $V_{GS(F)}$ | $V_{DS}$ = 0 V, $I_G$ = 1 mA | 0.7 | | | |
| **DYNAMIC** | | | | | | |
| Common-Source Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 5 mA, f = 1 kHz | 6 | | | mS |
| Common-Source Output Conductance | $g_{os}$ | | 20 | | | µS |
| Common-Source Forward Transconductance | $g_{fs}$ | $V_{DG}$ = 10 V, $I_D$ = 5 mA, f = 100 MHz | 6 | | | mS |
| Common-Source Output Conductance | $g_{os}$ | | 30 | | | µS |
| Common-Source Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, $I_D$ = 5 mA, f = 1 kHz | 3.5 | | | pF |
| Common-Source Reverse Transfer Capacitance | $C_{rss}$ | | 1 | | | |
| Equivalent Input Noise Voltage | $\bar{e}_n$ | $V_{DS}$ = 10 V, $I_D$ = 5 mA, f = 10 kHz | 4 | | | $nV/\sqrt{Hz}$ |
| Noise Figure | NF | $R_G$ = 100 kΩ | 0.1 | | | dB |
| **MATCHING** | | | | | | |
| Differential Gate-Source Voltage | $\lvert V_{GS1} - V_{GS2} \rvert$ | $I_D$ = 5 mA, $V_{DG}$ = 10 V | 7 | | 10 | mV |
| Gate-Source Voltage Differential Change with Temperature | $\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ | $I_D$ = 5 mA, $V_{DG}$ = 10 V; T = -55 to 25°C | 10 | | | µV/°C |
| | | T = 25 to 125°C | 10 | | | |
| Saturation Drain Current Ratio | $\frac{I_{DSS1}}{I_{DSS2}}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V | 0.98 | | | |
| Transconductance Ratio | $\frac{g_{fs1}}{g_{fs2}}$ | $V_{DG}$ = 10 V, $I_D$ = 5 mA, f = 1 kHz | 0.98 | | | |
| Differential Gate Current | $\lvert I_{G1} - I_{G2} \rvert$ | $V_{DG}$ = 10 V, $I_D$ = 5 mA, $T_A$ = 125°C | 0.005 | | | nA |
| Common Mode Rejection Ratio | CMRR | $V_{DD}$ = 5 to 10 V, $I_D$ = 5 mA | 90 | | | dB |

NOTES:
a. $T_A$ = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4