H5N0301SM

Silicon N Channel Power MOS FET
Power Switching

HITACHI

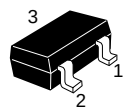
ADE-208-954 (Z)
1st. Edition
Dec. 2000

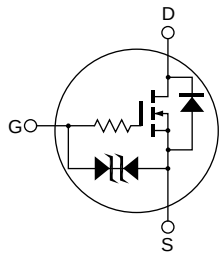
Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device

Outline

SMPAK





1. Source
2. Gate
3. Drain

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	50	mA
Drain peak current	$I_{D(pulse)}$ Note 1	200	mA
Channel dissipation	$Pch_{(pulse)}$ Note 2	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

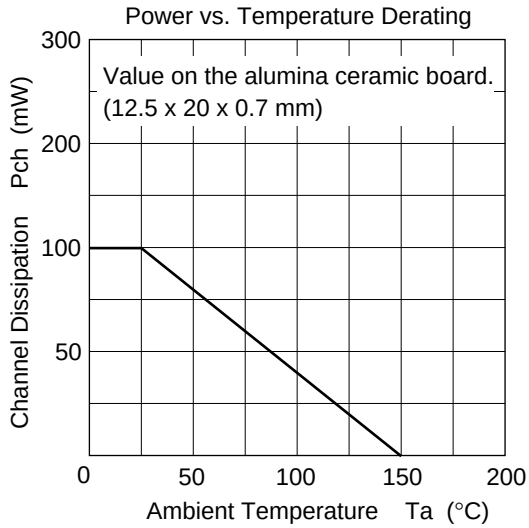
Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value on the alumina ceramic board (12.5 x 20 x 0.7 mm)

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±8 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.8	—	1.8	V	I_D = 10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	6	7.2	Ω	I_D =25m A, V_{GS} =4 V Note 1
		—	9	13	Ω	I_D=10mA,V_{GS} =2.5 V Note 1
Forward transfer admittance	$\|y_{fs}\|$	65	85	—	mS	I_D=25mA,,V_{DS}=10 V Note 1
Input capacitance	Ciss	—	12	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	8	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	40	—	ns	V_{GS} = 4 V, I_D = 25m A
Rise time	t_r	—	115	—	ns	R_L = 400 Ω
Turn-off delay time	$t_{d(off)}$	—	120	—	ns	
Fall time	t_f	—	125	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.82	1.23	V	I_F = 50m A, V_{GS} = 0 Note 1

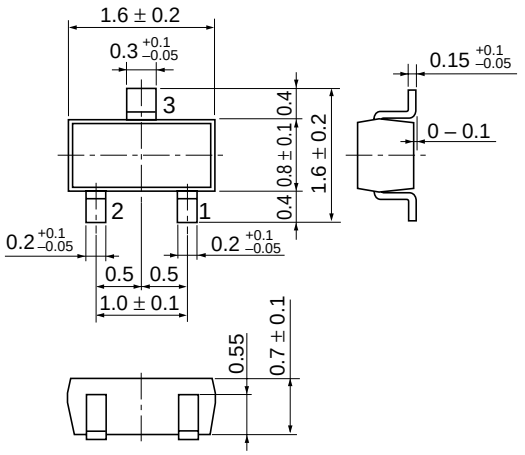
Note: 1. Pulse test

Main Characteristics



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	SMPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.003 g

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