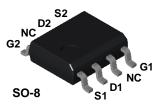
# Index of /ds/NP/

	Name	Last modif	ied	Size	Description
	Parent Directory				
<u> </u>	NPDS402.pdf	22-Dec-99	00:13	123K	
<u> </u>	NPDS403.pdf	22-Dec-99	00:13	123K	
Ŀ)_	NPDS404.pdf	22-Dec-99	00:13	123K	
Ŀì_	NPDS405.pdf	22-Dec-99	00:13	123K	
<u> </u>	NPDS5565.pdf	22-Dec-99	00:13	130K	
<u> </u>	NPDS5566.pdf	22-Dec-99	00:13	130K	
D`_	NPDS5911.pdf	22-Dec-99	00:13	121K	
D`_	NPDS5912.pdf	22-Dec-99	00:13	121K	
D_	NPDS8301.pdf	22-Dec-99	00:13	109K	
D`_	NPDS8302.pdf	22-Dec-99	00:13	109K	
<u> </u>	NPDS8303.pdf	22-Dec-99	00:13	109K	
[``	NPN_Epitaxial_Silicon+	16-Apr-99	13:01	73K	

Discrete POWER & Signal Technologies





# **N-Channel General Purpose Dual Amplifier**

Sourced from Process 98.

FAIRCHIL

SEMICONDUCTOR 11

# **Absolute Maximum Ratings\***

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V <sub>DG</sub>	Drain-Gate Voltage	50	V
V <sub>GS</sub>	Gate-Source Voltage	50	V
I <sub>GF</sub>	Forward Gate Current	10	mA
T <sub>J</sub> ,T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

\*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

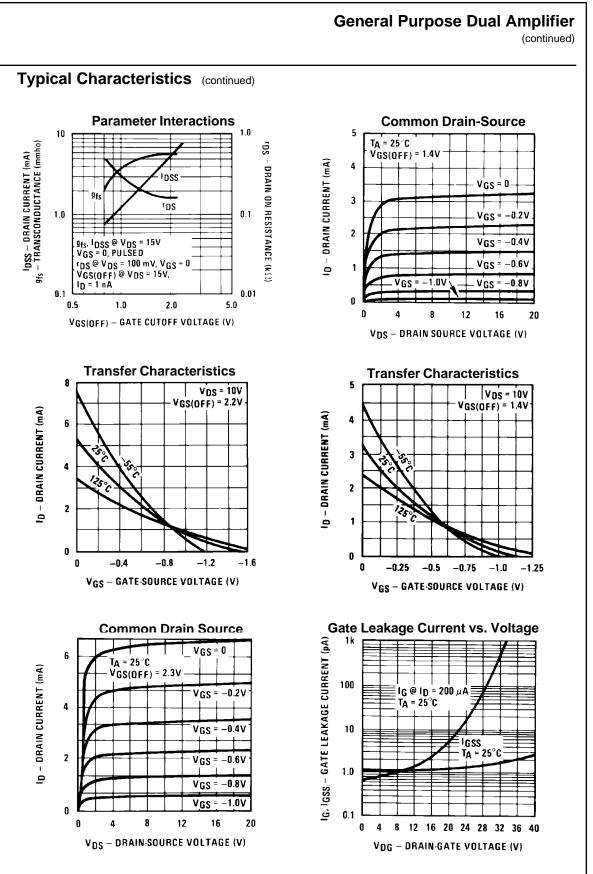
#### NOTES:

1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations

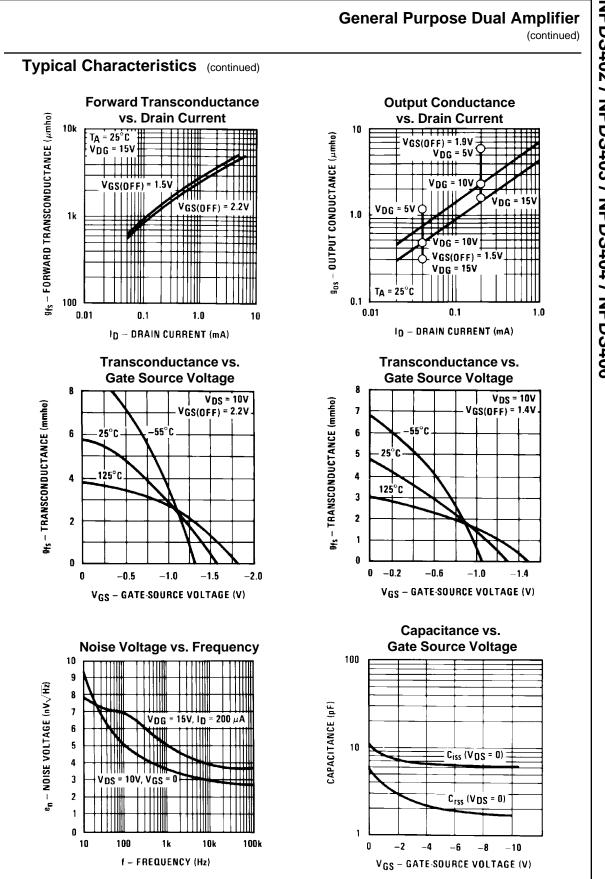
©1997 Fairchild Semiconductor Corporation

		General Purp	oose D		nplifie (continued
Electr Symbol	ical Characteristics TA =	= 25°C unless otherwise noted Test Conditions	Min	Мах	Units
Cymbol	i arameter			Max	Units
	RACTERISTICS				
V <sub>(BR)GSS</sub>	Gate-Source Breakdown Voltage	$I_{G} = 1.0 \ \mu A, V_{DS} = 0$	- 50		V
	Gate Reverse Current	$V_{GS} = 30 \text{ V},  V_{DS} = 0$	- 50	25	pA
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	$V_{DS} = 35 \text{ V}, V_{DS} = 0$ $V_{DS} = 15 \text{ V}, I_D = 1.0 \text{ nA}$	- 0.5	- 2.5	V
V <sub>GS</sub> (off)	Gate-Source Voltage	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 200 \mu\text{A}$	0.0	- 2.3	V
V <sub>G1 - G2</sub>	Voltage Gate 1-Gate 2	$I_{G} = 1.0 \ \mu A, V_{DS} = 0$	+/-50	2.0	V
I <sub>DSS</sub>	ACTERISTICS Zero-Gate Voltage Drain Current*	$V_{DS} = 10 \text{ V}, V_{GS} = 0$	0.5	10	mA
SMALL SI	GNAL CHARACTERISTICS				
9fs	Common Source Forward Transconductance		2000 1000	7000 2000	μmhos μmhos
goss	Common Source Output Conductance	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0, \text{ f} = 1.0 \text{ kHz}$		20	μmhos
g <sub>os</sub>	Common Source Output Conductance	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 200 \mu \text{A}, \text{ f} = 1.0 \text{ kHz}$		2.0	μmhos
C <sub>iss</sub>	Input Capacitance	$V_{DG} = 15 \text{ V}, I_D = 200 \ \mu\text{A}, f = 1.0 \text{ MHz}$		8.0	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DG}$ = 15 V, $I_D$ = 200 µA, f = 1.0 MHz		3.0	pF
CMMR	Common Mode Rejection	$V_{DG}$ = 10 to 20 V, $I_{D}$ = 200 $\mu A$	95		dB
$V_{GS1}$ , $V_{GS2}$	Differential Match	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 200 μA, NPDS402 NPDS403		10 10	
		NPDS403 NPDS404 NPDS406		15 40	mV mV mV mV

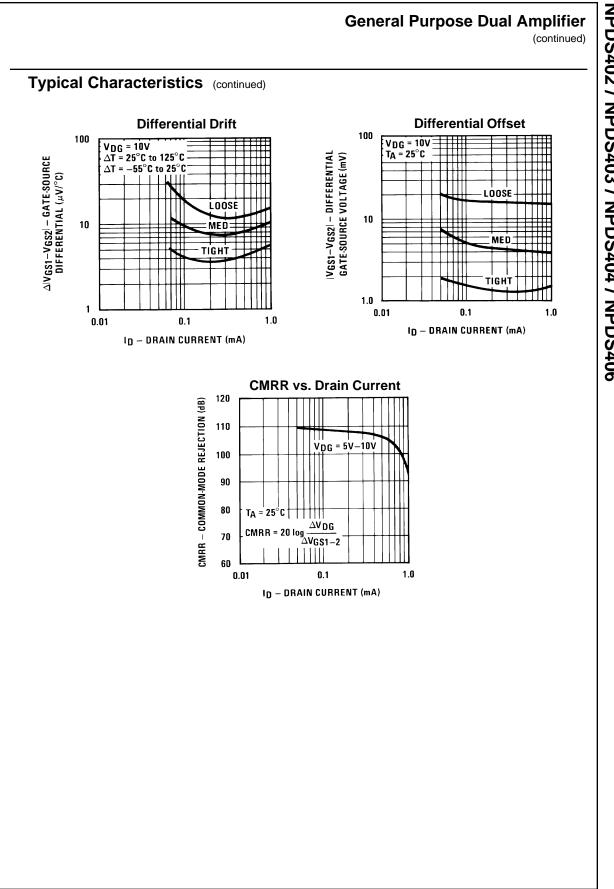
\*Pulse Test: Pulse Width  $\leq$  300 ms, Duty Cycle  $\leq$  2%



NPDS402 / NPDS403 / NPDS404 / NPDS406



NPDS402 / NPDS403 / NPDS404 / NPDS406



NPDS402 / NPDS403 / NPDS404 / NPDS406

Discrete POWER & Signal Technologies



# **NPDS5565 NPDS5566**



# **N-Channel General Purpose Dual Amplifier**

Sourced from Process 96.

#### **Absolute Maximum Ratings\*** TA = 25°C unless otherwise noted

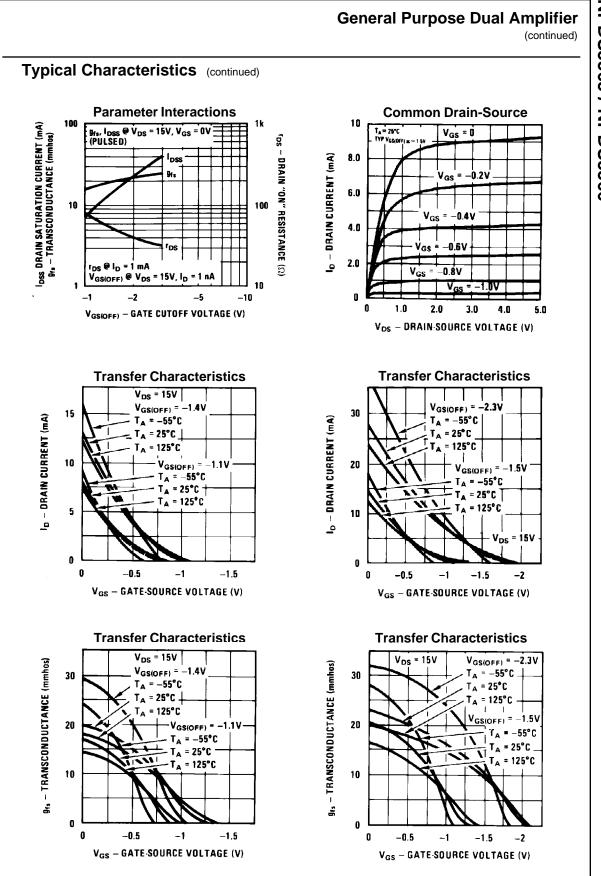
Symbol	Parameter	Value	Units
$V_{DG}$	Drain-Gate Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	40	V
I <sub>GF</sub>	Gate Current	10	mA
T」,T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

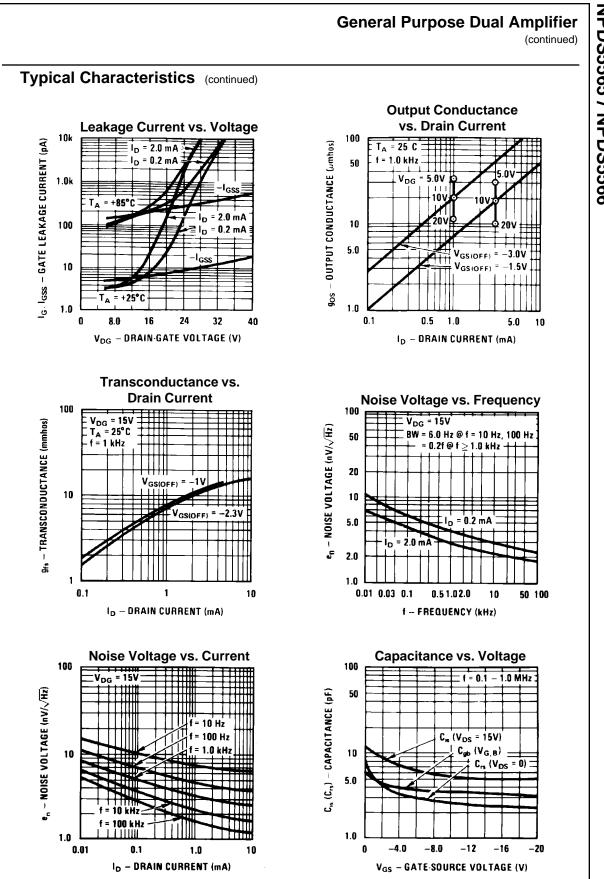
\*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

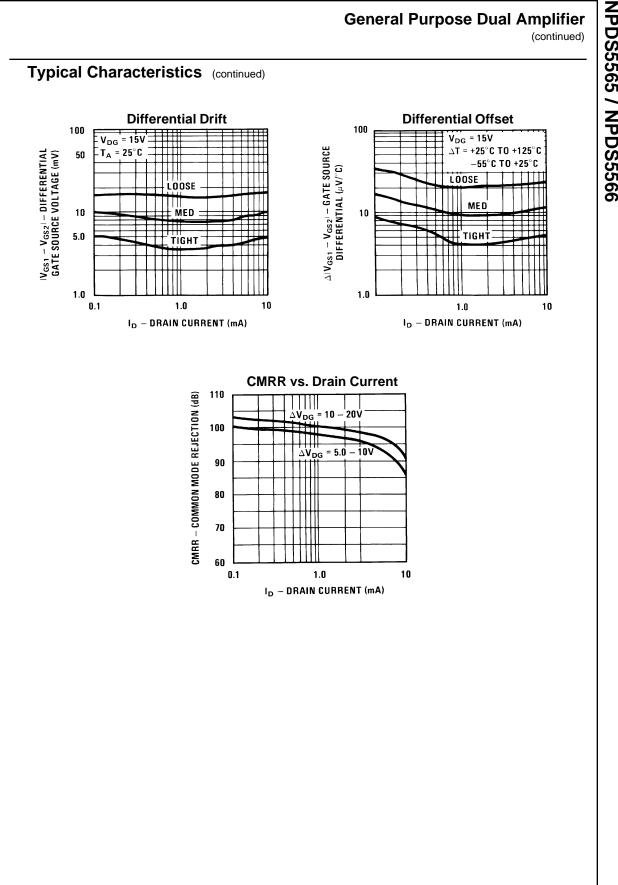
### NOTES:

1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Symbol	Parameter	Test Conditions	Min	Мах	Units
			I		
	RACTERISTICS		10		M
V <sub>(BR)GSS</sub>	Gate-Source Breakdown Voltage	$I_{G} = 1.0 \ \mu A, V_{DS} = 0$	- 40	100	V
GSS	Gate Reverse Current	$V_{GS} = 20 V, V_{DS} = 0$ $V_{GS} = 20 V, V_{DS} = 0, T_A = 150 \text{ °C}$		100 200	pΑ μΑ
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	$V_{DS} = 15 \text{ V}, I_D = 1.0 \text{ nA}$	- 0.5	- 3.0	V
V <sub>GS(f)</sub>	Forward Gate-Source Voltage	$V_{DS} = 0, I_{D} = 2.0 \text{ mA}$		1.0	V
V <sub>G1 - G2</sub>	Voltage Gate 1 - Gate 2	$V_{DS}$ = 0, $I_{G}$ = + / - 1.0 $\mu$ A	+/-40		V
ON CHAR	ACTERISTICS				1
DSS	Zero-Gate Voltage Drain Current*	$V_{DS} = 15 V, V_{GS} = 0$	5.0	30	mA
f <sub>DS(on)</sub>	Drain-Source On Resistance	$I_{D} = 1.0 \text{ mA}, V_{GS} = 0$		100	Ω
SMALL SI 9fs	GNAL CHARACTERISTICS Common Source Forward Transconductance	$V_{DS} = 15 \text{ V}, \text{ I}_D = 2.0 \text{mA}, \text{ f} = 1.0 \text{ kHz}$ $V_{DS} = 15 \text{ V}, \text{ I}_D = 2.0 \text{ mA}, \text{ f} = 100 \text{ MHz}$	7500 7000	12,500	μmhos μmhos
oss	Common Source Output Conductance	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 2.0 \text{mA}, \text{ f} = 1.0 \text{ kHz}$		45	μmhos
Ciss	Input Capacitance	$V_{DG} = 15 \text{ V}, I_D = 2.0 \text{mA}, f = 1.0 \text{MHz}$		12	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, I_D = 2.0 \text{mA}, f = 1.0 \text{ kHz}$		3.0	pF
Ðn	Equivalent Short-Circuit Input Noise Voltage	$V_{DG}$ = 15 V, I <sub>D</sub> = 2.0 mA, f = 10 Hz		50	nV/√Hz
NF	Noise Figure	$\label{eq:V_DG} \begin{array}{l} V_{\text{DG}} = 15 \text{ V}, \text{ I}_{\text{D}} = 2.0 \text{ mA}, \text{ f} = 10 \text{ Hz} \\ R_{\text{G}} = 1.0 \text{ m}\Omega \end{array}$		1.0	dB
<sub>DSS1</sub> - I <sub>DSS2</sub>	I <sub>DSS</sub> Match	$V_{DS} = 15 V, V_{GS} = 0$		5.0	%
9fs1 - 9fs2	g <sub>fs</sub> Match	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 2.0 \text{mA}, \text{ f} = 1.0 \text{ kHz}$		10	%
$V_{GS1}$ , $V_{GS2}$	Differential Match	V <sub>DG</sub> = 15 V, I <sub>D</sub> = 2.0 mA, NPDS5565 NPDS5566		10 20	mV mV
V <sub>GS1 -</sub> V <sub>GS2</sub>	Differential Drift			25 50	μV/°C μV/°C
		T <sub>A</sub> = -55 to 25 °C NPDS5565 NPDS5566		25 50	μV/°C μV/°C

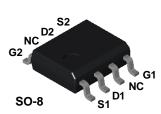






Discrete POWER & Signal Technologies

# **NPDS5911 NPDS5912**



# **N-Channel General Purpose Dual Amplifier**

Sourced from Process 93.

FAIRCHILD SEMICONDUCTOR 11

#### **Absolute Maximum Ratings\*** TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
$V_{DG}$	Drain-Gate Voltage	25	V
V <sub>GS</sub>	Gate-Source Voltage	25	V
I <sub>GF</sub>	Forward Gate Current	10	mA
T <sub>J</sub> ,T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

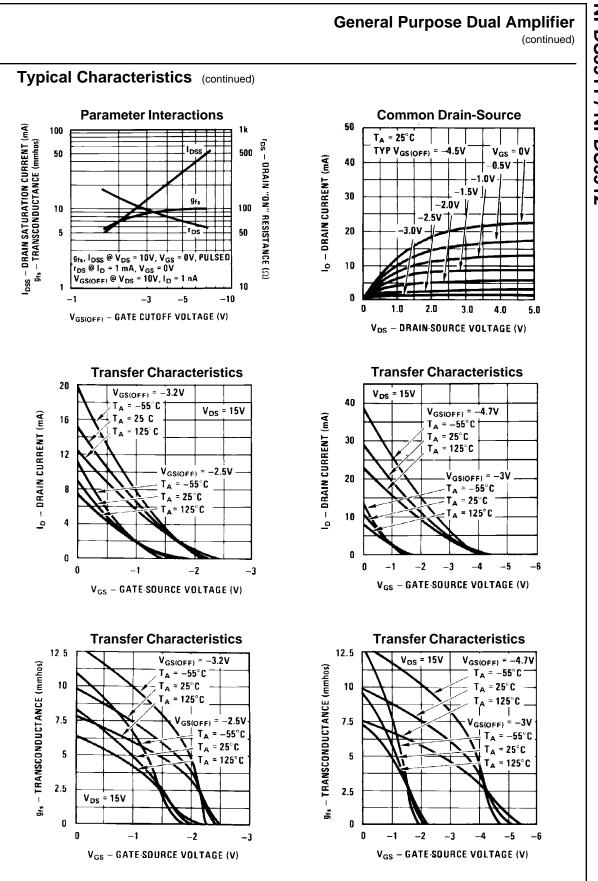
\*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

### NOTES:

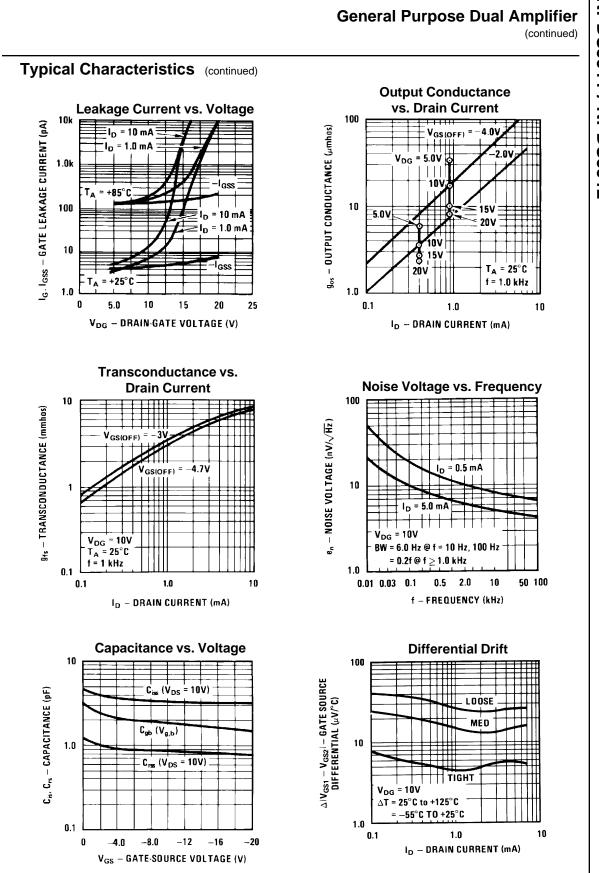
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

	ical Characteristics TA =	= 25°C unless otherwise noted			
Symbol	Parameter	Test Conditions	Min	Мах	Units
OFF CHA	RACTERISTICS				
V <sub>(BR)GSS</sub>	Gate-Source Breakdown Voltage	$I_G = 1.0 \ \mu A, V_{DS} = 0$	- 25		V
I <sub>GSS</sub>	Gate Reverse Current	$V_{GS} = 15 \text{ V}, V_{DS} = 0$ $V_{GS} = 15 \text{ V}, V_{DS} = 0, T_A = 150 ^{\circ}\text{C}$		100 250	pA nA
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1.0 \text{ nA}$	- 1.0	- 5.0	V
V <sub>GS</sub>	Gate-Source Voltage	$V_{DG} = 10 \text{ V}, \text{ I}_{D} = 5.0 \text{ mA}$	- 0.3	- 4.0	V
V <sub>G1 - G2</sub>	Voltage Gate 1 - Gate 2	$V_{DS} = 0, I_G = + / - 1.0 \mu A$	+/-25		V
	ACTERISTICS Zero-Gate Voltage Drain Current*	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0$	7.0	40	mA
	Transconductance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 5.0 \text{ mA},$ f = 100 MHz	5000	10,000	μmhos
goss	Common Source Output Conductance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 5.0 \text{mA}, \text{ f} = 1.0 \text{ kHz}$		100	μmhos
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10V, I_D = 5.0mA, f = 100 MHz$ $V_{DG} = 10 V, I_D = 5.0mA, f = 1.0 MHz$		150 5.0	μmhos pF
0155	· · ·	·bg iet,ib eleinini, ine ini≞		0.0	
Cree	Reverse Transfer Capacitance	$V_{DS} = 10 V$ , $I_{D} = 5.0 mA$ , $f = 1.0 kHz$		1.2	•
	Reverse Transfer Capacitance Equivalent Short-Circuit Input Noise Voltage	$V_{DS} = 10 \text{ V},  \text{I}_{D} = 5.0 \text{ mA},  \text{f} = 1.0 \text{ kHz}$ $V_{DG} = 10 \text{ V},  \text{I}_{D} = 5.0 \text{ mA},  \text{f} = 10 \text{ kHz}$		1.2 20	pF
e <sub>n</sub>		$V_{DG}$ = 10 V, I <sub>D</sub> = 5.0 mA, f = 10 kHz $V_{DG}$ = 10 V, I <sub>D</sub> = 5.0 mA, f = 10 kHz			pF
e <sub>n</sub> NF	Equivalent Short-Circuit Input Noise Voltage	$V_{DG}$ = 10 V, I <sub>D</sub> = 5.0 mA, f = 10 kHz		20	pF nV/√Hz
e <sub>n</sub> NF I <sub>DSS1</sub> -I <sub>DSS2</sub>	Equivalent Short-Circuit Input Noise Voltage Noise Figure	$V_{DG} = 10 \text{ V}, \text{ I}_{D} = 5.0 \text{ mA}, \text{ f} = 10 \text{ kHz}$ $V_{DG} = 10 \text{ V}, \text{ I}_{D} = 5.0 \text{ mA}, \text{ f} = 10 \text{ kHz}$ $R_{G} = 100 \text{ k}\Omega$		20 1.0	pF nV/√Hz dB
e <sub>n</sub> NF I <sub>DSS1</sub> -I <sub>DSS2</sub> gfs1 - gfs2	Equivalent Short-Circuit Input Noise Voltage Noise Figure	$\begin{split} V_{DG} &= 10 \ V, \ I_D = 5.0 \ m\text{A}, \ f = 10 \ \text{kHz} \\ V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 10 \ \text{kHz} \\ R_G &= 100 \ \text{k}\Omega \\ V_{DS} &= 10 \ V, \ V_{GS} &= 0 \end{split}$		20 1.0 5.0	pF nV/√Hz dB %
en NF I <sub>DSS1</sub> -I <sub>DSS2</sub> gfs1 - gfs2 goss1 -goss2	Equivalent Short-Circuit Input Noise Voltage Noise Figure I <sub>DSS</sub> Match g <sub>fs</sub> Match	$\begin{split} V_{DG} &= 10 \; V, \; I_D = 5.0 \; \text{mA}, \; f = 10 \; \text{kHz} \\ V_{DG} &= 10 \; V, \; I_D = 5.0 \; \text{mA}, \; f = 10 \; \text{kHz} \\ R_G &= 100 \; \text{k}\Omega \\ V_{DS} &= 10 \; V, \; V_{GS} = 0 \\ V_{DS} &= 10 \; V, \; I_D = 5.0 \text{mA}, \; f = 1.0 \; \text{kHz} \end{split}$		20 1.0 5.0 5.0	pF nV/√Hz dB %
e <sub>n</sub> NF I <sub>DSS1</sub> -I <sub>DSS2</sub> gfs1 - gfs2 goss1 -goss2 I <sub>G1</sub> - I <sub>G2</sub>	Equivalent Short-Circuit Input Noise Voltage Noise Figure I <sub>DSS</sub> Match g <sub>fs</sub> Match g <sub>oss</sub> Match	$\begin{split} V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 10 \ \text{kHz} \\ V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 10 \ \text{kHz} \\ R_G &= 100 \ \text{k}\Omega \\ V_{DS} &= 10 \ V, \ V_{GS} = 0 \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ T_A = 125^\circ \text{C} \\ V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ \textbf{NPDS5911} \end{split}$		20 1.0 5.0 20 20 10	pF nV/√Hz dB % μmhos nA mV
Crss           θn           NF           lbss1 -lbss2           gfs1 - gfs2           goss1 -goss2           Ig1 - lg2           VGS1 - VGS2	Equivalent Short-Circuit Input Noise Voltage Noise Figure I <sub>DSS</sub> Match g <sub>rs</sub> Match I <sub>G</sub> Match	$\begin{split} V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 10 \ \text{kHz} \\ V_{DG} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 10 \ \text{kHz} \\ R_G &= 100 \ \text{k}\Omega \\ V_{DS} &= 10 \ V, \ V_{GS} = 0 \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \\ V_{DS} &= 10 \ V, \ I_D = 5.0 \ \text{mA}, \ f = 1.0 \ \text{kHz} \end{split}$		20 1.0 5.0 5.0 20 20	pF nV/√Hz dB % μmhos nA

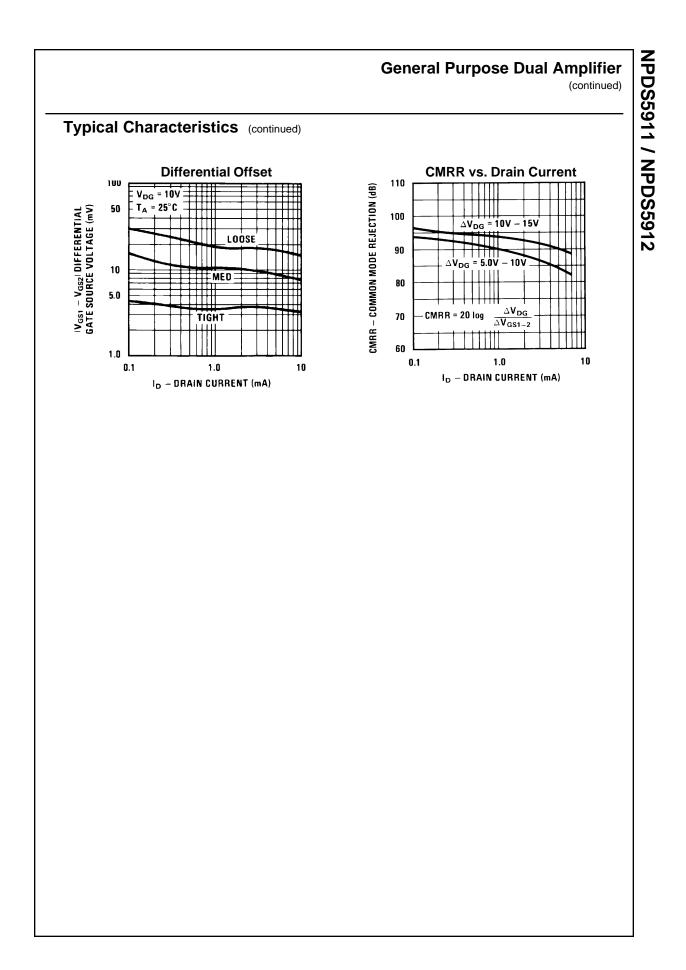
\*Pulse Test: Pulse Width  $\leq$  300 ms, Duty Cycle  $\leq$  2%



NPDS5911 / NPDS5912

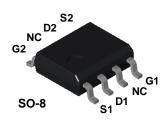


NPDS5911 / NPDS5912



Discrete POWER & Signal **Technologies** 





# **N-Channel General Purpose Dual Amplifier**

Sourced from Process 83.

FAIRCHILD

SEMICONDUCTOR 11

# **Absolute Maximum Ratings\***

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V <sub>DG</sub>	Drain-Gate Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	40	V
I <sub>GF</sub>	Forward Gate Current	10	mA
$T_J$ , $T_stg$	Operating and Storage Junction Temperature Range	-55 to +150	°C

\*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

#### NOTES:

1) These ratings are based on a maximum junction temperature of 150 degrees C.
 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

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# **General Purpose Dual Amplifier**

V<sub>GS</sub> = 0V

-0.3V

-0.6V 0,9V

-1.2V 1.5V

3.0

5.0

4.0

(continued)

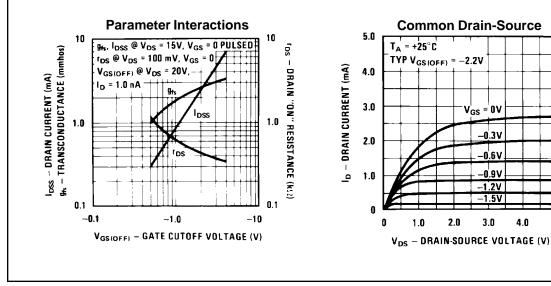
Symbol	Parameter	Test Conditions	Min	Max	Units
)FF CH4	ARACTERISTICS				
(BR)GSS	Gate-Source Breakdown Voltage	$I_{G} = 1.0 \ \mu A, V_{DS} = 0$	- 40		V
SS	Gate Reverse Current	$V_{GS} = 20 \text{ V}, \text{ V}_{DS} = 0$		100	pА
S(off)	Gate-Source Cutoff Voltage	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 1.0 \text{ nA}$	- 0.5	- 3.5	V
s	Gate-Source Voltage	$V_{DS} = 20 \text{ V}, I_D = 200 \mu\text{A}$	- 0.3	- 3.5	V

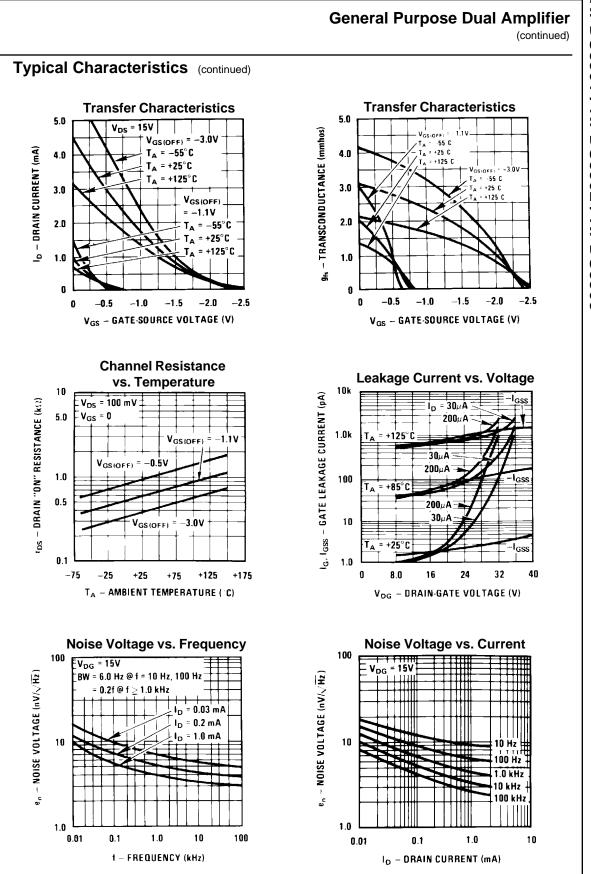
# SMALL SIGNAL CHARACTERISTICS

<b>g</b> fs	Common Source Forward Transconductance	$V_{DS} = 20 V$ , $V_{GS} = 0$ , f = 1.0 kHz $V_{DS} = 20 V$ , $I_D = 200 \mu A$ ,	1000 700	4000 1200	μmhos μmhos
		f = 1.0  kHz			μιπιου
goss	Common Source Output Conductance	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 200 \mu\text{A},$ f = 1.0 kHz		20	μmhos
g <sub>os</sub>	Common Source Output Conductance	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 200 \mu\text{A},$ f = 1.0 kHz		5.0	μmhos
$V_{GS1}$ , $V_{GS2}$	Differential Match	$V_{DG} = 20 \text{ V}, \text{ I}_{D} = 200 \mu\text{A},$			
		NPDS8301		5.0	mV
		NPDS8302		10	mV
		NPDS8303		15	mV
$\Delta V_{GS1}$ V <sub>GS2</sub>	Differential Drift	$V_{DS} = 20 \text{ V}, I_{D} = 200 \mu\text{A},$			
		T <sub>A</sub> = 25 to 85 °C <b>NPDS8301</b>		10	μV/°C
		NPDS8302		15	μV/°C
		NPDS8303		25	μV/°C

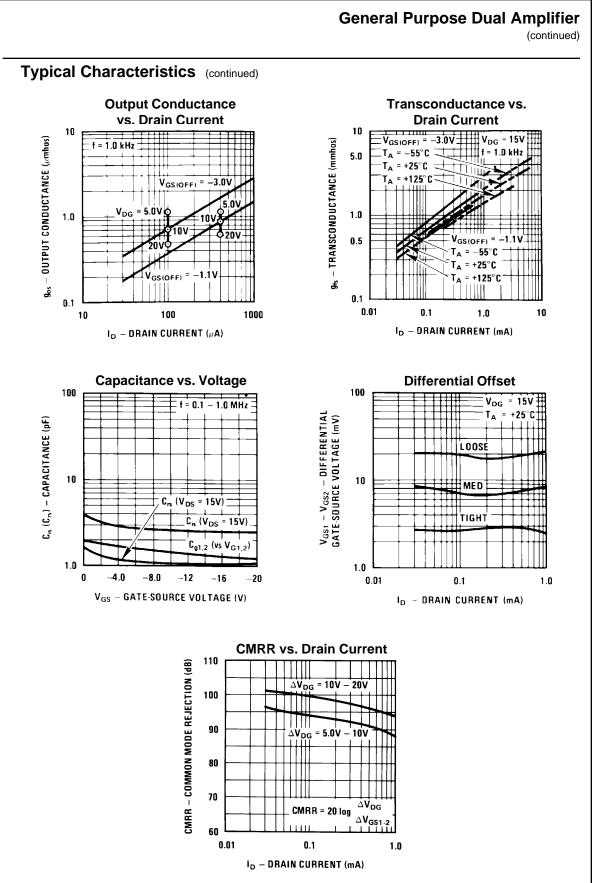
\*Pulse Test: Pulse Width  $\leq$  300 ms, Duty Cycle  $\leq$  2%

# **Typical Characteristics**





NPDS8301 / NPDS8302 / NPDS8303



# NPDS8301 / NPDS8302 / NPDS8303

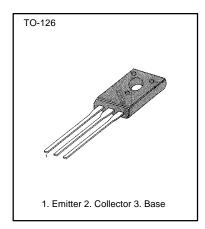
# NPN EPITAXIAL MJE800/801/803 SILICON DARLINGTON TRANSISTOR

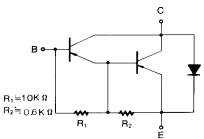
# HIGH DC CURRENT GAIN MIN $h_{FE}$ 750 I $_{C}$ -1.5 and -2.0A DC MONOLITHIC CONSTRUCTION WITH BUILT-IN BASE-EMITTER RESISTORS

• Complement to MJE700/701/702/703

# **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Rating	Unit
Collector- Base Voltage	V <sub>CBO</sub>		
: MJE800/801		60	V
: MJE802/803		80	V
Collector-Emitter Voltage	V <sub>CEO</sub>		
: MJE800/801		60	V
: MJE802/803		80	V
Emitter- Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C</sub>	4	А
Base Current	IB	0.1	Α
Collector Dissipation (T <sub>c</sub> =25°C)	Pc	40	W
Junction Temperature	TJ	150	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ 150	°C





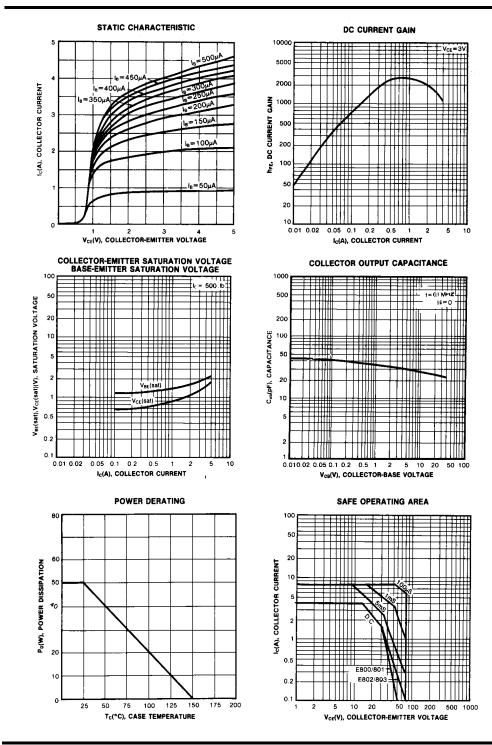
# ELECTRICAL CHARACTERISTICS (Tc=25°C)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector Emitter Breakdown Voltage	BV <sub>CEO</sub>	$I_{\rm C} = 50 {\rm mA}, \ I_{\rm B} = 0$			
: MJE800/801			60		V
: MJE802/803			80		V
Collector Cutoff Current	ICEO				
: MJE800/801		$V_{CE} = 60V, I_B = 0$		100	μA
: MJE802/803		$V_{CE} = 80V, I_{B} = 0$		100	μA
Collector Cutoff Current	I <sub>CBO</sub>	$V_{CB} = Rated BV_{CEO}, I_E = 0$		100	μA
		$V_{CB}$ = Rated BV <sub>CEO</sub> , I <sub>E</sub> = 0		500	μA
		$T_{\rm C} = 100^{\circ}{\rm C}$			μοι
Emitter Cutoff Current	I <sub>EBO</sub>	$V_{BF} = 5V, I_{C} = 0$		2	mA
DC Current Gain : MJE800/802	h <sub>FE</sub>	$V_{CE} = 3V, I_{C} = 1.5A$	750		
: MJE801/803		$V_{CE} = 3V, I_{C} = 2A$	750		
: ALL DEVICES		$V_{CE} = 3V, I_{C} = 4A$	100		
Collector-Emitter Saturation Voltage	V <sub>CE</sub> (sat)				
: MJE800/802		$I_{\rm C} = 1.5$ A, $I_{\rm B} = 30$ mA		2.5	V
: MJE801/803		$I_{\rm C} = 2A, I_{\rm B} = 40 {\rm mA}$		2.8	v
: ALL DEVICES		$I_{C} = 4A, I_{B} = 40mA$		3	v
Base-Emitter On Voltage	V <sub>BE</sub> (on)				·
: MJE800/802		$V_{CE} = 3V, I_{C} = 1.5A$		1.2	V
: MJE801/803		$V_{CE} = 3V, I_C = 2A$		2.5	v
: ALL DEVICES		$V_{CE} = 3V, I_{C} = 4A$		3	v



Rev. B.1

# NPN EPITAXIAL MJE800/801/803 SILICON DARLINGTON TRANSISTOR



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