



NQP1 DIE

N-Channel JFET Pair

T-29-27

The NQP1 Die is a monolithic JFET pair designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This die features tight matching specs, low gate leakage for accuracy, and wide dynamic range as I_G is measured at $V_{DG} = 20$ V. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

NQP1CHP*
2N5198 2N5199
*Meets or exceeds specification for all part numbers listed below

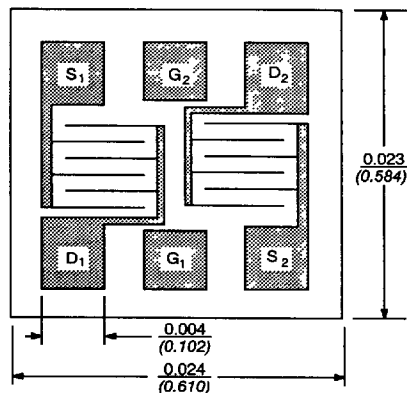
For additional design information please consult the typical performance curves NQP.

DESIGNED FOR:

- General Purpose Amplifiers

FEATURES

- High Input Impedance



Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

NQP1 DIE



SPECIFICATIONS ^a			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ^b	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-57	-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = 20 V, I_D = 1 nA$	-2	-0.7	-4	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 20 V, V_{GS} = 0 V$	3	0.7	7	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -30 V, V_{DS} = 0 V$	-10			pA
		$T_A = 150^\circ C$	-20			nA
Gate Operating Current	I_G	$V_{DG} = 20 V, I_D = 200 \mu A$	-5			pA
		$T_A = 125^\circ C$	-0.8			nA
Gate-Source Voltage	V_{GS}	$V_{DG} = 20 V, I_D = 200 \mu A$	-1.5			
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz$	2.5			mS
Common-Source Output Conductance	g_{os}		2			μS
Common-Source Forward Transconductance	g_{fs}	$V_{DG} = 20 V, I_D = 20 \mu A, f = 1 kHz$	0.8			mS
Common-Source Output Conductance	g_{os}		1			μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz$	3			pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1			
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz$	9			$\frac{nV}{\sqrt{Hz}}$
Noise Figure	NF	$V_{DS} = 20 V, V_{GS} = 0 V$ $f = 100 Hz, R_G = 10 M\Omega$				dB
MATCHING						
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$I_D = 200 \mu A, V_{DG} = 20 V$	7		10	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$I_D = 200 \mu A$ $V_{DG} = 20 V$	$T = -55 \text{ to } 25^\circ C$	10		$\mu V/^\circ C$
			$T = 25 \text{ to } 125^\circ C$	10		
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 20 V, V_{GS} = 0 V$	0.97			
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DG} = 20 V, I_D = 200 \mu A, f = 1 kHz$	0.97			
Differential Output Capacitance	$ g_{os1} - g_{os2} $		0.2			μS
Differential Gate Current	$ I_{G1} - I_{G2} $	$V_{DG} = 20 V, I_D = 200 \mu A$ $T_A = 125^\circ C$	0.1			nA
Common Mode Rejection Ratio	CMRR	$V_{DD} = 10 \text{ to } 20 V, I_D = 200 \mu A$	97			dB

NOTES:

- a. $T_A = 25^\circ C$ unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; $PW = 300 \mu s$, duty cycle $\leq 3\%$.