National Semiconductor Corporation

NS32201-6/NS32201-8/NS32201-10 Timing Control Units

General Description

The NS32201 Timing Control Unit (TCU) is a 24-pin device fabricated on a Schottky bipolar process. It provides a two-phase clock, system control logic and cycle extension logic for the Series 32000® microprocessor family. The TCU input clock can be provided by either a crystal or an external clock signal whose frequency is twice the system clock frequency.

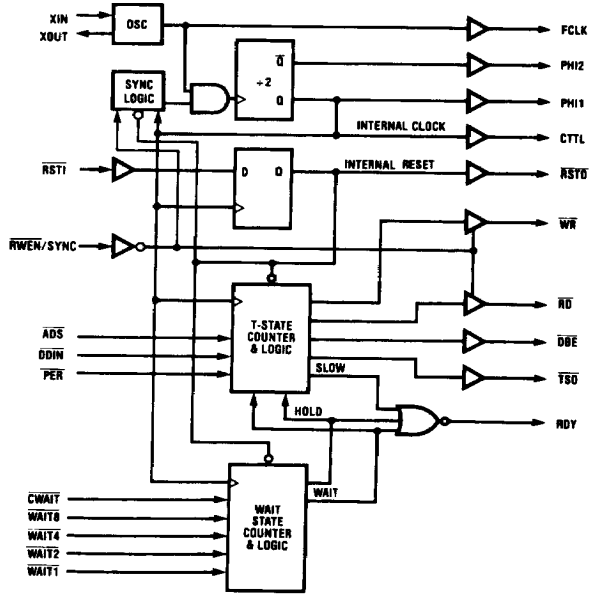
In addition to the two-phase clock for the CPU and MMU (PHI1 and PHI2), it also provides two system clocks for general use within the system (FCLK and CTTL). FCLK is a fast clock whose frequency is the same as the input clock, while CTTL is a TTL replica of PHI1 clock.

The system control logic and cycle extension logic make the TCU very attractive by providing extremely accurate bus control signals, and allowing extensive control over the bus cycle timing.

Features

- Oscillator at twice the CPU clock frequency
- 2 phase full V_{CC} swing high capacitance clock drivers (PHI1 and PHI2)
- 4-bit input ($\overline{WAITn}$) allowing precise specification of 0 to 15 wait states
- Cycle Hold for system arbitration and/or memory refresh
- System timing (FCLK, CTTL) and control ($\overline{RD}$, $\overline{WR}$, and $\overline{DBE}$) outputs
- General purpose Timing State Output ($\overline{TSO}$) that identifies internal states
- Peripheral cycle to accomodate slower MOS peripherals
- Provides "ready" (RDY) output for the Series 32000 CPUs
- Synchronous system reset generation from Schmitt trigger input
- Phase synchronization to a reference signal
- Single 5V power supply
- 24-pin dual-in-line package

Block Diagram



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1.0 Functional Description

1.1 POWER AND GROUNDING

The NS32201 requires a single +5V power supply, applied to pin 24 (V_{CC}). See D.C. Electrical Characteristics. The Logic Ground on pin 12 (GND), is the common pin for the TCU.

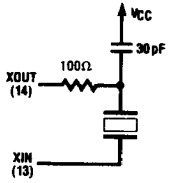
A 0.1 μf, ceramic decoupling capacitor must be connected across V_{CC} and GND, as close to the TCU as possible.

1.2 CRYSTAL OSCILLATOR CHARACTERISTICS

The NS32201 has a "Pierce"-type oscillator. Connections of the crystal and bias components to XIN and XOUT are shown in *Figure 1-1*. It is important that the crystal and the RC components be mounted in close proximity to the XIN, XOUT and V_{CC} pins to keep printed circuit trace lengths to an absolute minimum.

Typical Crystal Specifications:

Type ..... At-Cut
Tolerance ..... 0.005% at 25°C
Stability ..... 0.01% from 0° to 70°C
Resonance ..... Fundamental parallel
Capacitance ..... 20 pF
Maximum Series Resistance 50Ω



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CRYSTAL FREQUENCY (MHz)	R (OHM)
6–12	470
12–18	220
18–24	100
24–30	47

FIGURE 1-1. Crystal Connection Diagram

1.3 CLOCKS

The NS32201 TCU has four clock output pins. The PHI1 and PHI2 clocks are required by the Series 32000 CPUs. These clocks are non-overlapping as shown in *Figure 1-2*.

Each rising edge of PHI1 defines a transition in the timing state of the CPU.

As the TCU generates the various clock signals with very short transition timings, it is recommended that the conductors carrying PHI1 and PHI2 be kept as short as possible. It is also recommended that only the Series 32000 CPU and, if used, the MMU (Memory Management Unit) be connected to the PHI1 and PHI2 clocks. In addition to the CPU and MMU, 25 pF ceramic capacitors from these pins to ground are recommended as they provide a better VOH on the outputs. These capacitors should be mounted close to the TCU to minimize trace inductances.

CTTL is a TTL compatible clock signal which runs at the same frequency as PHI1 and is closely balanced with it. CTTL is intended for driving TTL loads.

FCLK is also a TTL compatible clock, running at the frequency of XIN input. This clock is also intended for driving TTL loads and has a frequency that is twice the CTTL clock frequency. The exact phase relationship between PHI1, PHI2, CTTL and FLCK can be found in Section 2.

1.4 RESETTING

The NS32201 TCU provides circuitry to meet the reset requirements of the Series 32000 CPUs. If the Reset Input line, $\overline{RSTI}$ is pulled low, the TCU asserts $\overline{RSTO}$ which resets the Series 32000 CPU. This Reset Output may also be used as a system reset signal. *Figure 1-3a* illustrates the reset connections for a non Memory-Managed system. *Figure 1-3b* illustrates the reset connections for a Memory-Managed system.

1.5 SYNCHRONIZING TWO OR MORE TCUs

During reset, (when $\overline{RSTO}$ is low), one or more TCUs can be synchronized with a reference (Master) TCU. The $\overline{RWEN}$/SYNC input to the slave TCU(s) is used for synchronization. The Slave TCU samples the $\overline{RWEN}$/SYNC input on the rising edge of FCLK when $\overline{RSTO}$ is low and CTTL is high (see *Figure 1-5*). If $\overline{RWEN}$/SYNC is sampled high, the phase of CTTL of the Slave TCU is shifted by one XIN clock cycle.

Two possible circuits for TCU synchronization are illustrated in *Figures 1-4a* and *1-4b*. It should be noted that when $\overline{RWEN}$/SYNC is high, the $\overline{RD}$ and $\overline{WR}$ signals will be TRI-STATE on the slave TCU.

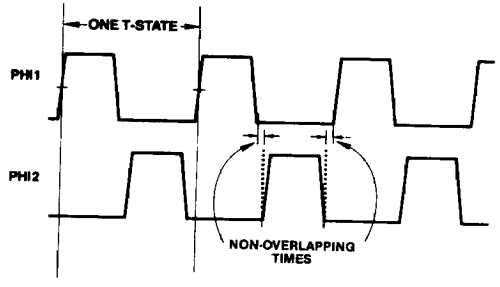

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FIGURE 1.2. PHI1 and PHI2 Clock Signals

1.0 Functional Description (Continued)

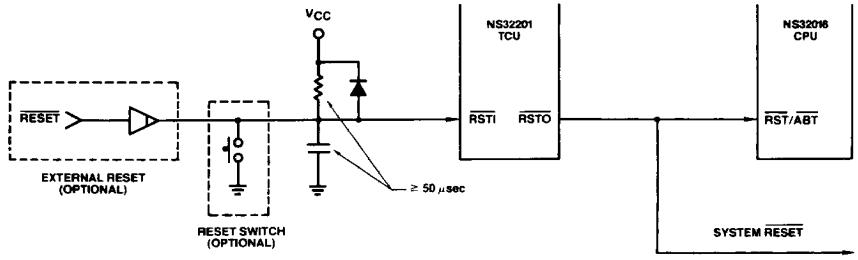

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FIGURE 1-3a. Recommended Reset Connections (Non Memory-Managed System)

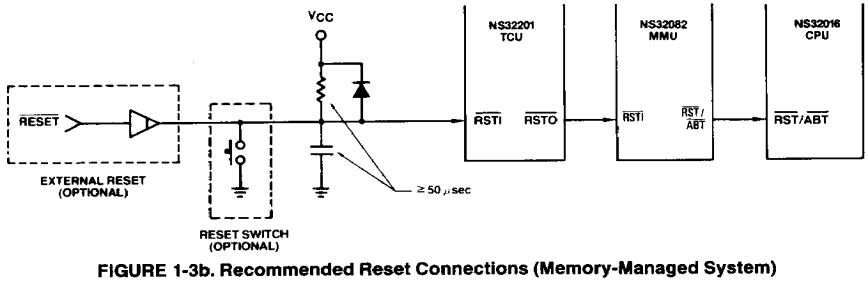

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FIGURE 1-3b. Recommended Reset Connections (Memory-Managed System)

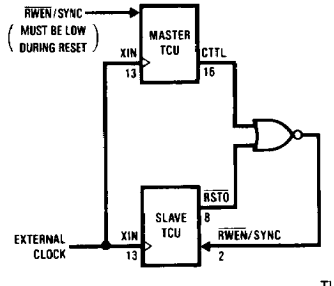

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FIGURE 1-4a. Slave TCU does not use $\overline{\text{RWEN}}$ during Normal Operation

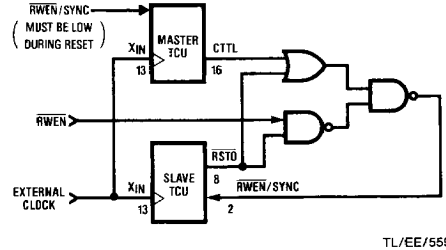

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FIGURE 1-4b. Slave TCU Uses Both SYNC and $\overline{\text{RWEN}}$

Note: When two or more TCUs are to be synchronized, the XIN of all the TCUs should be connected to an external clock source. For details on the external clock, see Switching Characteristics in Section 2.

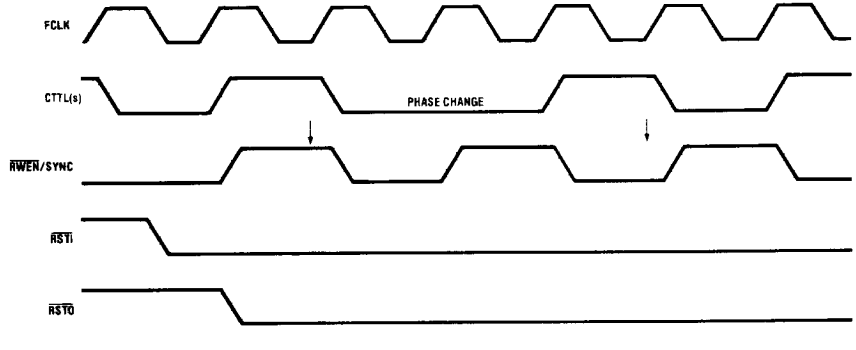

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FIGURE 1-5. Synchronizing Two TCUs

1.0 Functional Description (Continued)

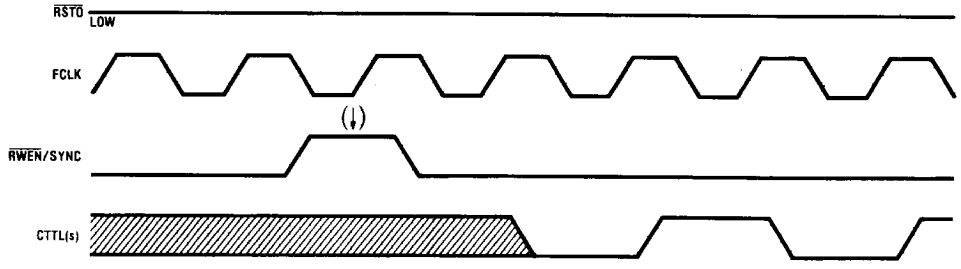

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FIGURE 1-6. Synchronizing one TCU to an External Pulse

In addition to synchronizing two or more TCUs, the RWEN/SYNC input can be used to "fix" the phase of one TCU to an external pulse. The pulse to be used must be high for only one rising edge of FCLK. Independent of CTTL's state at the FCLK rising edge, its state following the next FCLK rising edge should be low. *Figure 1-6* shows the timing of this sequence.

1.6 BUS CYCLES

In addition to providing all the necessary clock signals, the NS32201 TCU provides bus control signals to the system. The TCU senses the ADS signal from the CPU or MMU to start a bus cycle. The DDIN input signal is also sampled to determine whether a Read or Write cycle is to be generated. In addition to RD and WR, other signals are provided: DBE and TSO. DBE is used to enable data buffers. The leading edge of DBE is delayed a half clock period during Read cycles to avoid bus conflicts between data buffers and either the CPU or the MMU. This is shown in *Figure 1-7*.

The Timing State Output (TSO) is a general purpose signal that may be used by external logic for synchronizing to a System cycle. TSO is activated at the beginning of state T2 and returns to the high level at the beginning of state T4 of the CPU cycle. TSO can be used to gate the CWAIT signal when continuous waits are required. Another application of TSO is the control of interface circuitry for dynamic RAMs.

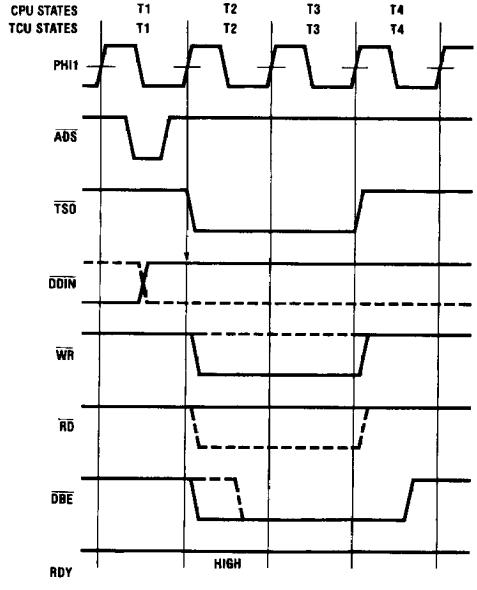

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FIGURE 1-7. Basic TCU Cycle (Fast Cycle)

Notes:

1. The CPU and TCU view some timing states (T-states) differently. For clarity, references to T-states will sometimes be followed by (TCU) or (CPU). (CPU) also implies (MMU).
2. Arrows indicate when the TCU samples the input.
3. RWEN is assumed low (RD and WR enabled) unless specified differently.
4. For clarity, T-states for both the TCU and CPU are shown above the diagrams. (See Note 1.)

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1.0 Functional Description (Continued)

1.7 BUS CYCLE EXTENSION

The NS32201 TCU uses the Wait input signals to extend normal bus cycles. A normal bus cycle consists of four PHI1 clock cycles. Whenever one or more Wait inputs to the TCU are activated, a bus cycle is extended by at least one PHI1 clock cycle. The purpose is to allow the CPU to access slow memories or peripherals. The TCU responds to the Wait signals by pulling the RDY signal low as long as Wait States are to be inserted in the Bus cycle.

There are three basic cycle extension modes provided by the TCU, as described below.

1.7.1 Normal Wait States

This is a normal Wait State insertion mode. It is initiated by pulling $\overline{\text{CWAIT}}$ or any of the $\overline{\text{WAITn}}$ lines low in the middle of T2. *Figure 1-8* shows the timing diagram of a bus cycle when $\overline{\text{CWAIT}}$ is sampled high at the end of T1 and low in the middle of T2.

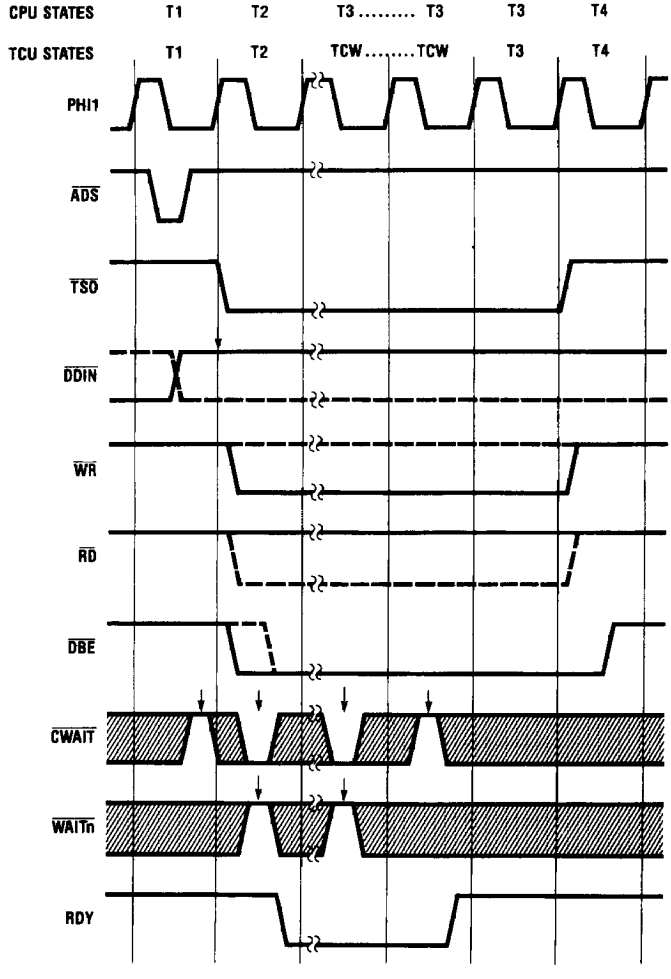

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FIGURE 1-8. Wait State Insertion Using $\overline{\text{CWAIT}}$ (Fast Cycle)

1.0 Functional Description (Continued)

The RDY signal goes low during T2 and remains low until $\overline{CWAIT}$ is sampled high by the TCU. RDY is pulled high by the TCU during the same PHI1 cycle in which the $\overline{CWAIT}$ line is sampled high.

If any of the $\overline{WAITn}$ signals are sampled low during T2 and $\overline{CWAIT}$ is high during the entire bus cycle, then the RDY line goes low for 1 to 15 clock cycles, depending on the binary weighted value of $\overline{WAITn}$. If, for example, $\overline{WAIT1}$ and $\overline{WAIT4}$ are sampled low, then five wait states will be inserted. This is shown in *Figure 1-9*.

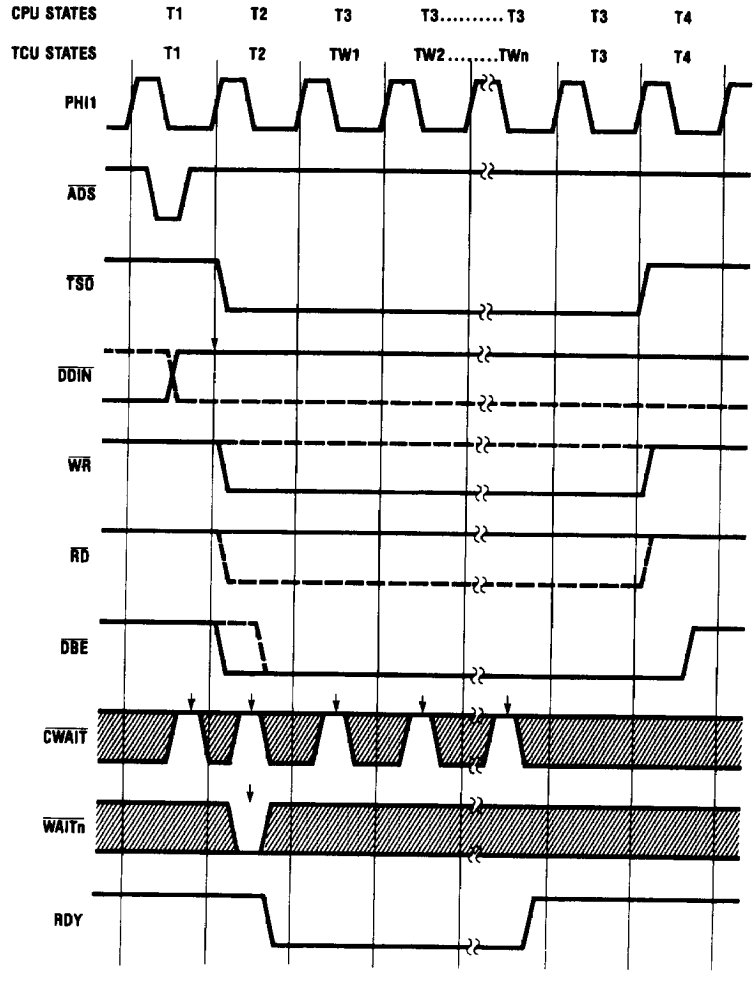

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FIGURE 1-9. Wait State Insertion Using $\overline{WAITn}$ (Fast Cycle)

1.0 Functional Description (Continued)

1.7.2 Peripheral Cycle

This cycle is entered when the $\overline{PER}$ signal line is sampled low at the beginning of T2. The TCU adds five wait states identified as TD0-TD4 into a normal bus cycle. The $\overline{RD}$ and $\overline{WR}$ signals are also re-shaped so the setup and hold times for address and data will be increased.

This may be necessary when slower peripherals must be accessed.

Figure 1-10 shows the timing diagram of a peripheral cycle.

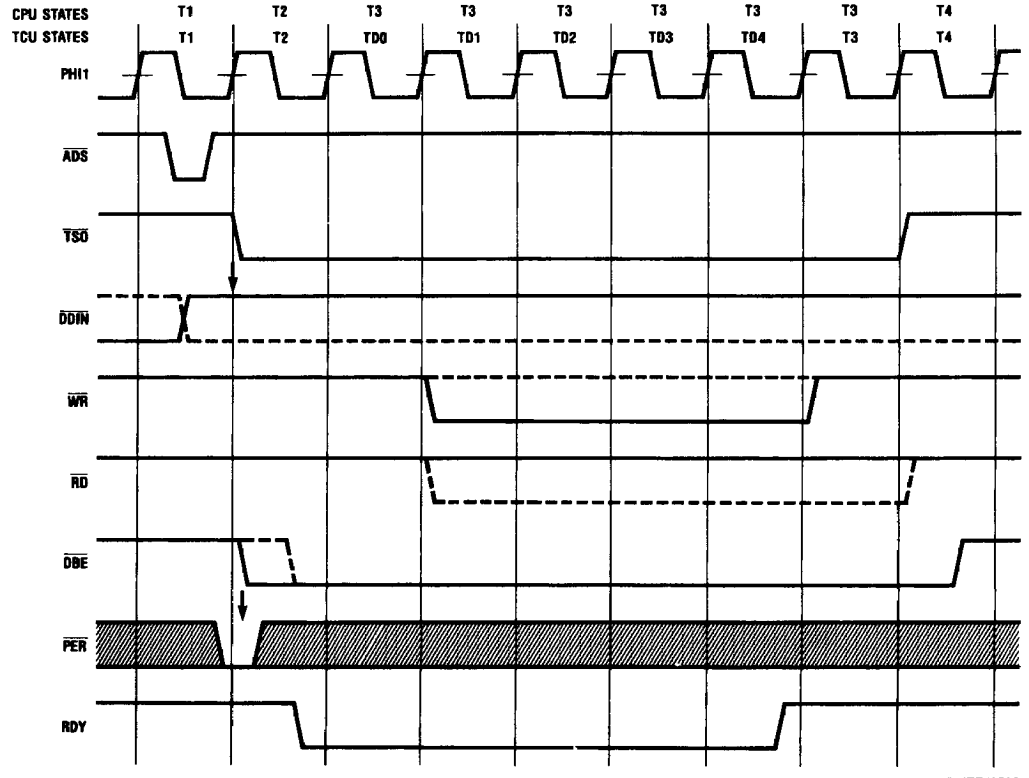

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FIGURE 1-10. Peripheral Cycle

1.0 Functional Description (Continued)

1.7.3 Cycle Hold

If the $\overline{CWAIT}$ input is sampled low at the end of state T1, the TCU will go into cycle hold mode and stay in this mode for as long as $\overline{CWAIT}$ is kept low. During this mode the control signals $\overline{RD}$, $\overline{WR}$, $\overline{TSO}$ and $\overline{DBE}$ are kept inactive; RDY is pulled low, thus causing wait states to be inserted into the bus cycle. The cycle hold feature can be used in applications involving dynamic RAMs. A timing diagram showing the cycle hold feature is shown in *Figure 1-11*.

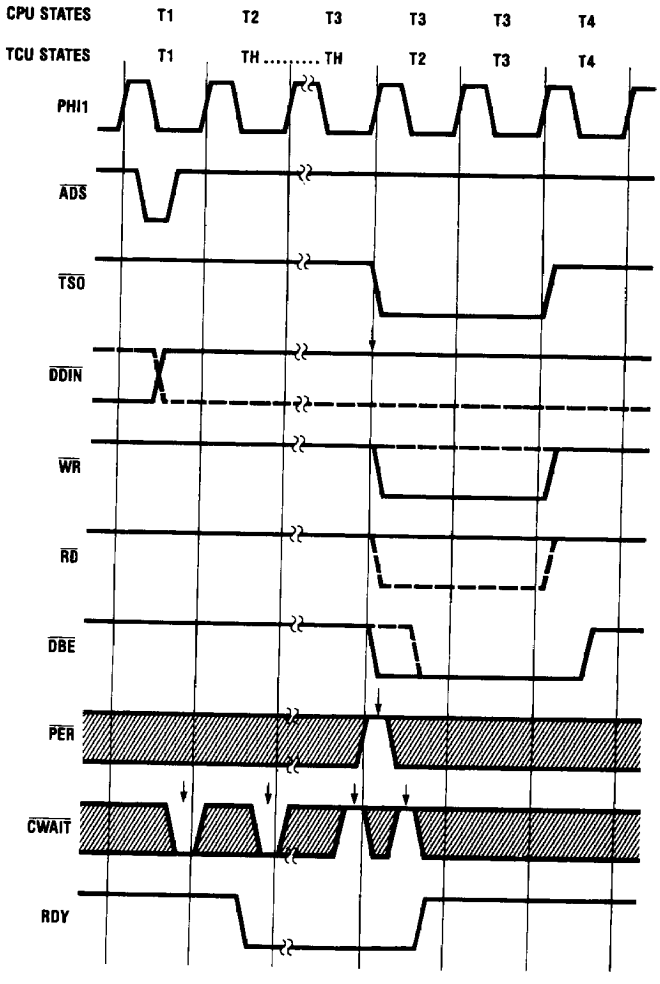

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FIGURE 1-11. Cycle Hold Timing Diagram

1.8 BUS CYCLE EXTENSION COMBINATIONS

Any combination of the TCU input signals used for extending a bus cycle can be activated at one time. The TCU will honor all of the requests according to a certain priority scheme. A cycle hold request is assigned top priority. It follows a peripheral cycle request, and then $\overline{CWAIT}$ and $\overline{WAITn}$ respectively.

If, for example, all the input signals $\overline{CWAIT}$, $\overline{PER}$ and $\overline{WAITn}$ are asserted at the beginning of the cycle, the TCU will enter the cycle hold mode. As soon as $\overline{CWAIT}$ goes high, the input signal $\overline{PER}$ is sampled to determine whether a peripheral cycle is requested.

Next, the TCU samples $\overline{CWAIT}$ again and $\overline{WAITn}$ to check whether additional wait states have to be inserted into the bus cycle. This sampling point depends on whether $\overline{PER}$ was sampled high or low. If $\overline{PER}$ was sampled high, then the sampling point will be in the middle of the TCU state T2, (*Figure 1-14*), otherwise it will occur three clock cycles later (*Figure 1-15*). *Figures 1-12* to *1-15* show the timing diagrams for different combinations of cycle extensions.

1.0 Functional Description (Continued)

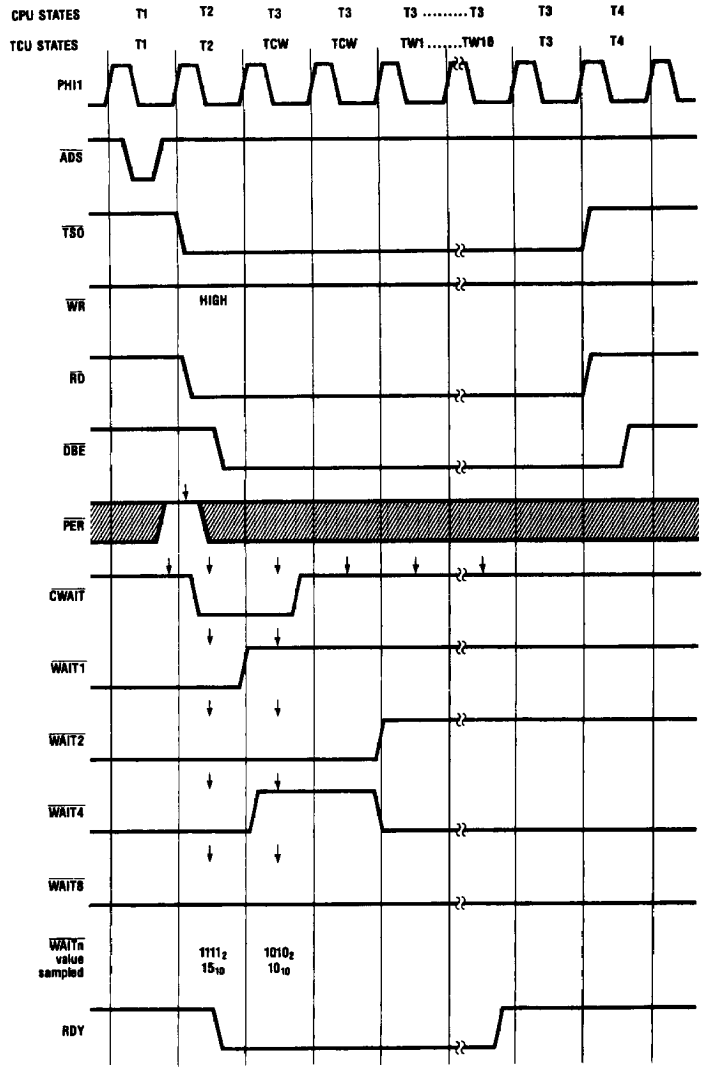

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FIGURE 1-12. Fast Cycle With 12 Wait States (2 CWAIT and WAIT10) (Read Cycle)

1.0 Functional Description (Continued)

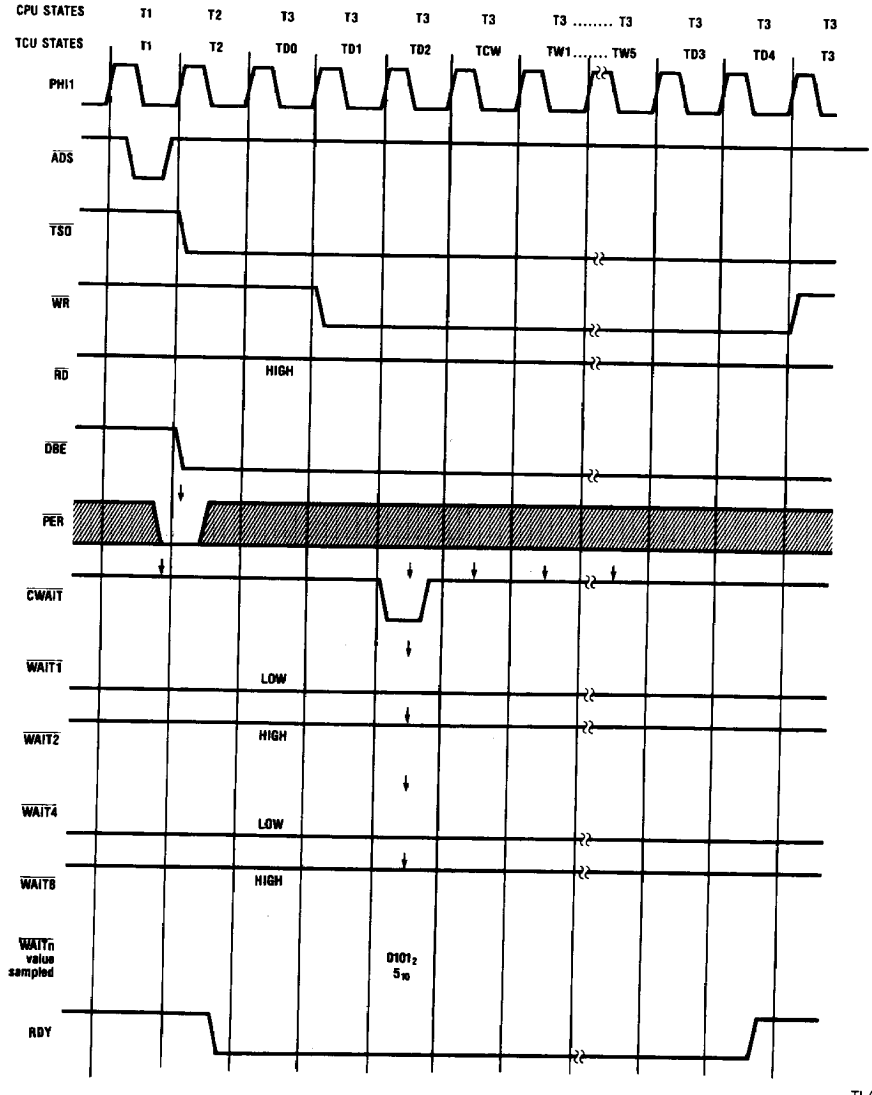

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FIGURE 1-13. Peripheral Cycle With Six Wait States (1 $\overline{\text{CWAIT}}$ and $\overline{\text{WAIT5}}$) (Write Cycle)

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1.0 Functional Description (Continued)

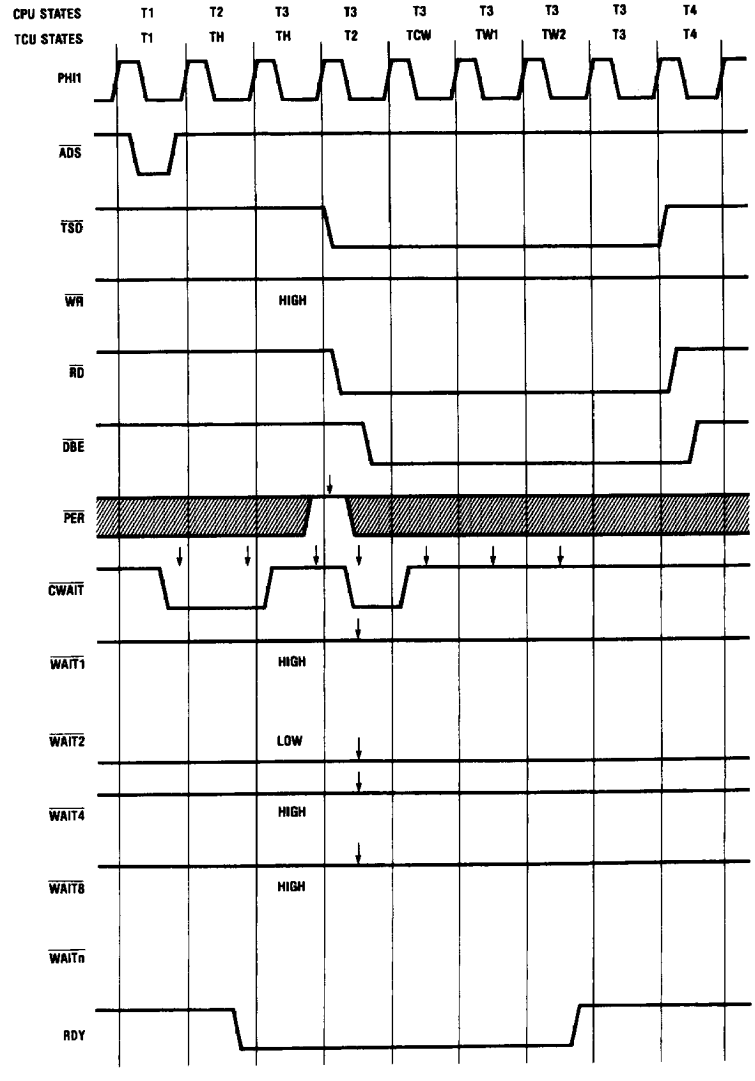

FIGURE 1-14. Cycle Hold With Three Wait States (1 $\overline{\text{CWAIT}}$ and $\overline{\text{WAIT2}}$) (Read Cycle)

1.0 Functional Description (Continued)

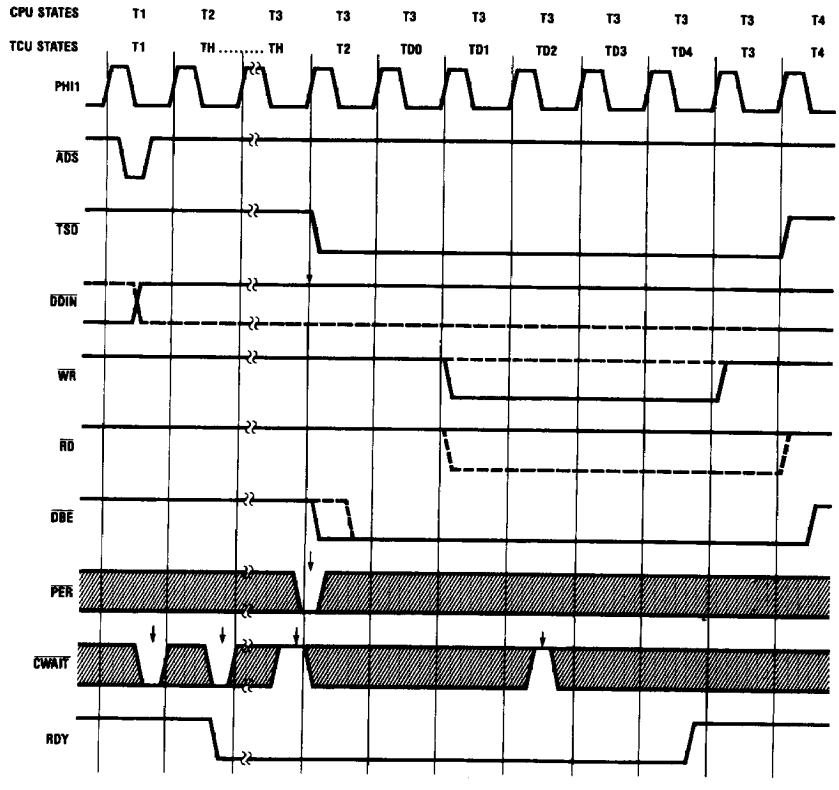

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FIGURE 1-15. Cycle Hold of a Peripheral Cycle

1.9 OVERRIDING $\overline{\text{WAITn}}$ Wait STATES

The TCU handles the $\overline{\text{WAITn}}$ Wait States by means of an internal counter that is reloaded with the binary value corresponding to the state of the $\overline{\text{WAITn}}$ inputs each time $\overline{\text{CWAIT}}$ is sampled low, and is decremented when $\overline{\text{CWAIT}}$ is high.

This allows to either extend a bus cycle of a predefined number of clock cycles, or prematurely terminate it. To terminate a bus cycle, for example, $\overline{\text{CWAIT}}$ must be asserted for at least one clock cycle, and the $\overline{\text{WAITn}}$ inputs must be forced to their inactive state.

At least one wait state is always inserted when using this procedure as a result of $\overline{\text{CWAIT}}$ being sampled low. *Figure 1-16* shows the timing diagram of a prematurely terminated bus cycle where eleven wait states were being inserted.

1.0 Functional Description (Continued)

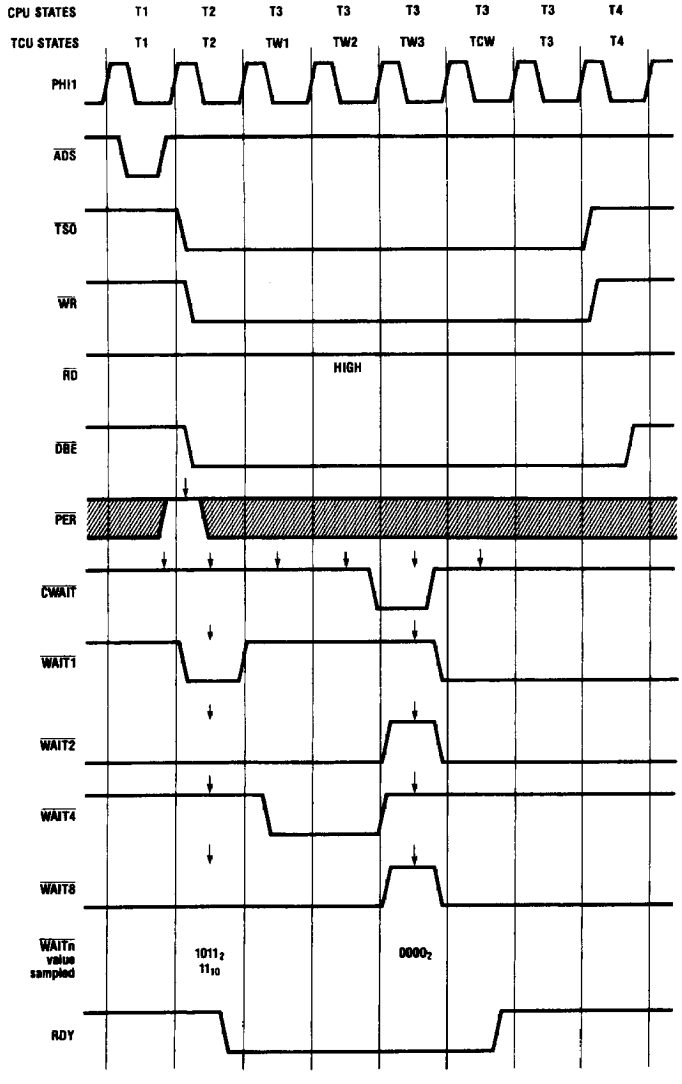


FIGURE 1-16. Overriding $\overline{\text{WAITn}}$ Wait States (Write Cycle)

2.0 Device Specifications

2.1 NS32201 PIN DESCRIPTIONS

The following is a description of all NS32201 pins. The descriptions reference portions of the Functional Description, Chapter 2.

2.1.1 SUPPLIES

Power (V_{CC}): +5V positive supply. Sec. 1.1.

Ground (GND): Power supply return. Sec. 1.1.

2.1.2 INPUT SIGNALS

Reset Input ($\overline{RSTI}$): Active low. Schmitt triggered, asynchronous signal used to generate a system reset. Sec. 1.4.

Address Strobe ($\overline{ADS}$): Active low. Identifies the first timing state (T1) of a bus cycle.

Data Direction Input ($\overline{DDIN}$): Active low. Indicates the direction of the data transfer during a bus cycle. Implies a Read when low and a Write when high.

Read/Write Enable and Synchronization ($\overline{RWEN}$/SYNC): TRI-STATE® the $\overline{RD}$ and the $\overline{WR}$ outputs when high and enables them when low. Also used to synchronize the phase of the TCU clock signals, when two or more TCUs are used. Sec. 1.5.

Crystal or External Clock Source (XIN): Input from a crystal or an external clock source. Sec. 1.3.

Continuous Wait ($\overline{CWAIT}$): Active low. Initiates a continuous wait if sampled low in the middle of T2 during a fast cycle, or in the middle of TD2 during a peripheral cycle. If $\overline{CWAIT}$ is low at the end of T1, it initiates a Cycle Hold. Sec. 1.7.1.

Four-Bit Wait State Inputs ($\overline{WAIT1}$, $\overline{WAIT2}$, $\overline{WAIT4}$ and $\overline{WAIT8}$): Active low. These inputs, (collectively called $\overline{WAITn}$), allow from zero to fifteen wait states to be specified. They are binary weighted. Sec. 1.7.1.

Peripheral Cycle ($\overline{PER}$): Active low. If active, causes the TCU to insert five wait states into a normal bus cycle. It also causes the Read and Write signals to be re-shaped to meet the setup and hold timing requirement of slower MOS peripherals. Sec. 1.7.2.

2.1.3 OUTPUT SIGNALS

Reset Output ($\overline{RSTO}$): Active low. This signal becomes active when $\overline{RSTI}$ is low, initiating a system reset. $\overline{RSTO}$ goes high on the first rising edge of PHI1 after $\overline{RSTI}$ goes high. Sec. 1.4.

Read Strobe ($\overline{RD}$): (TRI-STATE) Active low. Identifies a Read cycle. It is decoded from $\overline{DDIN}$ and TRI-STATE by $\overline{RWEN}$/SYNC. Sec. 1.6.

Write Strobe ($\overline{WR}$): (TRI-STATE) Active low. Identifies a Write cycle. It is decoded from $\overline{DDIN}$ and TRI-STATE by $\overline{RWEN}$/SYNC. Sec. 1.6.

NOTE: $\overline{RD}$ and $\overline{WR}$ are mutually exclusive in any cycle. Hence they are never low at the same time.

Data Buffer Enable ($\overline{DBE}$): Active low. This signal is used to control the data bus buffers. It is low when the data buffers are to be enabled. Sec. 1.6.

Timing State Output ($\overline{TSO}$): Active low. The falling edge of $\overline{TSO}$ signals the beginning of state T2 of a bus cycle. The rising edge of $\overline{TSO}$ signals the beginning of state T4. Sec. 1.6.

Ready (RDY): Active high. This signal will go low and remain low as long as wait states are to be inserted in a bus cycle. It is normally connected to the RDY input of the CPU. Sec. 1.7.

Fast Clock (FCLK): This is a TTL level clock running at the same frequency as the crystal or the external source. Its frequency is twice that of the CPU clocks. Sec. 1.3.

CPU Clocks (PHI1 and PHI2): These outputs provide the Series 32000 CPU with two phase, non-overlapping clock signals. Their frequency is half that of the crystal or external source. Sec. 1.3.

TTL System Clock (CTTL): This is a TTL compatible version of the PHI1 clock. Hence, it operates at the CPU clock frequency. Sec. 1.3.

Crystal Output (XOUT): This line is used as the return path for the crystal (if used). It must be left open when an external clock source is used to drive XIN. Sec. 1.2.

2.0 Device Specifications (Continued)

2.2 ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	7V
Input Voltages	−1 to +5.5V
Output Voltages	−1 to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Continuous Power Dissipation at 25°C Free-Air (Note 1)	
Cavity Package	3030 mW
Molded Package	2840 mW

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended, operation should be limited to those conditions specified under Electrial Characteristics.*

2.3 ELECTRICAL CHARACTERISTICS T_A = 0° to +70°C, V_{CC} = 5V ±5%, GND = 0V

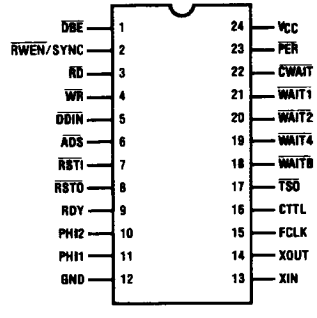
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	All Inputs Except $\overline{RSTI}$ & XIN			0.8	V
V_{IH}	Input High Voltage	All Inputs Except $\overline{RSTI}$ & XIN	2			V
V_{T+}	$\overline{RSTI}$ Rising Threshold Voltage		0.50 V_{CC}	0.60 V_{CC}	0.70 V_{CC}	V
V_{HYS}	$\overline{RSTI}$ Hysteresis Voltage		0.10 V_{CC}	0.20 V_{CC}	0.25 V_{CC}	V
V_{IX}	XIN Input Threshold Voltage		0.40 V_{CC}	0.5 V_{CC}	0.60 V_{CC}	V
I_{IX}	XIN Input Load Current	0.5V ≤ V_{IN} ≤ 4.5V			±500	μA
I_{IL}	Input Low Current	V_{IN} = 0.5V Except XIN			−500	μA
I_{IH}	Input High Current	V_{IN} = 5.25V Except XIN			50	μA
V_{OL}	Output Low Voltage	PHI1 & PHI2 I = 1 mA	−0.5		0.3	V
		All Other Outputs Except XOUT I = 20 mA			0.5	
V_{OH}	Output High Voltage	PHI1 & PHI2 I = −1 mA	V_{CC} − 0.3			V
		All Other Outputs Except XOUT I = −1 mA	2.4			
$I_{O(off)}$	Output Leakage Current On $\overline{RD}$ and $\overline{WR}$	0.4V ≤ V_{OUT} ≤ V_{CC}			±50	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −18 mA Except XIN		−0.7	−1.2	V
I_{CC}	Supply Current	fXIN = 20 MHz		180	260	mA

Note 1: For operation over 25°C free-air temperature, for cavity package, derate linearly to 2121 mW at 70°C at the rate of 20.2 mW/°C, and for molded package, derate linearly to 1818 mW at 70°C at the rate of 22.7 mW/°C.

Note 2: All typical values are for V_{CC} = 5V and T_A = 25°C.

Connection Diagram

Dual-In-Line Package



Top View

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FIGURE 2-1

Order Number NS32201D or NS32201N
See NS Package Number D24C or N24A

2.0 Device Specifications (Continued)

2.4 SWITCHING CHARACTERISTICS

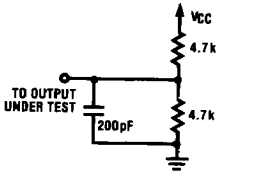
2.4.1 Definitions

All the timing specifications given in this section refer to 2.0V on the rising or falling edges of the clock phases PHI1 or PHI2, and to 0.8V or 2.0V on all TTL compatible signals, unless specifically stated otherwise.

ABBREVIATIONS

L.E.—Leading Edge
T.E.—Trailing Edge
R.E.—Rising Edge
F.E.—Falling Edge

2.4.2 Output Load Circuits (Notes 1, 2, 3)



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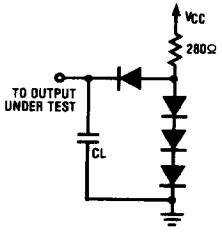
LOAD 1



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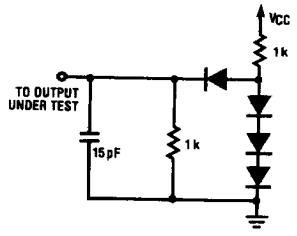
LOAD 2



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LOAD 3

Note 1: Unless otherwise specified, the timing measurements are taken with the output pins in the following conditions.

Load 1 PHI1 and PHI2

Load 2 CL = 50 pF all TTL outputs

CL = 100 pF only CTTL

Load 3 $\overline{RD}$ and $\overline{WR}$ for TRI-STATE measurements only.

Note 2: Load Capacitance includes probe and jig capacitance.

Note 3: All diodes are 1N914 or equivalent.

2.4.3 Timing Tables

Name	Figure	Description	Reference/Conditions	NS32201-6		NS32201-8		NS32201-10		Units
				Min	Max	Min	Max	Min	Max	
CLOCK-SIGNALS (XIN, FCLK, PHI1 & PHI2) TIMING (Note 3)										
t_{Cp}	2.2	Clock Period	PHI1 R.E. to Next PHI1 R.E.	160		120		100		ns
t_{CLh}	2.2	Clock High Time	At V_{CC} −0.9V on PHI1, PHI2 (Both Edges)	0.5 t_{Cp} −17 ns	0.5 t_{Cp} −7 ns	0.5 t_{Cp} −16 ns	0.5 t_{Cp} −7 ns	0.5 t_{Cp} −15 ns	0.5 t_{Cp} −7 ns	
t_{CLl}	2.2	Clock Low Time	At 0.8V on PHI1, PHI2 (Both Edges)	0.5 t_{Cp}	0.5 t_{Cp} +12 ns	0.5 t_{Cp}	0.5 t_{Cp} +11 ns	0.5 t_{Cp}	0.5t_{CP} +10 ns	
$t_{CLw(1,2)}$	2.2	Clock Pulse Width	At 2.0V on PHI1, PHI2 (Both Edges)	0.5 t_{Cp} −14 ns	0.5 t_{Cp} −4 ns	0.5 t_{Cp} −12 ns	0.5 t_{Cp} −4 ns	0.5 t_{Cp} −10 ns	0.5 t_{Cp} −4 ns	
t_{CLwas}		PHI1, PHI2 Asymmetry (t_{CLW1} - $t_{CLW(2)}$)	At 2.0V on PHI1, PHI2	−5	5	−5	5	−5	5	ns
t_{CLR}	2.2	Clock Rise Time	0.8V to V_{CC} −0.9V on PHI1, PHI2 R.E.		9		8		7	ns
t_{CLF}	2.2	Clock Fall Time	V_{CC} −0.9V to 0.8V on PHI1, PHI2 F.E.		7		7		7	ns
$t_{nOVL(1,2)}$	2.2	Clock Nonoverlap Time	0.8V on PHI1, PHI2 F.E. to 0.8V on PHI2, PHI1 R.E.	0	5	0	5	0	5	ns
t_{nOVLas}		Non-Overlap Asymmetry ($t_{nOVL(1)}$ - $t_{nOVL(2)}$)	At 0.8V on PHI1, PHI2	−4	4	−4	4	−4	4	ns
t_{XIR}	2.3	XIN Rise Time	1.5V to V_{CC} −1.5V on XIN R.E.		15		11		9	ns
t_{XIF}	2.3	XIN Fall Time	V_{CC} −1.5V to 1.5V on XIN F.E.		15		11		9	ns
t_{Xh}	2.2	XIN High Time (External Input)	2.5V on XIN R.E. to 2.5V on XIN F.E.	25		20		16		ns

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2.0 Device Specifications (Continued)

2.4 SWITCHING CHARACTERISTICS (Continued)

2.4.3 Timing Tables

Name	Figure	Description	Reference/Conditions	NS32201-6		NS32201-8		NS32201-10		Units
				Min	Max	Min	Max	Min	Max	
t_{XI}	2.2	XIN Low Time (External Input)	2.5V on XIN F.E. to 2.5V on XIN R.E.	25		20		16		ns
t_{XFr}	2.2	XIN to FCLK R.E. Delay	2.5V on XIN R.E. to FCLK R.E.	15	29	15	28	15	27	ns
t_{XFf}	2.2	XIN to FCLK F.E. Delay	2.5V on XIN F.E. to FCLK F.E.	15	29	15	28	15	27	ns
t_{XCr}	2.2	XIN to CTTL R.E. Delay	2.5V on XIN R.E. to CTTL R.E.	24	40	24	39	24	35	ns
t_{XPr}	2.2	XIN to PHI1 R.E. Delay	2.5V on XIN R.E. to PHI1 R.E.	21	40	21	37	21	32	ns
t_{FCR}	2.3	FCLK Rise Time	0.8V to 2.0V on FCLK R.E.		12		9		7	ns
t_{FCF}	2.3	FCLK Fall Time	2.0V to 0.8V on FCLK F.E.		12		9		7	ns
t_{FCr}	2.2	FCLK to CTTL R.E. Delay	FCLK R.E. to CTTL R.E.	5	17	5	16	5	15	ns
t_{FCf}	2.2	FCLK to CTTL F.E. Delay	FCLK R.E. to CTTL F.E.	5	17	5	16	5	15	ns
t_{FPr}	2.3	FCLK to PHI1 R.E. Delay	FCLK R.E. to PHI1 R.E.	2	17	2	13	2	10	ns
t_{FPf}	2.3	FCLK to PHI1 F.E. Delay	FCLK R.E. to PHI1 F.E.	−4	8	−4	6	−4	4	ns
t_{Fw}	2.3	FCLK High Time with Crystal	At 2.0V on FCLK (Both Edges)	0.25 t_{Cp} −7 ns	0.25 t_{Cp} +7 ns	0.25 t_{Cp} −6 ns	0.25 t_{Cp} +6 ns	0.25 t_{Cp} −5 ns	0.25 t_{Cp} +5 ns	
t_{PCf}	2.3	PHI2 R.E.to CTTL F.E. Delay	PHI2 R.E. to CTTL F.E.	−8	12	−7	11	−6	10	ns
t_{CTw}	2.3	CTTL High Time	At 2.0V on CTTL (Both Edges)	0.5 t_{Cp} −8 ns	0.5 t_{Cp} +8 ns	0.5 t_{Cp} −8 ns	0.5 t_{Cp} +8 ns	0.5 t_{Cp} −7 ns	0.5 t_{Cp} +7 ns	
CTTL TIMING (CL = 50 pF)										
t_{PCr}	2.4	PHI1 to CTTL R.E. Delay	PHI1 R.E. to CTTL R.E.	−2	7	−2	6	−2	5	ns
t_{CTR}	2.3	CTTL Rise Time	0.8V to 2.0V on CTTL R.E.		6		6		5	ns
t_{CTF}	2.3	CTTL Fall Time	2.0V to 0.8V on CTTL F.E.		5		5		4	ns

Note 1: PHI1 and PHI2 are interchangeable for the following parameters: t_{Cp}, t_{CLh}, t_{CLl}, t_{CLw}, t_{CLR}, t_{CLF}, t_{nOVL}, t_{XPr}, t_{FPr}, t_{FPf}.

2.0 Device Specifications (Continued)

2.4.3 Timing Tables (Continued)

Name	Figure	Description	Reference/Conditions	NS32201-6		NS32201-8		NS32201-10		Units
				Min	Max	Min	Max	Min	Max	
CTTL TIMING (CL = 100 pF)										
t_{PCr}	2.3	PHI1 to CTTL R.E. Delay	PHI1 R.E. to CTTL R.E.	−2	8	−2	7	−2	6	ns
t_{CTR}	2.3	CTTL Rise Time	0.8V to 2.0V on CTTL R.E.		8		8		7	ns
t_{CTF}	2.2	CTTL Fall Time	2.0V to 0.8V on CTTL F.E.		6		6		5	ns
CONTROL INPUTS ($\overline{RST1}$, $\overline{RSTO}$, $\overline{ADS}$, $\overline{DDIN}$) TIMING										
t_{RSTr}	2.4	$\overline{RSTO}$ R.E. Delay	After PHI1 R.E.		25		20		15	ns
t_{RSTs}	2.4	$\overline{RSTI}$ Setup Time	Before PHI1 R.E.	20		20		20		ns
t_{ADs}	2.4	$\overline{ADS}$ Setup Time	Before PHI1 R.E.	30		28		25		ns
t_{ADw}	2.4	$\overline{ADS}$ Pulse Width	$\overline{ADS}$ L.E. to $\overline{ADS}$ T.E.	25		25		25		ns
t_{DDs}	2.4	$\overline{DDIN}$ Setup Time	Before PHI1 R.E.	10		10		10		ns
t_{DDh}	2.4	$\overline{DDIN}$ Hold Time	After PHI1 R.E.	15		15		15		ns
CONTROL OUTPUTS ($\overline{TSD}$, $\overline{RD}$, $\overline{WR}$, $\overline{DBE}$ & $\overline{RWEN}$/SYNC) TIMING										
t_{Tf}	2.5	$\overline{TSO}$ L.E. Delay	After PHI1 R.E.		12		11		10	ns
t_{Tr}	2.5	$\overline{TSO}$ T.E. Delay	After PHI1 R.E.		20		18		15	ns
$t_{RWf(F)}$	2.5	$\overline{RD}$/$\overline{WR}$ L.E. Delay (Fast Cycle)	After PHI1 R.E.		50		40		30	ns
$t_{RWf(S)}$	2.6	$\overline{RD}$/$\overline{WR}$ L.E. Delay (Peripheral Cycle)	After PHI1 R.E.		30		23		15	ns
t_{RWr}	2.5/6	$\overline{RD}$/$\overline{WR}$ T.E. Delay	After PHI1 R.E.		25		23		20	ns
$t_{DBf(W)}$	2.5/6	$\overline{DBE}$ L.E. Delay (Write Cycle)	After PHI1 R.E.		35		30		24	ns
$t_{DBf(R)}$	2.5/6	$\overline{DBE}$ L.E. Delay (Read Cycle)	After PHI2 R.E.		30		23		15	ns
t_{DBr}	2.5/6	$\overline{DBE}$ T.E. Delay	After PHI2 R.E.		20		20		20	ns
t_{pLZ}	2.7	$\overline{RD}$,$\overline{WR}$ Low Level to TRI-STATE	After $\overline{RWEN}$/SYNC R.E.		20		20		20	ns
t_{pHZ}	2.7	$\overline{RD}$,$\overline{WR}$ High Level to TRI-STATE	After $\overline{RWEN}$/SYNC R.E.		20		20		20	ns
t_{pZL}	2.7	$\overline{RD}$,$\overline{WR}$ TRI-STATE to Low Level	After $\overline{RWEN}$/SYNC F.E.		25		23		20	ns
t_{pZH}	2.7	$\overline{RD}$,$\overline{WR}$ TRI-STATE to High Level	After $\overline{RWEN}$/SYNC F.E.		25		23		20	ns
WAIT STATES & CYCLE HOLD ($\overline{CWAIT}$, $\overline{WAIT}$n, $\overline{PER}$ & $\overline{RDY}$) TIMING										
$t_{CWs(H)}$	2.8	$\overline{CWAIT}$ Setup Time (Cycle Hold)	Before PHI1 R.E.	35		30		25		ns
$t_{CWh(H)}$	2.8	$\overline{CWAIT}$ Hold Time (Cycle Hold)	After PHI1 R.E.	0		0		0		ns
$t_{CWs(W)}$	2.8/9	$\overline{CWAIT}$ Setup Time (Wait States)	Before PHI2 R.E.	13		12		10		ns
$t_{CWh(W)}$	2.9	$\overline{CWAIT}$ Hold Time (Wait States)	After PHI2 R.E.	20		14		8		ns
t_{Ws}	2.9	$\overline{WAIT}$n Setup Time	Before PHI2 R.E.	5		5		5		ns
t_{Wh}	2.9	$\overline{WAIT}$n Hold Time	After PHI2 R.E.	25		20		15		ns
t_{Ps}	2.10	$\overline{PER}$ Setup Time	Before PHI1 R.E.	0		0		0		ns
t_{Ph}	2.10	$\overline{PER}$ Hold Time	After PHI1 R.E.	30		25		20		ns
t_{Rd}	2.8/9/10	$\overline{RDY}$ Delay	After PHI2 R.E.		30		26		23	ns
SYNCHRONIZATION (SYNC) TIMING										
t_{Sys}	2.11	SYNC Setup Time	Before FCLK R.E.	20		19		18		ns
t_{Syh}	2.11	SYNC Hold Time	After FCLK R.E.	3		2		0		ns
t_{CS}	2.11	CTTL/SYNC Inversion Delay	CTTL (master) to $\overline{RWEN}$/SYNC (slave)		25		20		15	ns

2.0 Device Specifications (Continued)

2.4.4 Timing Diagrams

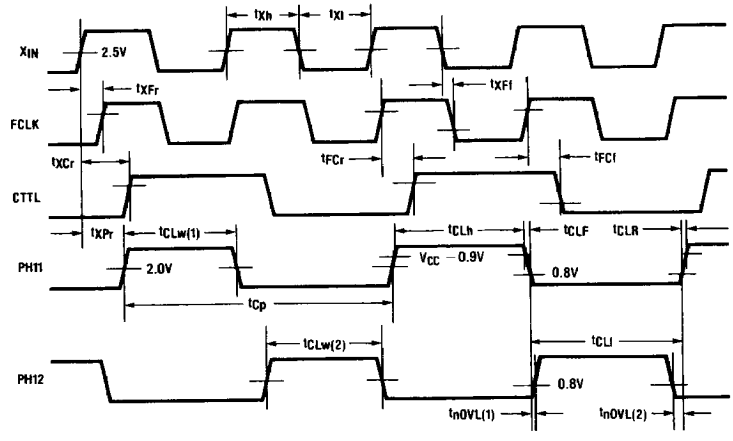

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FIGURE 2-2. Clock Signals (a)

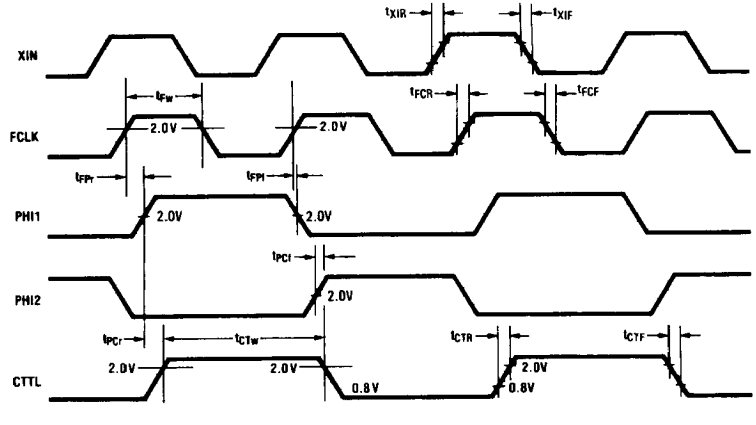

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FIGURE 2-3. Clock Signals (b)

2.0 Device Specifications (Continued)

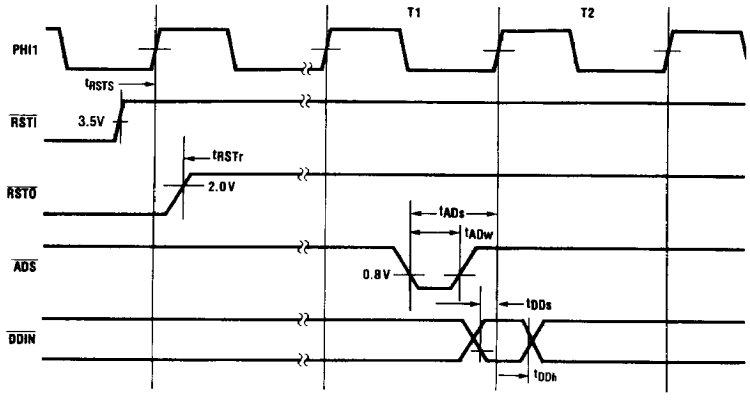

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FIGURE 2-4. Control Inputs

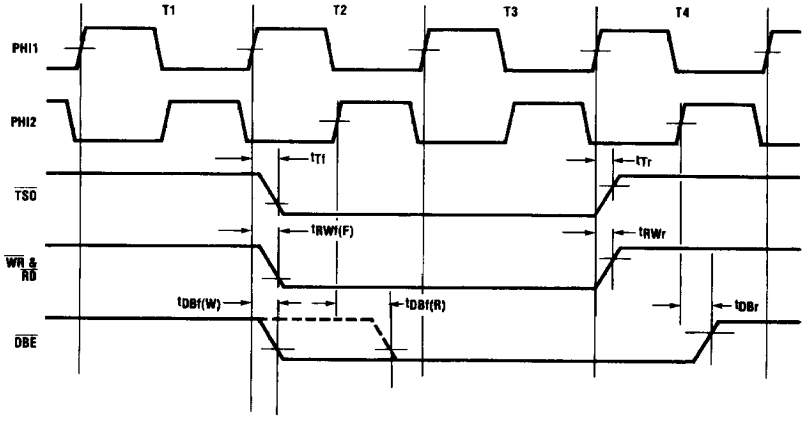

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FIGURE 2-5. Control Outputs (Fast Cycle)

4

2.0 Device Specifications (Continued)

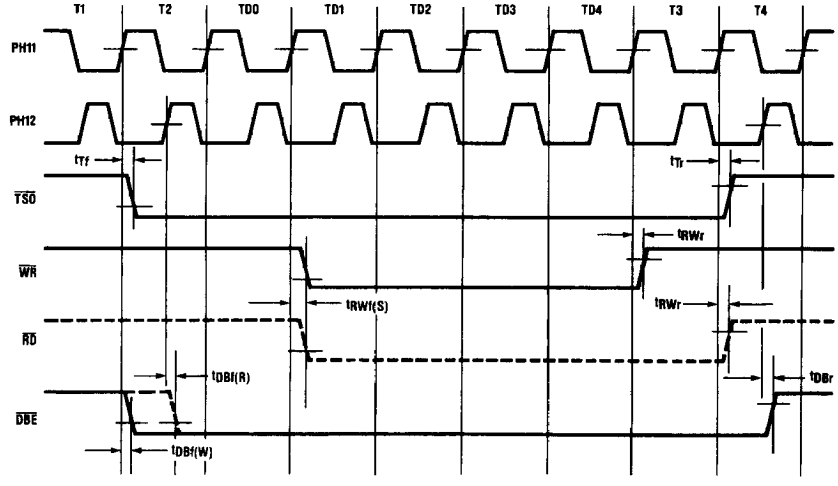

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FIGURE 2-6. Control Outputs (Peripheral Cycle)

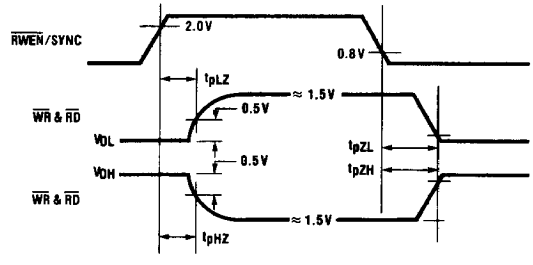

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FIGURE 2-7. Control Outputs (TRI-STATE Timing)

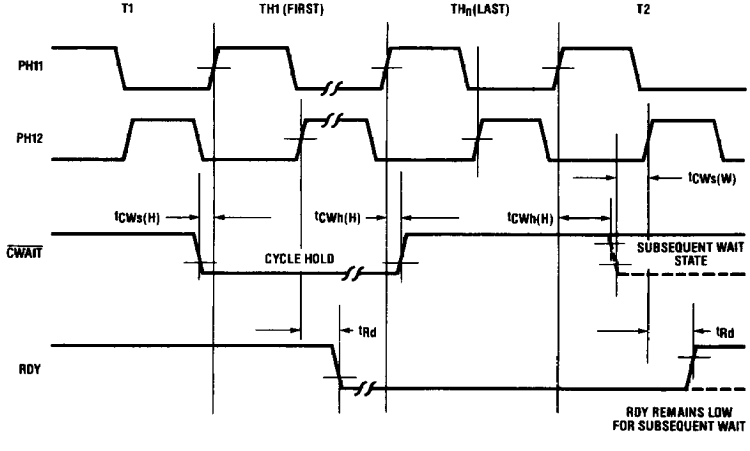

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FIGURE 2-8. Cycle Hold

2.0 Device Specifications (Continued)

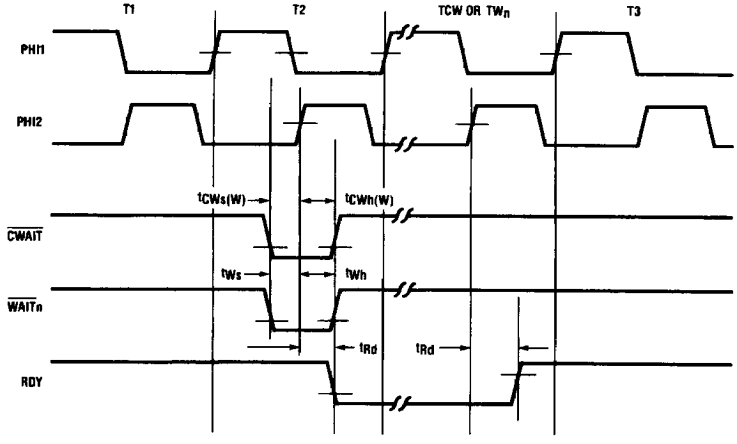

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FIGURE 2-9. Wait States (Fast Cycle)

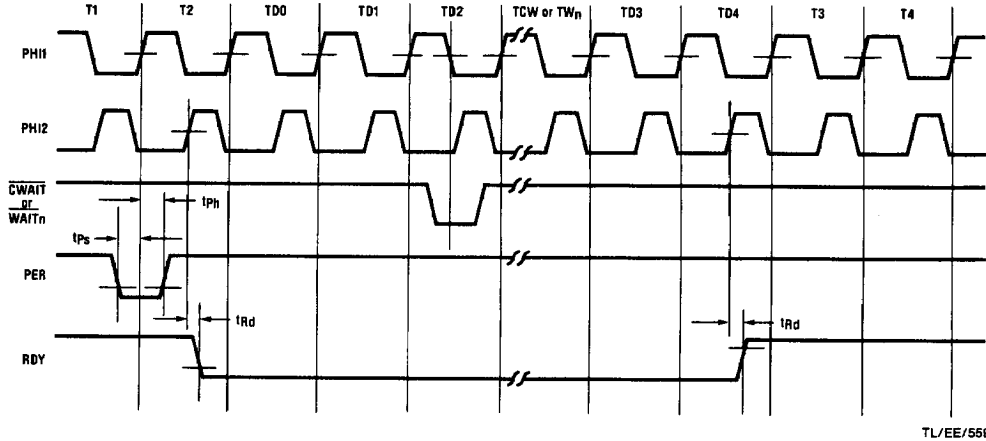

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FIGURE 2-10. Wait States (Peripheral Cycle)

2.0 Device Specifications (Continued)

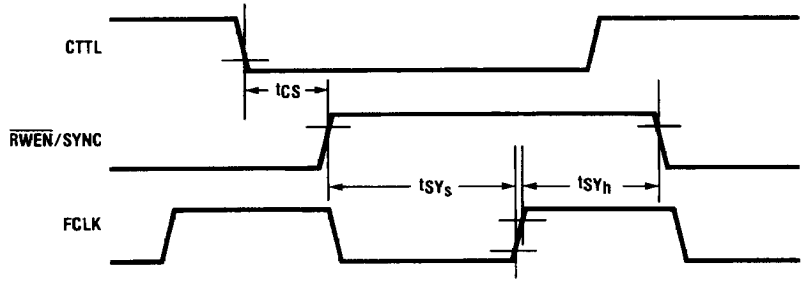

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FIGURE 2-11. Synchronization Timing