National Semiconductor

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NSBMC292™-16/-25/-33 Burst Memory Controller

General Description

The NSBMC292 Burst Memory Controller is an integrated circuit which implements all aspects of DRAM control for high performance systems using an Am29030™ or Am29035 Processor. The NSBMC292 is functionally equivalent to the V292BMC™.

The on-chip I-cache of these processors serves to partially decouple throughput from the performance of main memory, however, a sophisticated memory design is still required for optimum performance.

Static RAM offers a simple solution. Unfortunately, this solution is relatively expensive and space consumptive because of low bit density per device and high cost per bit.

From a cost and density point of view, Dynamic RAM is an attractive alternative. The drawbacks are relatively slow access times and the complexity of the control circuitry required to operate them.

The access time problem is solved if the DRAM is used in page mode. In this mode, access times rival that of static RAM. The control circuit problem is resolved by the NSBMC292.

The function that the NSBMC292 performs is to optimally translate the burst access protocol of the Am29030/35 to the page mode access protocol supported by dynamic RAMs.

One or two-way interleaved arrangements of DRAMs are supported. During burst access, data is accessed at the rate of one word per two cycles for non-interleaved, per cycle for two-way interleaved.

The NSBMC292 has been designed to allow maximum flexibility in its application. The full range of processor speeds is supported for a wide range of DRAM speeds, sizes and organizations.

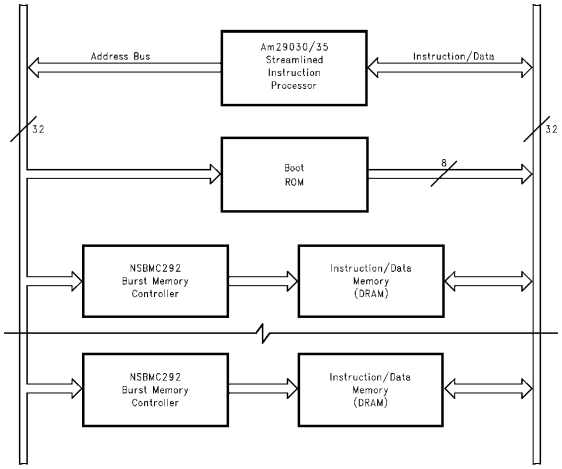
Because the bus interface is customized to the Am29030/35, no glue logic is required. Integration is further enhanced by providing on-chip, a 24-bit timer and a 5-bit bus time-out monitor.

The NSBMC292 is packaged as a 132-pin PQFP with a footprint of only 1.3 square inches. It reduces design complexity, space requirements and is fully derated for loading, temperature and voltage.

Features

- Interfaces directly to the Am29030/35
- Manages page mode dynamic memory devices
- Supports DRAMs from 256 kbits to 64 MB
- Non-interleaved or two way interleaved operation
- Software-configured operational parameters
- Integrated page cache management
- On-Chip memory address multiplexer/drivers
- 24-Bit counter/timer
- 5-Bit bus watch timer
- High-speed/low power CMOS technology

Block Diagram



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Typical System Configuration

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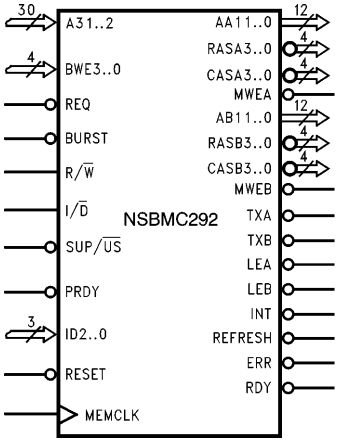
Logic and Connection Diagrams



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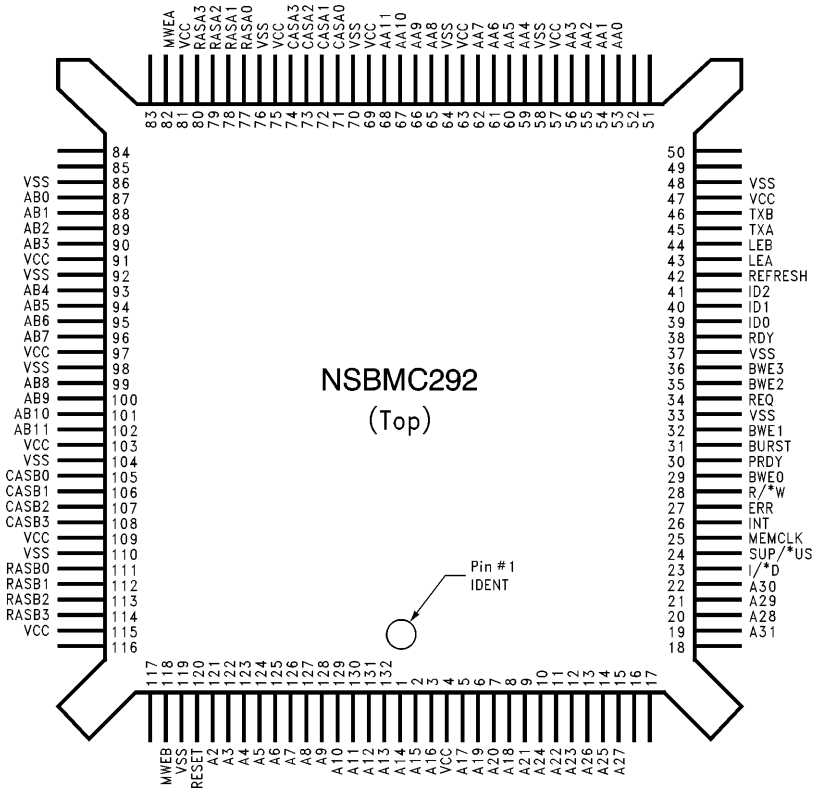

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Order Number NSBMC292VF
See Package Number VF132A

Pin Descriptions

TABLE I

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	A14	44	LEB	91	V_{CC}
2	A15	45	TXA	92	V_{SS}
3	A16	46	TXB	93	AB4
4	V_{CC}	47	V_{CC}	94	AB5
5	A17	48	V_{SS}	95	AB6
6	A19	53	AA0	96	AB7
7	A20	54	AA1	97	V_{CC}
8	A18	55	AA2	98	V_{SS}
9	A21	56	AA3	99	AB8
10	A24	57	V_{CC}	100	AB9
11	A22	58	V_{SS}	101	AB10
12	A23	59	AA4	102	AB11
13	A26	60	AA5	103	V_{CC}
14	A25	61	AA6	104	V_{SS}
15	A27	62	AA7	105	CASB0
19	A31	63	V_{CC}	106	CASB1
20	A28	64	V_{SS}	107	CASB2
21	A29	65	AA8	108	CASB3
22	A30	66	AA9	109	V_{CC}
23	I/D	67	AA10	110	V_{SS}
24	SUP/USR	68	AA11	111	RASB0
25	MEMCLK	69	V_{CC}	112	RASB1
26	INT	70	V_{SS}	113	RASB2
27	ERR	71	CASA0	114	RASB3
28	R/W	72	CASA1	115	V_{CC}
29	BWE0	73	CASA2	118	MWEB
30	PRDY	74	CASA3	119	V_{SS}
31	BURST	75	V_{CC}	120	RESET
32	BWE1	76	V_{SS}	121	A2
33	V_{SS}	77	RASA0	122	A3
34	REQ	78	RASA1	123	A4
35	BWE2	79	RASA2	124	A5
36	BWE3	80	RASA3	125	A6
37	V_{SS}	81	V_{CC}	126	A7
38	READY	82	MWEA	127	A8
39	ID0	86	V_{SS}	128	A9
40	ID1	87	AB0	129	A10
41	ID2	88	AB1	130	A11
42	REFRESH	89	AB2	131	A12
43	LEA	90	AB3	132	A13

Note: In order for the switching characteristics of this device to be guaranteed, it is necessary to connect **all** of the power pins (V_{CC}, V_{SS}) to the appropriate power levels. The use of low impedance wiring to the power pins is required. In systems using the Am29030 with its attendant high switching rates, multi-layer printed circuit boards with buried power and ground planes are required.

Pin Descriptions (Continued)

Am29030/35 INTERFACE

The following pins are functionally equivalent to those on the Am29030/35 from which their names are taken. Like named pins on the Am29030/35 and the NSBMC292 are to be wired together. All 3-State outputs are to be weakly pulled up to V_{CC}. A 10 kΩ resistor is sufficient.

Pin	Description
A2–31	**Address Bus (Input):** This system bus is a word address which determines the location at which an access is required.
REQ	**Address Strobe (Input; Active Low):** This input is used to indicate that a valid access cycle is in progress.
I/*D	**Data/*Code (Input):** This input qualifies an access as being for data (Low) or instruction (High).
BURST	**Burst Last (Input; Active Low):** Processor output that indicates that the data can be continuously transferred in a sequential burst.
PRDY	**Processor Ready (Input; Active Low):** The RDY signal directly at the processor is monitored by the Bus time-out monitor to detect an incomplete bus access. See Bus Monitor Control (p8).
RDY	**Data Ready (Output; 3-State; Active Low):** The RDY output is used to signal the processor that data on the Bus is valid (Read), or that data has been accepted for Write.
RESET	**Reset (Input; Active Low):** Assertion of this input sets the NSBMC292 to its initial state. Following initialization, the NSBMC292 must be configured before any memory access is possible.
BWE0–3	**Byte Write Enable (Input; Active Low):** These inputs are used to determine which byte(s) within the addressed word are to be written.
R/*W	**WRITE /*READ (Input):** This input indicates the direction which data is to be transferred to/from on the data bus.
SUP/*USR	**Supervisor (Input; Active Low):** Indicates that the processor is operating in supervisor mode. Required for access to configuration registers.
MEMCLK	**Memory System Clock (Input):** Processor output clock required to operate and synchronize NSBMC292 internal functions.
ERR	**Bus Error (Output; Active Low):** When enabled, this signal is generated by the Bus Monitor Circuit to prevent processor lock-up on access to a region that is not responding.
INT	**Interrupt (Output; 12 mA; Active Low):** This signal is asserted when the 24-bit counter reaches terminal count, and interrupt out is enabled. May be programmed for pulse or handshake operation.
ID0–2	**Chip ID (Input):** These inputs select the address offset of the NSBMC292 configuration registers. Each NSBMC292 in a system must have a unique address for proper operation.

Pin Descriptions (Continued)

MEMORY INTERFACE

The NSBMC292 is designed to drive a memory array organized as 2 leaves each of 32 bits. The address and control signals for the memory array are output through high current drivers in order to minimize propagation delay due to memory input impedance and trace capacitance. External array drivers are not required. The address and control signals, however, should be externally terminated.

Pin	Description
A(A,B)0–11	**Multiplexed Address Bus (Output; 24 mA):** These two buses transfer the multiplexed row and column addresses to the memory array leaves A and B. Note that when non-interleaved operation is selected, only address bus A should be used.
RAS(A,B)0–3	**Row Address Strobes (Output; 12 mA Active Low):** These strobes indicate the presence of a valid row address on busses A(A,B)0–11. These signals are to be connected one to each leaf of memory. Four banks of interleaved memory may be attached to a NSBMC292.
CAS(A,B)0–3	**Column Address Strobe (Output; 12 mA, Active Low):** These strobes latch a column address from A(A,B)0–11. They are assigned one to each byte in a leaf.
MWE(A,B)	**Memory Write Enable (Output; 24 mA, Active Low):** These are the write strobes for the DRAMs. One is supplied for each leaf to minimize signal loading.
REFRESH	**Refresh in progress (Output; 12 mA, Active Low):** This output gives notice that a refresh cycle is to be executed. The timing leads refresh RAS by one cycle.

BUFFER CONTROLS

Buffer control signals are provided to simplify the control of the interface between the DRAM and Am29030/35 data bus. Multiple operating modes facilitate choice of buffer type. Simple bus buffers (''245''s), bus latches (''543''s) and bus registers (''646''s) are all supported.

Pin	Description
TX(A,B)	**Data Bus Transmit A and B (Output; Active Low):** These outputs are multi-function signals. The signal names, as they appear on the logic symbol, are the default signal names (Mode = 0). The function of these outputs is to control buffers output enables during data read transactions and, in effect, control the multiplexing of data from each memory leaf onto the AM29030/35 data bus.
LE(A,B)	**Data Bus Latch Enable A and B (Output; Active Low):** The function of these outputs is mode independent although the timing of the signals change for different operational modes. These signals control transparent latches that hold data transmitted during a write transaction. In modes 0 and 1, the latch controls follow the timing of CAS for each leaf, while in modes 2 and 3 the timing of LEA and LEB is shortened to ½ clock.

Functional Description

OVERVIEW

The NSBMC292 couples the Am29030/35 interface to DRAM access protocols, generates bus buffer and data multiplexor controls and incorporates system and bus monitor timing resources. These functional elements are shown in *Figure 1*. A maximum of 8 controllers may be included in a system, each managing up to 4 banks of memory.

The NSBMC292 directly drives an array of fast page mode DRAMs. This array may be organized as 1 or 2 leaves of 32 bits each. Standard memory sizes from 256 kbit to 64 Mbit are supported and 8-, 16-, and 32-bit access are allowed. If interleaved mode is selected, burst access is zero-wait-state; if memory is non-interleaved, 1-wait-state burst access results.

The NSBMC292 allows for flexibility in the control of data buffers to the memory array. Propagation delay is minimized by providing these controls directly, and design flexibility maximized by allowing the control strategy to be programmable. Buffers as diverse as 74FCT245, 74FCT543, 74FCT646, 74FCT853 and 74FCT861 may be used without additional glue logic.

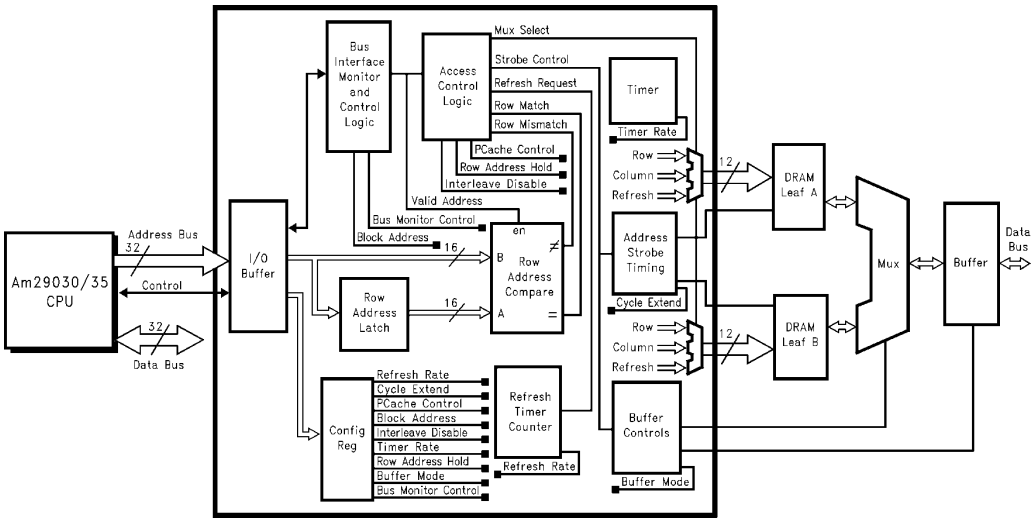

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FIGURE 1. Functional Block Diagram

Functional Description (Continued)

CONFIGURATION AND CONTROL

The NSBMC292 contains 64 bits of configuration data that controls it's operational mode. The configuration is programmed by sending data on the address bus. *Figure 2* shows the format of a configuration access. The byte select field determines which byte of the 64-bit field will be updated by the contents of the byte data field. Bits [1,0] are reserved and must be "0". The base address is fixed at 0x1f0f0000 while the BMC select field must match the value programmed at the ID[2..0] pins. In order to protect against accidental programming, the configuration registers can only be modified when the processor is in supervisor mode.

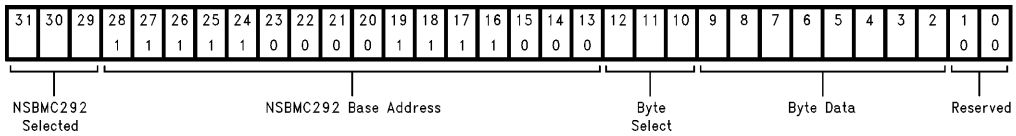

FIGURE 2. Address Bus Fields Used to Access Configuration Data

BLOCK ADDRESS FIELD

Once configured, a NSBMC292 responds to access requests within the programmed block address range. The programmed value sets the starting address of the block, while the size of the block is determined by the DRAM size control bits. The block address, however, is constrained to start on a boundary that is an integer multiple of the block size. For example, if 1 Mb x 1 DRAMs are used, the memory block size is 8 MB and must start on an 8 MB boundary.

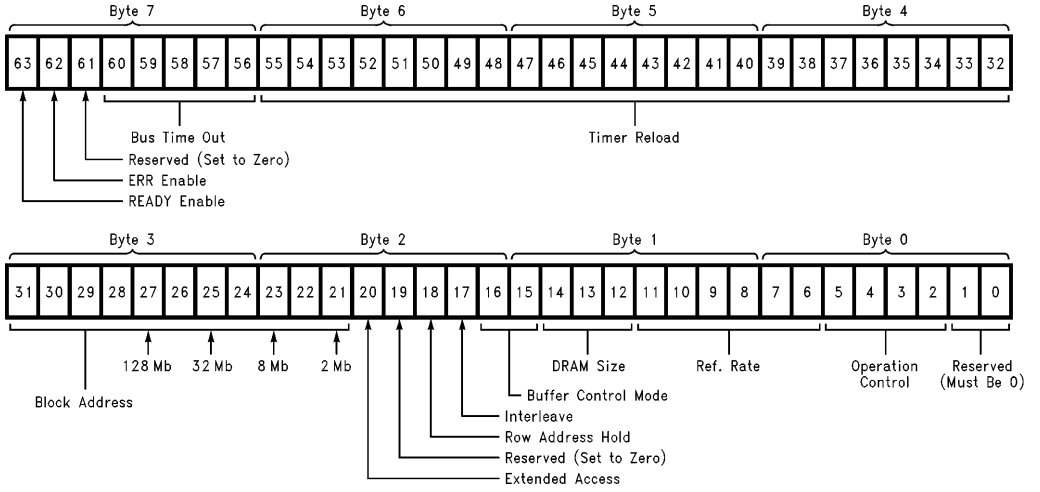

FIGURE 3. Configuration Register Control Fields

Functional Description (Continued)

CYCLE EXTEND

In order to maximize the choice of memory device speeds that may be used for various system clock rates, the Row Address Strobe (RAS) period for a basic access may be programmed for either 3 or 4 clock cycles. When cleared to ''0'', configuration bit 20 indicates that 3 clock cycles (2 wait states) are to be used, when set to ''1'', 4 clock cycles or 3 wait states are required. Setting bit 20 to ''1'' also has the effect of increasing the RAS pre-charge time by 1 clock cycle. Calculation of the number of cycles required per access type is detailed in the NSBMC292 Application Guide.

ROW ADDRESS HOLD

Bit 18 of the configuration register controls the time at which the memory address switches from row to column address. This allows the designer to control the address hold time relative to RAS so that the slowest memory can be used for a range of clock speeds. Setting Bit 18 to ''1'' yields the maximum row address hold time, clearing it shortens the row address hold in favor of additional column address setup.

INTERLEAVE DISABLE

In cost sensitive applications, it is sometimes desirable for a system to operate with a single bank of memory so as to reduce the minimum memory required. In this case the interleave mode bit is programmed to ''1''. If a second bank of memory is added, this bit can be programmed to ''0'' to enable interleave operation and peak performance. In non-interleave mode a burst access is completed in 3 clock cycles for the initial accrss and two cycles thereafter (bit 20 = 0), or four cycles for the initial access and 3 cycles thereafter with bit 20 = 1. Systems that are configured for non-interleave operation should be designed so that only the leaf A signals are used.

The NSBMC292 does not explicitly support 16-bit memory systems, however, if the simple expedient of re-arranging the address input signals is done, 16-bit support is easily achieved. Configurations such as 16-Bit interleaved memory systems are possible, however, since the device count for this configuration is identical to 32-Bit non-interleaved, but the performance is better for the 32-Bit system, it is recommended that the 32-Bit configuration be used in this case.

BUFFER CONTROL MODE FIELD

The transfer of Data from the memory subsystem to the AM29030/35 bus occurs through buffers controlled by the NSBMC292. Two of the signals (LEA, LEB) provide transparent latch controls for use during write cycles. LEA and LEB have variable timing but fixed interpretation. The other two signals, TXA and TXB, change in both timing and function according to programmed mode. Table II presents these signals using names that are function derived.

Signals containing TX are transmit controls for buffers that have output enables (transmit from the memory system). Buffers such as ''245''s or ''646''s, which have direction and enable pins, are controlled by CE (chip enable) in modes 1 and 3. Signals ending with A or B are specific to one or the other of the two leaves of memory controlled by the NSBMC292. Signals without suffixes apply to both leaves. The signal LeafB/*A, required in some configurations, indicates which memory leaf will be selected on the next clock cycle.

TABLE II. Interpretation of the Buffer Control Signals for Various Control Modes

Mode	Signal 1	Signal 2
0	TXA	TXB
1	CEA	CEB
2	TX	LeafB/*A
3	CE	LeafB/*A

Table III presents some of the possible configurations with the corresponding mode settings. For a comprehensive discussion of the selection of a buffer strategy, refer to the NSBMC292 Application Guide.

TABLE III. Possible NSBMC292 Memory/Buffer Configurations

Buffer Type	DRAM Type	Buffer Mode
74FCT646	Nibble	Mode 3
Am29C983	Bit	Mode 2
74FCT543	Bit	Mode 0

For the memory/buffer combinations presented in Table III, RDY is returned after two cycles (1 wait state) for a simple write and after 3 cycles (2 wait states) for an initial simple read. Subsequent access in a burst occur at the rate of one per clock cycle.

DRAM SIZE FIELD

This three bit field, bits 12–14, selects the DRAM device address size, and consequently, memory block size. Note that the memory in both leaves of a bank are required to be of the same size and organization for correct operation. Table IV lists the size codes and the corresponding device sizes.

TABLE IV. Size Code Settings, DRAM Density and Address Range Size

Memory Size Code	Memory Block Size	Max Banks	Memory Types
0 0 0	2 MB	1	256 kb x 1
0 0 1	8 MB	1	1 Mb x 1
0 1 0	32 MB	1	4 Mb x 1
0 1 1	128 MB	1	16 Mb x 1
1 0 0	2 MB	4*	64 kb x 4
1 0 1	8 MB	4*	256 kb x 4
1 1 0	32 MB	4*	1 Mb x 4
1 1 1	128 MB	4*	4 Mb x 4

*Note that banks are sequentially addressed within a block.

REFRESH RATE FIELD

The system clock frequency is used to derive the period of DRAM refresh cycles. The refresh rate is calculated as (PCLK clock frequency) / (16 x (programmed value + 1)). If, for example, the system clock is 25 MHz and the programmed value is 24, the NSBMC292 will execute the 256 refresh cycles for a 256k DRAM in 4.096 ms.

The algorithm employed by the NSBMC292 guarantees the time for complete device refresh, however, individual row refresh may be delayed so as not to pre-empt bursts in

Functional Description (Continued)

progress. Since the maximum burst is 258 clock cycles in length, this delay in no way endangers data integrity. Access to devices other than NSBMC292 controlled memory are not delayed by refresh, access to memory while refresh is in progress are completed once the refresh cycle is complete.

TIMER CONTROL FIELD

The 24-bit timer is a counter which scales PCLK by a programmable amount and automatically reloads when terminal count is reached. The contents of the timer cannot be read directly, however, the counter will generate an interrupt when terminal count is reached. The timer is disabled following a RESET and the **Timer Count Value** (Configuration Bytes 4–6) must be programmed before the timer is enabled.

The interrupt output is asserted low when terminal count is reached and interrupt will remain asserted until the Acknowledge Timer Interrupt op-code is written to configuration byte 0. This timer is intended to be used either as a system heart beat or part of a system WATCHDOG™. This frees the internal timer to be used for real-time critical tasks.

BUS MONITOR CONTROL FIELD

The NSBMC292 contains circuitry that monitors all bus access requests regardless of the target address. Access made to a region configured for external ready can hang the processor if for some reason READY is not returned to terminate the access. The NSBMC292 can detect such a condition and if the bus watch feature is enabled, will return ERR.

The bus monitor operates by monitoring the state of the PRDY signal. Should it be asserted for longer than the programmed **Bus Time Out** value in configuration register 7, BERR is asserted if configuration bit 62 is set. The ERR signal is timed in similar fashion to the RDY signal.

The PRDY signal is to be connected directly to the RDY input of the processor. This signal is pinned-out separately from the RDY signal so that the bus monitor operates correctly even if RDY to the processor is driven from multiple sources combined through a logic gate. If the RDY signal is generated through a ''wire-OR'' then PRDY is physically identical to the RDY output from the NSBMC292.

OPERATION CONTROL FIELD

Byte 0 of the configuration register contains three fields. The first field (from LSB) is reserved for test purposes and must be zero for proper in-circuit operation. The second field is the operation control field which is used to control the state of the page cache, timer, interrupts and bus error signal. The third field is the low two bits of the refresh rate. The NSBMC292 has been designed such that if any of the bits in the operation control field is written with a ''1'', access to the other two fields is disabled and the previous value is retained. If all bits in the operation control field are ''0'', the reserved and refresh rate fields are updated from the current input.

Since the control register is accessed as a byte, automatic masking of the non-control field bits simplifies programming of the control parameters. All parameters in this field may be modified on-the-fly, and all functions are disabled by reset. The operational controls have been encoded such that any access to the register will only modify one parameter.

Bit								Control Function
7	6	5	4	3	2	1	0	
D	D	0	0	0	0	D	D	Update Bits 0,1, 6 and 7 with data D
X	X	0	1	0	0	X	X	Data Access Page Cache Disable (Default)
X	X	0	1	1	0	X	X	Data Access Page Cache Enable
X	X	0	1	0	1	X	X	Instruction Access Page Cache Disable (Default)
X	X	0	1	1	1	X	X	Instruction Access Page Cache Enable
X	X	1	0	0	0	X	X	Acknowledge Timer Interrupt
X	X	1	0	1	0	X	X	Enable Timer Interrupt Output
X	X	1	1	0	0	X	X	Disable Timer Interrupt (Default)

Functional Description (Continued)

PAGE CACHE MANAGEMENT

The Page Cache management implemented by the NSBMC292 incorporates a mechanism whereby advantage can be taken of the page access mode of DRAMs, not only for burst access, but also for non-sequential data and instruction access. The mechanism relies on the fact that as long as RAS is asserted, access to the selected row can be gained by simply asserting a column address and the CAS strobe. The resulting access is slower than a burst only by the amount of time required to ensure that the desired address is in the same row as was previously selected.

The benefits of this type of access are obvious, however, there can be drawbacks. If the required address does not reside in the same page as that selected, the currently selected row must be released and the new row selected before the access can proceed. The process of de-selecting a row and selecting a new one requires that the RAS pre-charge time be allowed to expire before the selection of a new row can begin. This pre-charge time can require up to two additional cycles over a standard access startup.

The efficiency of this type cache (PCache) is related to a large extent on the locality of reference of the datum being accessed. For systems that have mixed Instruction and Data memory systems, PCache efficiency is very dependant on the behavior of the program being executed as related to the ''run-length'' of data and instruction access, the processor internal cache utilization, and the locality of data and instruction references. Since throughput is lowered by cache misses, the page cache can be dynamically enabled/disabled for instruction and/or data access. In this manner the programmer can apply the mechanism judiciously in order to maximize throughput.

For systems in which Instruction and data spaces are controlled by independent NSBMC292s, the page cache management can be used to greater effect as data and instruction ''run length'' ceases to be a factor in determining performance. In this type of configuration cache efficiency is simply a function of locality of reference and a control strategy for the page cache mechanism is much simpler to derive and implement. PCache management is independently controlled for instruction and data access. A recommended starting strategy for improving performance of mixed instruction/data systems is to rely on the burst mechanism and the internal cache for instruction fetching, and enable PCache for Data access only. This general rule of thumb can be improved on, once program behavior is benchmarked.

Typical Application

System Clock:	25 MHz
Refresh Rate:	16 μs per row **(0 × 18)**
Memory Size:	256k x 4 **(Size = 5)**
Buffer Mode:	Signal 1 = TX, Signal 2 = Leaf B/*A **(Mode 2)**
Interleave:	**Enabled**
Row Address Hold:	½ clock cycle **(Row Address Hold = 0)**
Extended Access:	**Disabled** (3 clock RAS derived from t_{RSHL} of NSBMC292, RAS access time of DRAM, buffer delay of 74FCT16543 and setup time of the processor's data inputs)
Base Address:	8MB **(0b00000000100)**
BMC ID:	0

Required Configuration for startup

00000000 10000001 01010110 00000000 (0x00815600)

Configuration Setup

```
0x1F0F0000 (0x10F0000, 0);                  /* Config. bits 7..0 = 0 */
0x1F0F00558 (0x1F0F0400 + (0x56 << 2), 0);  /* Config. bits 15..8 = 0 */
0x1F0F00A24 (0x1F0F0800 + (0x89 << 2), 0);  /* Config. bits 23..16 = 0 */
0x1F0F00C00 (0x1F0F0C00, 0);                /* Config. bits 31..24 = 0 */
```

Typical Application (Continued)

The ease with which the NSBMC292 may be integrated into a system design is illustrated in the diagram in *Figure 4*. The system shown supports an Am29030/35 with between 2 MB and 128 MB of memory, depending on the devices selected, managed by a single NSBMC292. This specific example accommodates 256 kb x 4, 1 Mb x 4 or 4 Mb x 4 devices.

Connection of the NSBMC292 to the Am29030/35 processor is accomplished simply by wiring together pins with the same names. The only exceptions RDY and ERR. If the NSBMC292 is the only device that generates these signals, they can be connected directly to the appropriate inputs of the processor and requires only a small pull-up resistor to keep them de-asserted when in the high impedance state.

If multiple processor peripherals are connected to RDY or ERR, 3-state drivers should be used in such a manner that the signals are actively de-asserted prior to the driver being placed in its' high impedance state. If this rule is followed, a simple ''wire or'' can be used. Alternately, all sources of RDY and ERR can be combined using multiple input gates and the processor signals driven by the outputs.

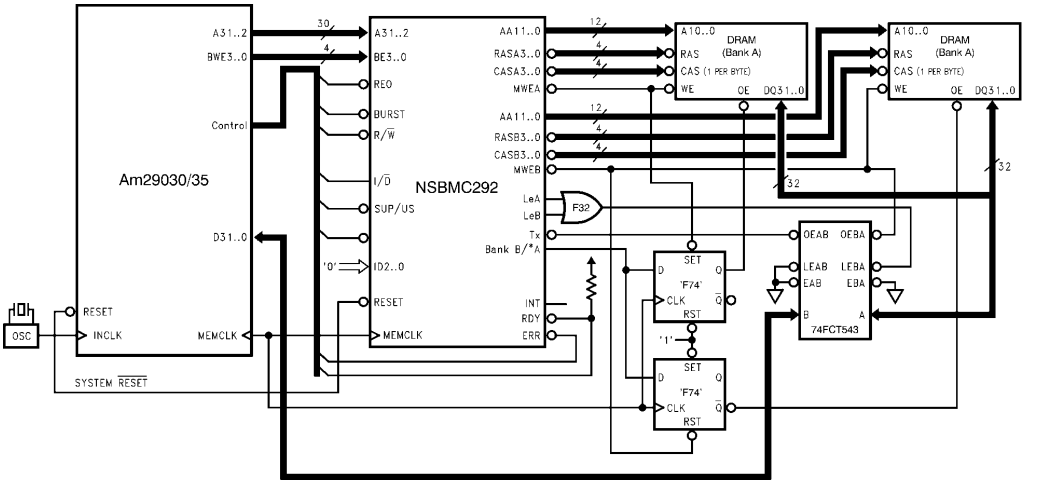

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FIGURE 4. Possible System Interconnection Using NSBMC292

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +7V
Input Voltage (V_{IN})	−0.3V to V_{CC} +0.3V
D.C. Input Current (I_{IN})	±50 mA
Storage Temperature ($\varnothing_{STG}$)	−65°C to +150°C

All Voltages Referenced to Ground

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Ambient Temperature Range ($\varnothing_A$)	
Plastic Package	−0°C to +70°C
Ceramic Package	−55°C to +85°C

DC Electrical Characteristics

#	Symbol	Description	Conditions	Min	Max	Units
1	V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V		1.4	V
2	V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	3.7		V
3	I_{IL}	Low Level Input Current	V_{IN} = V_{SS}, V_{CC} = 5.25V	−10		μA
4	I_{IH}	High Level Input Current	V_{IN} = V_{CC} = 5.25V		10	μA
5	V_{OL}	Low Level Output Voltage	V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA		0.4	V
6	V_{OH}	High Level Output Voltage	V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA	3.7		V
7	I_{OZL}	Low Level TRI-STATE® Output Current	V_{IN} = V_{IL} or V_{IH} V_O = V_{SS}	−20		μA
8	I_{OZH}	Low Level TRI-STATE Output Current	V_{IN} = V_{IL} or V_{IH} V_O = 5.25V		20	μA
9	I_{CCMax}	Maximum Supply Current	Continuous Simple Access Continous Burst Access		100 30	mA
10	C_{IN}	Input Capacitance			20	pF
11	C_{OUT}	Output Capacitance			20	pF

Timing Parameters

INTERFACE TIMING

The NSBMC292 interface to the Am29030/35 has been designed for direct interconnect. It is not necessary to place other logic devices between the processor and the NSBMC292, nor is their use encouraged. The introduction of intermediate address or control signal buffers can result in skews or delays that will require the system clock frequency to be derated for operation under worst case conditions. The timing diagrams presented in this section assume that all signals between the processor and the NSBMC292 are un-buffered.

REFRESH TIMING

Figure 5 details the timing of the RAS only refresh performed by the memory controller when there is a competing request from a bus master. A competing request is defined as any request that occurs between T0 and T5. For any request in this range, the timing is exactly as shown. As illustrated, the diagram represents the timing that results when bit 20 of the configuration register is cleared to zero. If bit 20 is set to ''1'', an additional cycle is inserted at T3 and T8.

SIMPLE ACCESS TIMING

The NSBMC292 can return data to the processor in only 3 clock or 4 clock cycles for a basic access (2 or 3 wait states) depending on the mode chosen (Configuration Bit 20). If multiple access cycles are requested back to back then the BMC will pause for a minimum of 2 clocks between RAS cycles to insure that the RAS pre-charge time is met resulting in 5 or 6 clocks between successive simple cycles.

Figure 6 shows the timing relationship between the system clock, processor control signals and NSBMC292 outputs. All NSBMC292 outputs are derived synchronously with the exception of tARA (processor address to row address delay). Two simple access cycles are shown in the diagram. The first is a read cycle that assumes that the NSBMC292 was idle prior to the start of the cycle, the second is backed onto the first to show the effect of RAS pre-charge imposed by NSBMC292. If bit 20 is set to ''1'', a wait state will be inserted after cycles T3 and T8.

BURST ACCESS TIMING

When a burst access is requested by the processor, the NSBMC292 generates the sequence in *Figure 7*. If the burst is, for example 2 words long, the processor de-asserts BURST in T5 and the sequence terminates in T6. The first access of the burst sequence begins in the same manner as a simple access. Consequently the timing parameters from *Figure 6* may be applied in *Figure 7*.

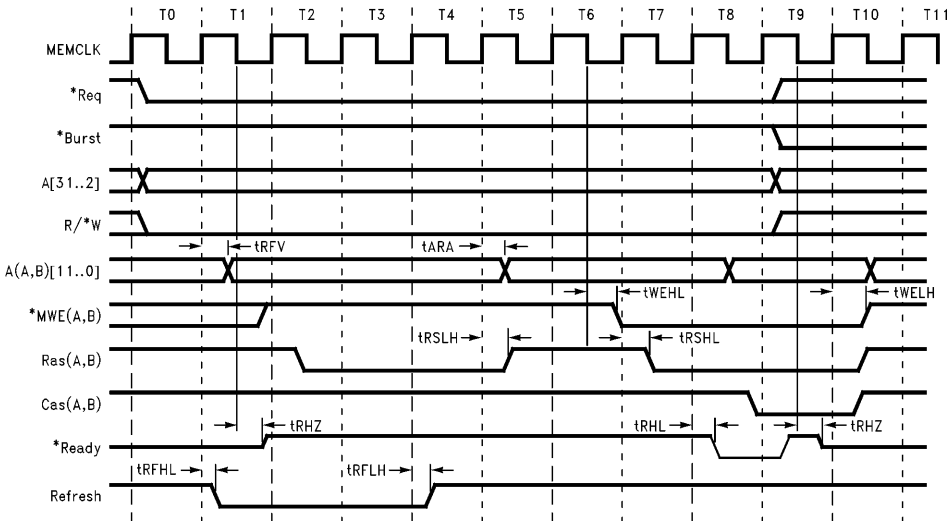

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FIGURE 5. Refresh Timing

Timing Parameters (Continued)

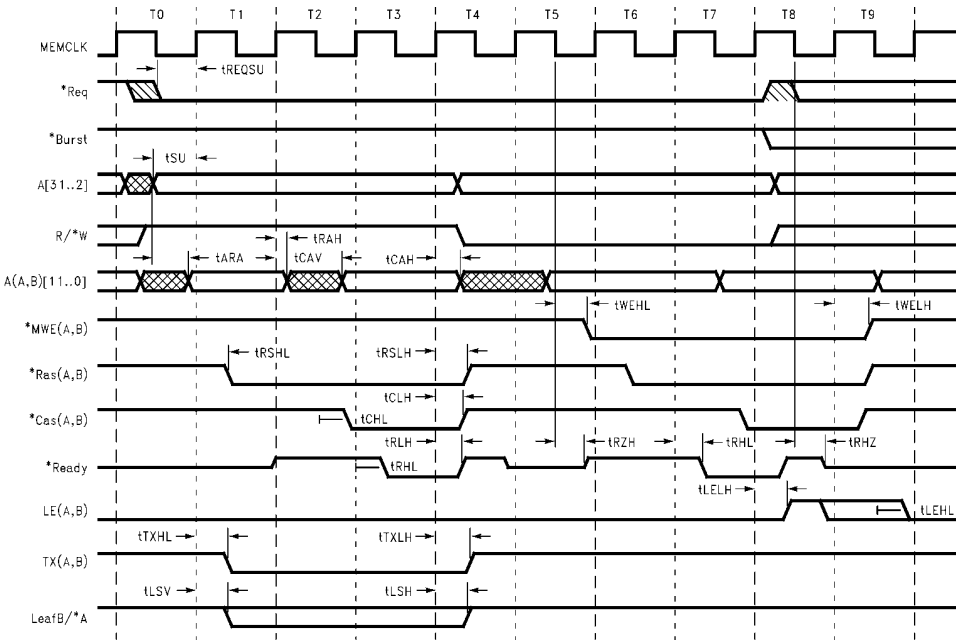

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FIGURE 6. Basic Access Timing

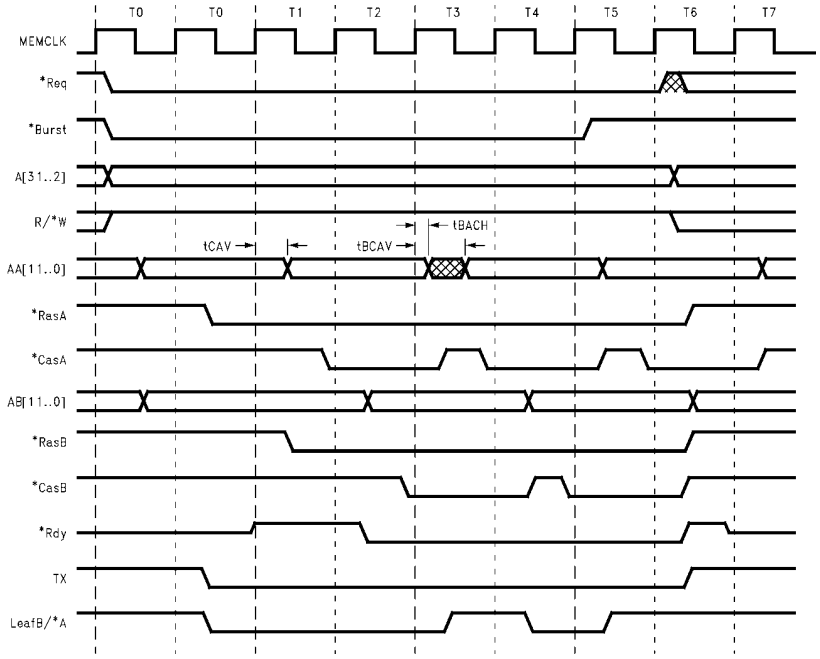

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FIGURE 7. Burst Access Timing

Timing Parameters (Continued)

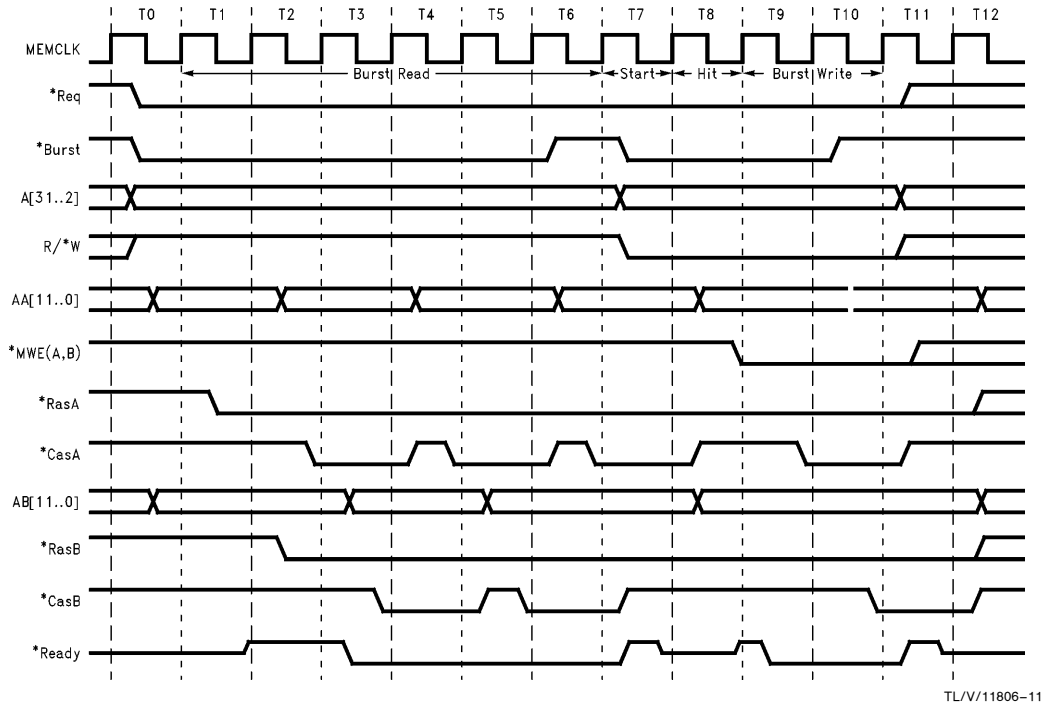


FIGURE 8. Burst Access w/t PCache Hit

Figures 8 and *9* show the sequence of events that can occur when PCache is enabled. The sequence in *Figure 8* shows two back-to-back in the same page. This type of sequence yields the highest data transfer rate achievable with DRAM. *Figure 9* shows the worst case scenario. This example shows two back-to-back simple access to different rows with PCache is enabled. This is an example of the slowest transfer sequence that may occur.

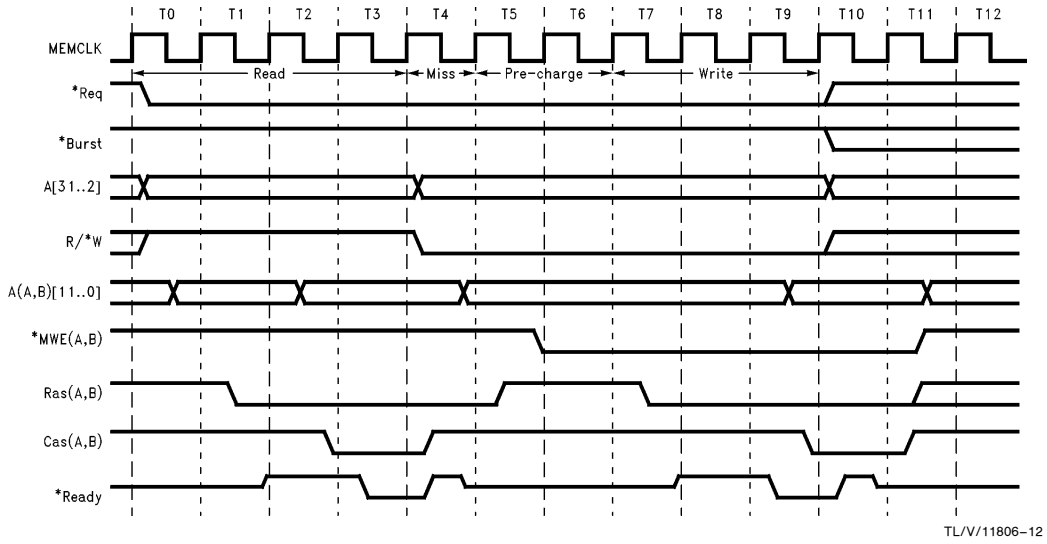


FIGURE 9. Simple Access w/t PCache Miss

AC Timing Parameters (Unless otherwise stated V_{CC} = 5.0V ±5%, 0°C < T_A < 70°C.)

#	Symbol	Description	16 MHz		25 MHz		33 MHz		Units
			Min	Max	Min	Max	Min	Max	
1	t_{RQSU}	Request Input Setup Time	14		12		9		ns
2	t_{SU}	Synchronous Input Setup	14		12		9		ns
3	t_H	Synchronous Input Hold		3		3		3	ns
4	t_{BSU}	Burst Input Setup	14		12		9		ns
5	t_{BH}	Burst Input Hold		3		3		3	ns
6	t_{RZH}	RDY 3-State to Valid Delay Relative to *MEMCLK		29		24		19	ns
7	t_{RHL}	RDY Synchronous Assertion Delay		26		21		17	ns
8	t_{RLH}	RDY Synchronous De-assertion Delay		25		20		16	ns
9	t_{RHZ}	RDY Valid to TRI-STATE Delay Relative to *MEMCLK		27		22		17	ns
10	t_{ARA}	Address Input to Row Address Output Delay (Note 1)		23		19		15	ns
11	t_{RAH}	*MEMCLK or MEMCLK to Row Address Hold		40		33		26	ns
12	t_{CAV}	*MEMCLK or MEMCLK to Column Address Valid (Note 1)		38		31		25	ns
13	t_{CAH}	MEMCLK to Column Address Hold	4		4		4		ns
14	t_{DRAH}	DRAM Row Address Hold (Note 2)	t_{M-4}		t_{M-4}		t_{M-4}		ns
15	t_{RSHL}	MEMCLK to RAS Asserted Delay (Note 1)		29		24		19	ns
16	t_{RSLH}	MEMCLK to RAS De-asserted Delay (Note 1)		26		21		17	ns
17	t_{CHL}	MEMCLK to CAS Asserted Delay (Note 1)		23		19		15	ns
18	t_{CLH}	MEMCLK to CAS De-asserted Delay (Note 1)		20		16		13	ns
19	t_{BHL}	MEMCLK to Buffer Control Asserted Delay (Note 1)		26		21		17	ns
20	t_{BLH}	MEMCLK to Buffer Control De-asserted Delay (Note 1)	4	23	4	19	4	15	ns
21	t_{BSV}	MEMCLK to Bank Select Valid Time (Note 1)		26		21		17	ns
22	t_{BSH}	MEMCLK to Bank Select Hold Time (Note 1)	4		4		4		ns
23	t_{WEHL}	*MEMCLK to Write Enable Asserted Delay (Note 1)		31		25		20	ns
24	t_{WELH}	MEMCLK to Write Enable De-asserted Delay (Note 1)		28		22		18	ns
25	t_{CAH}	*MEMCLK to Column Address Hold Time (Burst) (Note 1)	5		5		4		ns
26	t_{CAV}	*MEMCLK to Column Address Valid Delay (Burst) (Note 1)		29		23		19	ns
27	t_{LEHL}	*MEMCLK to Latch Enable Assertion		23		19		15	ns
28	t_{LELH}	MEMCLK to Latch Enable De-assertion		20		16		13	ns
29	t_{RFA}	MEMCLK to Row Address Valid (Refresh)		38		31		25	ns
30	t_{RFH}	MEMCLK to Row Address Hold (Refresh)	4		4		4		ns
31	t_{RFHL}	REFRESH Synchronous Assertion Delay		20		16		13	ns
32	t_{RFLH}	REFRESH Synchronous De-assertion Delay		20		16		13	ns

Signal output delays are measured relative to MEMCLK (except as indicated) using a 50 pF load.

Note 1: Derate the given delays by 0.06 ns per pF of load in excess of 50 pF.

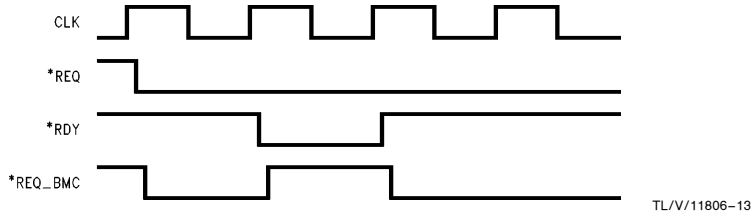
Note 2: t_M = MEMCLK High time when configuration bit 18 = 0.
t_M = MEMCLK cycle time = $1/_{(MEMCLK\ frequency)}$ for configuration bit 18 = 1.

Timing for Rev A silicon.

Errata for the V292BMC

A full set of CUPL style PAL equations would be as follows:

```
/*The "!" symbol on a pin indicates a physical low true signal*/
Pin          !reg           /*Request Signal Input from Am29030*/
Pin          !rdy           /*Ready Signal Input from Am29030*/
Pin          !burst         /*Burst Signal Input from Am29030*/
Pin          !reg_bmc       /*Request Signal Output to V292BMC*/
Pin          !reg_enable    /*Request Enable Signal Output for Internal Use*/
/*Equations for Low Speed Operation. The critical timing chain is
 *max CLOCK to RDY delay + max RDY to REQ_BMC delay + max REQ_BMC to clock setup
```



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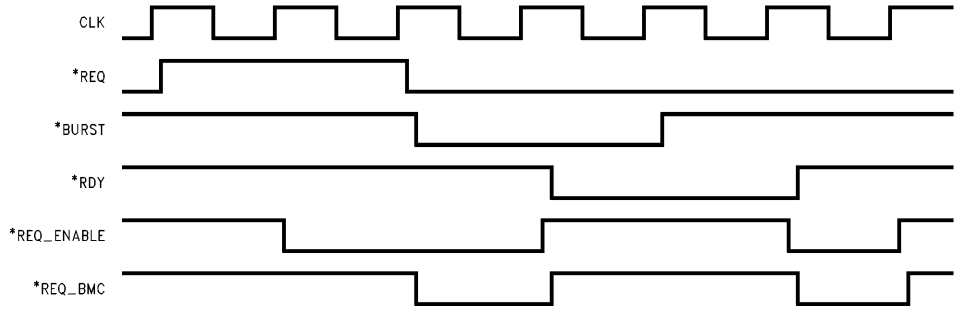
```
*/
req_bmc      = reg & !rdy;
/*Equations for High Speed Operation. The critical timing chain is
 *max CLOCK to REQ delay + max REQ to REQ_BMC delay + max REQ_BMC to clock setup
```



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```
*/
req_enabled  =  !req # rdy & !burst; /*Input to D type flip-flop*/
req_bmc      =  req & req_enable;
```

A second erratum for the V292BMC is

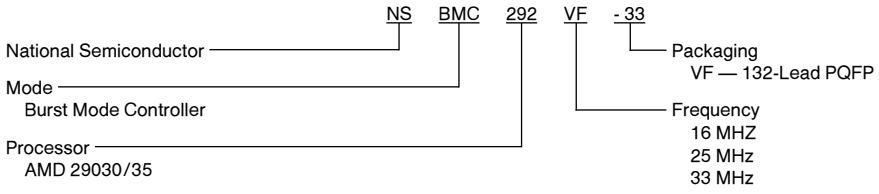
When the V292BMC is programmed for extended timing mode operation, back to back memory read cycles or back to back memory write cycles will fail.

The recommended fix would be as follows:

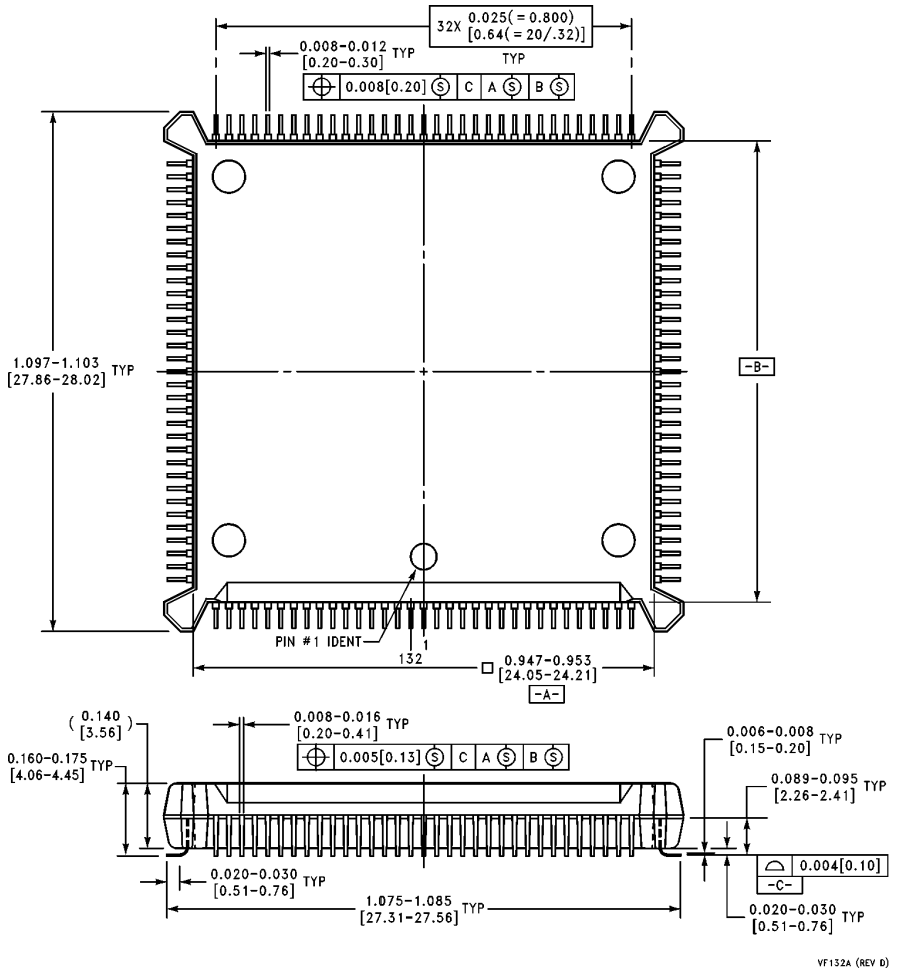
```
req_enabled  =  !reg # !rdy;/*Input to D type flip-flop*/
req_bmc      =  req & req_enable;
```

This will cause a 1 cycle delay to be added from the end of one request (as indicated by !RDY) and the beginning of the next request.

Ordering Information



Physical Dimensions inches (millimeters)



132-Pin Plastic Quad Flatpak (PQFP)
Order Number NSBMC292VF
NS Package Number VF132A

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