National Semiconductor

microCMOS

NSC831 Parallel I/O

General Description

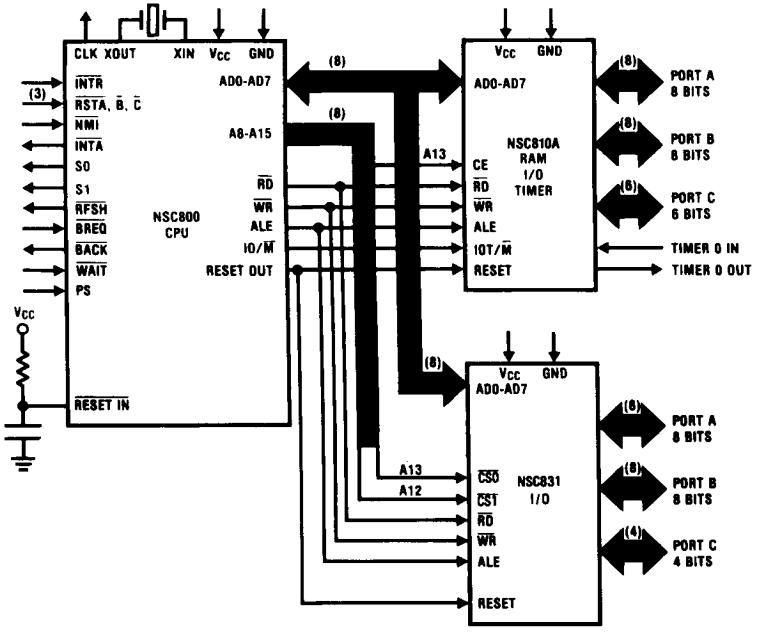
The NSC831 is an I/O device which is fabricated using microCMOS silicon gate technology, functioning as an input/output peripheral interface device. It consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written to or read from in bytes. Several types of strobed mode operations are available through Port A.

For military applications the NSC831 is available with class B screening in accordance with methods 5004 of MIL-STD-883.

Features

- Three programmable I/O ports
- Single 5V Power Supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Directly compatible with NSC800 family
- Strobed modes available on Port A

Microcomputer Family Block Diagram



TL/C/5584–1

Table of Contents

1.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin With Respect to Ground	−0.3V to V_{CC} + 0.3V
V_{CC}	7V
Lead Temp. (Soldering, 10 seconds)	300°C
Power Dissipation	1W

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

2.0 Operating Range V_{CC} = 5V ±10%

NSC831-1: 0°C to +70°C
−40°C to +85°C

NSC831-3: −40°C to +85°C
−55°C to +125°C

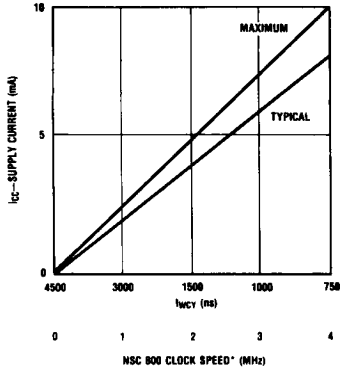
NSC831-4: 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

3.0 DC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	I_{OH} = −1.0 mA	2.4			V
		I_{OUT} = −10 μA	4.0V			V
V_{OL}	Logical 0 Output Voltage	I_{OL} = 2 mA	0		0.4	V
		I_{OUT} = 10 μA	0		0.1	V
I_{IL}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, t_{WCY} = 750 ns		15	20	mA
I_Q	Quiescent Current	RESET = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 1, CE = 1, AD0–7 = 0, ALE = 1, V_{IN} = 0, or V_{IN} = V_{CC} V_{CC} = 5.5V, GND = 0V, PA0–7 = 1, PB0–7 = 1, PC0–7 = 1 No Input Switching, T_A = 25°C		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage	(Note 1)	2.4	5	6	V

Note 1: Operation at lower power supply voltages will reduce the maximum operating speed. Operation at voltages other than 5V ±10% is guaranteed by design, not tested.

I_{CC} vs. SPEED



TL/C/5594–2

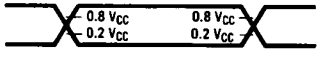
*When NSC831 is used with NSC800

4.0 AC Electrical Characteristics V_{CC} = 5V ±10%, GND = 0V

Symbol	Parameter	Test Conditions	NSC831-1		NSC831-3		NSC831-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	C_L = 150 pF		1000		400		250	ns
t_{AH}	AD0–AD7, CE, IO/$\overline{M}$ Hold Time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		130		90		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		120		ns
t_{AS}	AD0–AD7, CE, IO/$\overline{M}$ Setup Time		100		45		40		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		320		300	ns
t_{DS}	Data Setup Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Setup Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Output			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		220		ns
t_{RDD}	Data Bus Disable		0	100	0	85	0	85	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		300		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		80		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold With Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to INTR Output			300		300		300	ns
t_{SS}	Peripheral Data Setup With Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		300		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		300		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

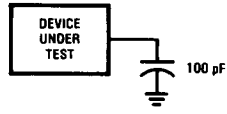
Note: Test conditions: t_{WCY} = 3000 ns for NSC831-1, 1200 ns for NSC831-3, 750 ns for NSC831-4

AC TESTING INPUT/OUTPUT WAVEFORM



TL/C/5594–3

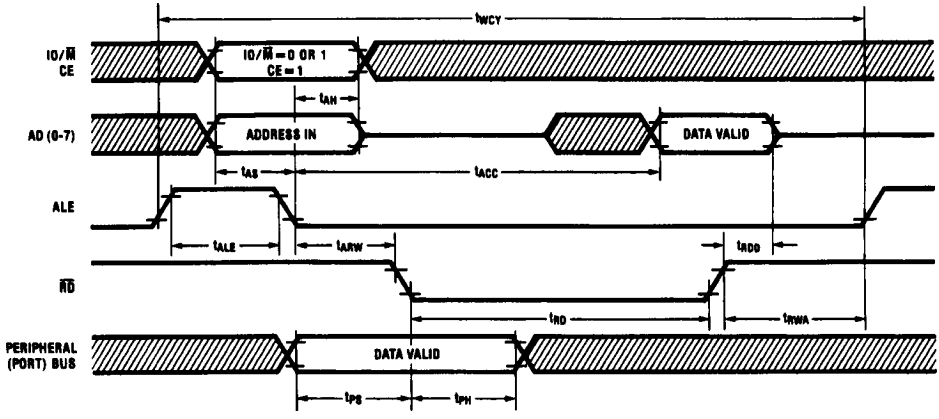
AC TESTING LOAD CIRCUIT



TL/C/5594–4

5.0 Timing Waveforms

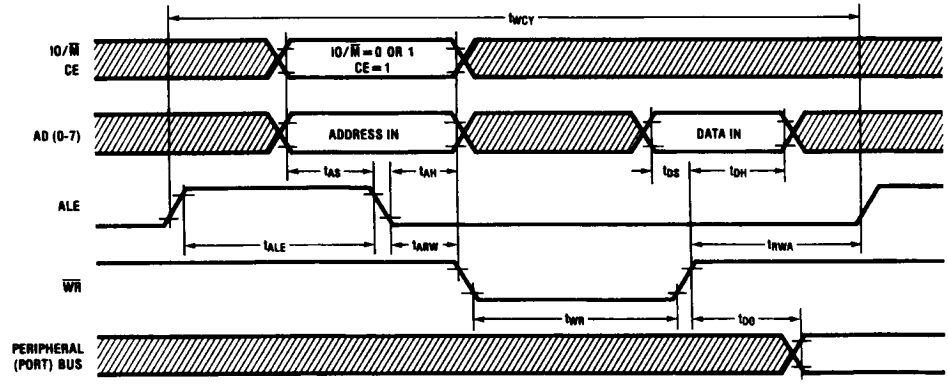
Read Cycle (Read from Port)



TL/C/5594–5

Note: Diagonal lines indicate interval of invalid data.

Write Cycle (Write to Port)

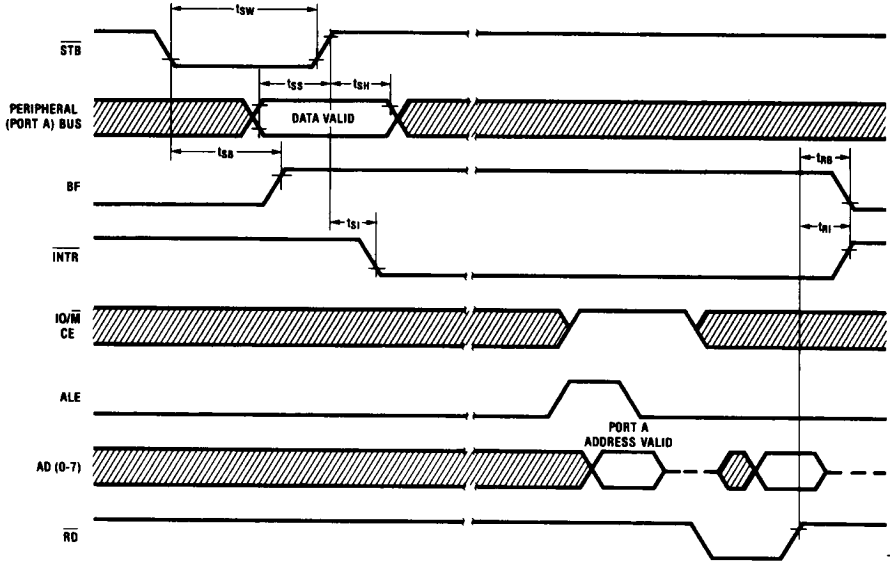


TL/C/5594–6

Note: Diagonal lines indicate interval of invalid data.

5.0 Timing Waveforms (Continued)

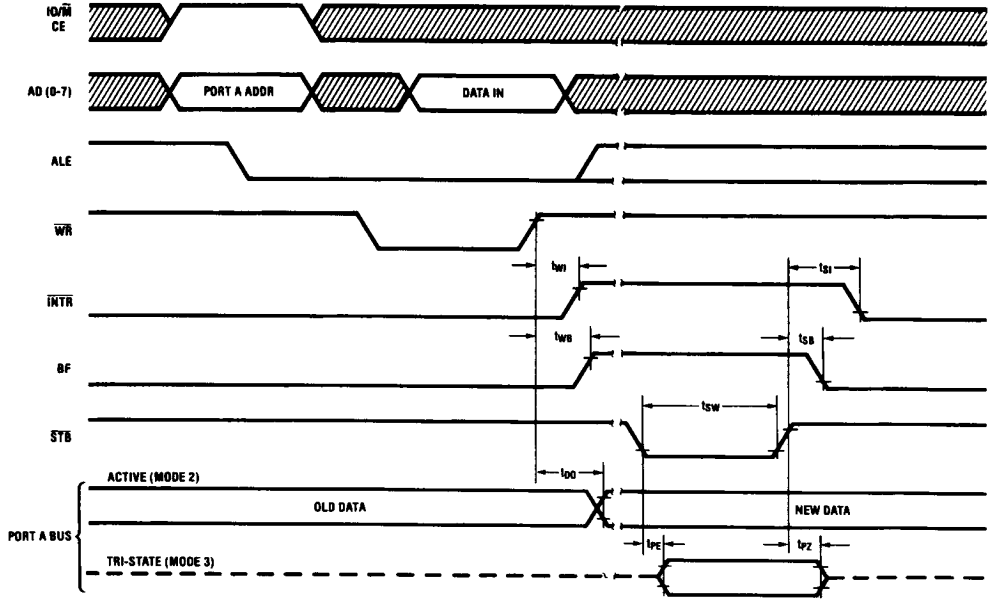
Strobed Mode Input



TL/C/5594–7

Note: Diagonal lines indicate interval of invalid data.

Strobed Mode Output



TL/C/5594–8

Note: Diagonal lines indicate interval of invalid data.

6.0 Pin Descriptions

The following describes the function of all NSC831 input/output pins. Some of these descriptions reference internal circuits.

6.1 INPUT SIGNALS

Master Reset (RESET): An active-high input on the RESET pin initializes the chip causing the three I/O ports (A, B and C) to revert to the input mode. The three ports, the three data direction registers and the mode definition register are reset to low (0).

Chip Enable ($\overline{CE_0}$, $\overline{CE_1}$): The CE inputs must be active at the falling edge of ALE. At ALE time, the CE inputs are latched to provide access to the NSC831.

Read ($\overline{RD}$): when the $\overline{RD}$ input is an active low, data is read from the AD0–AD7 bus.

Write ($\overline{WR}$): When the CE inputs are active an active low $\overline{WR}$ input causes the selected output port to be written with the data from the AD0–AD7 bus.

Address Latch Enable (ALE): The trailing edge (high to low transition) of the ALE input signal latches the address/data present on the AD0–AD7 bus, plus the input control signals on $\overline{CE_0}$ and $\overline{CE_1}$.

Power (V_{CC}): 5V power supply.

Ground (V_{SS}): Ground reference.

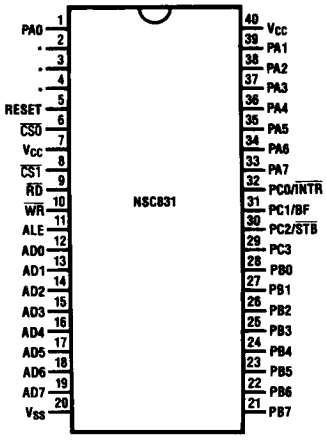
6.2 INPUT/OUTPUT SIGNALS

Bidirectional Address/Data Bus AD0–AD7: The lower 8 bits of the I/O address are applied to these pins, and latched by the trailing edge of ALE. During read operations, 8 bits are present on these pins, and are read when $\overline{RD}$ is low. During an I/O write cycle, Port A, B, or C is written with the data present on this bus at the trailing edge of the $\overline{WR}$ strobe.

Ports A, B, C (PA0–PA7, PB0–PB7, PC0–PC3): These are general purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDRs).

7.0 Connection Diagrams

Dual-In-Line Package



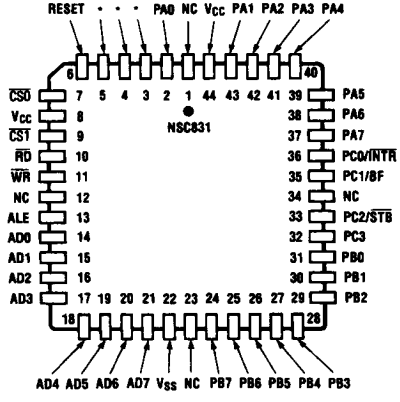
TL/C/5594–9

Top View

*Tie pins 2, 3, and 4 to either V_{CC} or V_{SS}.

Order Number NSC831D or N
See NS Package Number D40C or N40A

Leadless Chip Carrier



NC = NO CONNECT

TL/C/5594–10

Top View

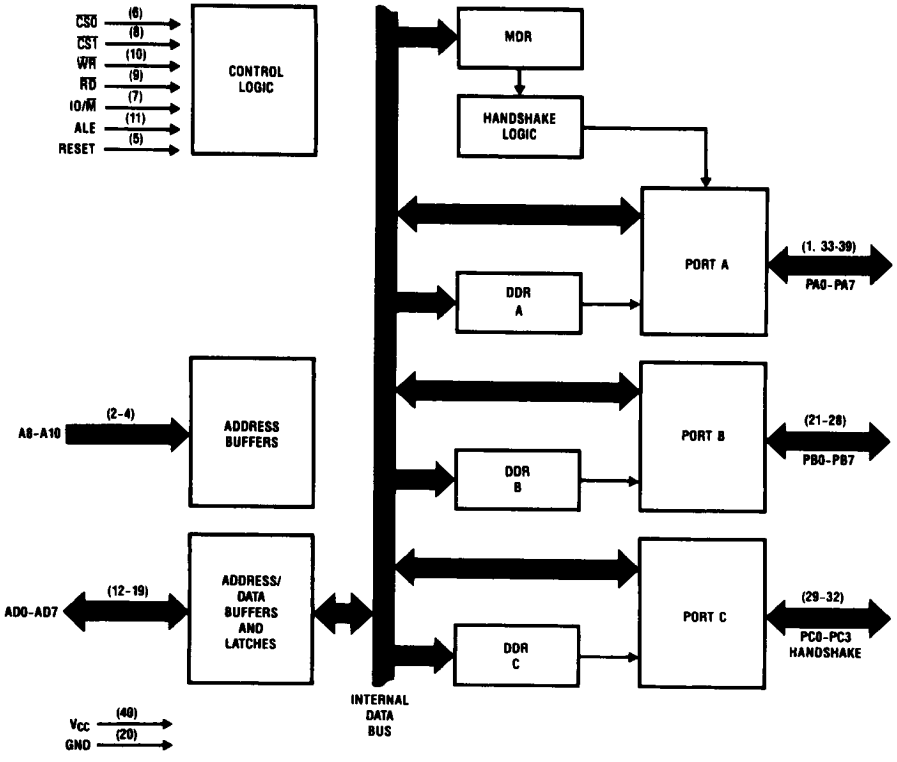
Order Number NSC831E
See NS Package Number E44A

8.0 Functional Description

Refer to *Figure 1* for a detailed block diagram of the NSC831, while reading the following paragraphs.

Input/Output (I/O): The I/O of the NSC831 contains three sets called Ports. There are two ports (A and B) which contain 8 bits each and one port (Port C) which has 4 bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (4 bits for Port C). When reading Port C, bits 4–7 will be read as ones. All ports share common functions of Read, Write, Bit-Set and Bit-Clear. Additionally, Port A is programmable for strobed (handshake mode input or output. Port C has a programmable second function for each bit associated with strobed modes. Table I defines the address location of the ports and control registers.

8.1 BLOCK DIAGRAM



TL/C/5594–11

Note: Applicable pinout for 40 pin dual-in-line package within parentheses.

FIGURE 1

8.0 Functional Description (Continued)

8.2 I/O PORTS

There are three I/O ports (labeled A, B and C) on the NSC831. Ports A and B are 8-bits wide; port C is 4-bits wide. These ports transfer data between the CPU bus and the peripheral bus and vice versa. The way in which these transfers are handled depends upon the currently programmed operating mode.

The NSC831 can be programmed to operate in four different modes. One of these modes (Basic I/O) allows direct transfer of I/O data without any handshaking between the NSC831 and the peripheral. The other three modes (Strobed I/O) provide for timed transfers of I/O data with handshaking between the NSC831 and the peripheral.

Determination of the NSC831 port's mode, data direction and data is done by five registers which are under program control. The Mode Definition Register determines in which of the four I/O modes the chip will operate. Another register (Data Direction Register) establishes the data direction for each bit in that port. The Data Register holds data to be transferred or that which was received. The final two registers per port allow individual data register bits to be cleared (Bit-Clear Register) or data register bits to be set (Bit-Set Register).

Operation during Strobed I/O utilizes two of the port C pins for handshaking and one port C pin to interrupt the CPU.

8.3 REGISTERS

As indicated in the overview, programmable registers control the flow of data through the ports. Table I shows the registers of the NSC831. All registers affecting I/O transfers are in the first grouping of this table.

• Mode Definition Register (MDR)

The MDR determines the operating mode for port A and whether or not the lower 3-bits of port C will be used for handshaking (Strobed I/O). Port B always transfers data via the Basic I/O mode, regardless of how the MDR is programmed.

The four modes are as follows:

Mode 0—Basic I/O (Input or Output)

Mode 1—Strobed Mode Input

Mode 2—Strobed Mode Output (Active Peripheral Bus)

Mode 3—Strobed Mode Output (TRI-STATE Peripheral Bus)

The address assignment of the MDR is xxx00111 as shown in Table I. The upper 3 "don't care" bits are determined by the users decode logic (chip enable address). Table II specifies the data that must be loaded into the MDR to select the mode.

• Data Direction Registers (DDR)

Each port has a DDR that determines whether an individual port bit will be an input or an output. If DDR for the port bit is set to a 1, then that port bit is an output. If its DDR is reset to a 0, then it is an input. The DDR bits cannot be individually written to; the entire DDR register is affected by a write to the DDR. Thus, all data bits written must be consistent for all desired port bit directions.

TABLE I. I/O and Timer Address Designations

8-Bit Address Field Bits								Designation I/O Port, Timer, etc.	R (Read) W (Write)
7	6	5	4	3	2	1	0		
x	x	x	x	0	0	0	0	Port A (Data)	R/W
x	x	x	x	0	0	0	1	Port B (Data)	R/W
x	x	x	x	0	0	1	0	Port C (Data)	R/W
x	x	x	x	0	0	1	1	Not Used	**
x	x	x	x	0	1	0	0	DDR - Port A	W
x	x	x	x	0	1	0	1	DDR - Port B	W
x	x	x	x	0	1	1	0	DDR - Port C	W
x	x	x	x	0	1	1	1	Mode Definition Reg.	W
x	x	x	x	1	0	0	0	Port A - Bit-Clear	W
x	x	x	x	1	0	0	1	Port B - Bit-Clear	W
x	x	x	x	1	0	1	0	Port C - Bit-Clear	W
x	x	x	x	1	0	1	1	Not Used	**
x	x	x	x	1	1	0	0	Port A - Bit-Set	W
x	x	x	x	1	1	0	1	Port B - Bit-Set	W
x	x	x	x	1	1	1	0	Port C - Bit-Set	W
x	x	x	x	1	1	1	1	Not Used	**

x = don't care

LB = low-order byte

HB = high-order byte

* A write accesses the modulus register, a read the read buffer.

** A read from an unused location reads invalid data, a write does not affect any operation of NSC831.

TABLE II. Mode Definition Register Bit Assignments

Mode	Bit 7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	0
1	x	x	x	x	x	x	0	1
2	x	x	x	x	x	0	1	1
3	x	x	x	x	x	1	1	1

8.0 Functional Description (Continued)

Any write or read to the port bits contradicting the direction established by the DDR will not affect the port bits output or input. However, a write to a port bit, defined as an input, will modify the output latch and a read to a port bit, defined as an output, will read this output latch. See *Figure 2*.

• Data Registers

These registers contain the actual data being transferred between the CPU and the peripheral. In Basic I/O, data presented by the peripheral (read cycle) will be latched on the falling edge of $\overline{RD}$. Data presented by the CPU (write cycle) will be valid after the rising edge of $\overline{WR}$ (see AC characteristics for exact timing).

During Strobed I/O, data presented by the peripheral must be valid on the rising edge of $\overline{STB}$. Data received by the peripheral will be valid on the rising edge of $\overline{STB}$. Data latched by the port on the rising edge of $\overline{STB}$ will be preserved until the next CPU read or $\overline{STB}$ signal.

• Bit Set-Clear Registers

The I/O features of the RAM-I/O-timer allow modification of a single bit or several bits of a port with the Bit-Set and Bit-Clear commands. The address selected indicates whether a Bit-Set or Clear will take place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing 1s will cause the indicated operation to be performed on the corresponding port bit. All bits of the mask with 0s cause the corresponding port bits to remain unchanged. Three sample operations are shown in Table III using port B as an example.

TABLE III. Bit-Set and Clear Examples

Operation Port B	Set B7	Clear B2 and B0	Set B4, B3 and B1
Address	xxx01101	xxx01001	xxx01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

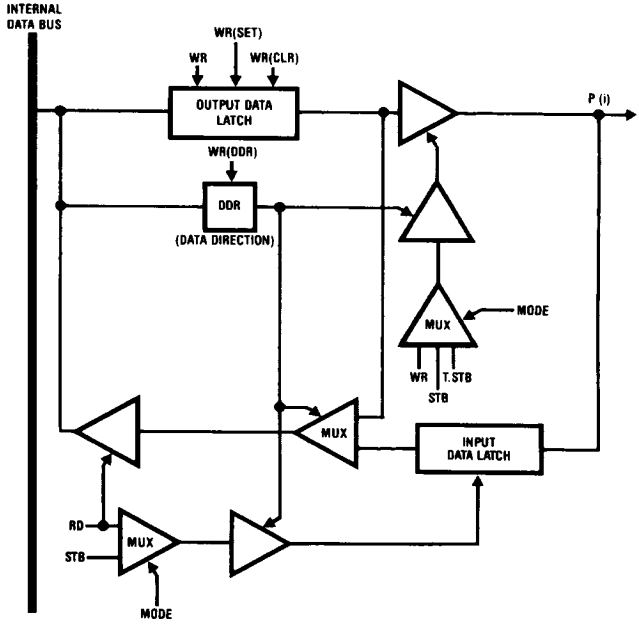
8.4 MODES

Two data transfer modes are implemented: Basic I/O and Strobed I/O. Strobed I/O can be further subdivided into three categories: Strobed Input, Strobed Output (active peripheral bus) and Strobed Output (TRI-STATE peripheral bus). The following descriptions detail the functions of these categories.

• Basic I/O

Basic I/O mode uses the $\overline{RD}$ and $\overline{WR}$ CPU bus signals to latch data at the peripheral bus. This mode is the permanent mode of operation for ports B and C. Port A is in this mode if the MDR is set to mode 0. Read and write byte operations and bit operations can be done in Basic I/O. Timing for these modes is shown in the AC Characteristics Table and described with the data register definitions.

When the NSC831 is reset, all registers are cleared to zero. This results in the basic mode of operation being selected, all port bits are made inputs and the output latch for each port bit is cleared to zero. The NSC831, at this point, can read data from any peripheral port without further set-up. If outputs are desired, the CPU merely has to program the appropriate DDR and then send data to the data ports.



TL/C/5594–12

FIGURE 2

8.0 Functional Description (Continued)

• Strobed I/O

Strobed I/O Mode uses the $\overline{STB}$, BF and $\overline{INTR}$ signals to latch the data and indicate that new data is available for transfer. Port A is used for the transfer of data when in any of the Strobed modes. Port B can still be used for Basic I/O and the lower 3-bits of port C are now the three handshake signals for Strobed I/O. Timing for this mode is shown in the AC Characteristic Tables.

Initializing the NSC831 for Strobed I/O Mode is done by loading the data shown in Table IV into the specified register. The registers should be loaded in the order (left to right) that they appear in Table IV.

TABLE IV. Mode Definition Register Configurations

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Basic I/O	xxxxxxx0	Port bit directions are determined by the bits of each port's DDR		
Strobed Input	xxxxxx01	00000000	xxx011	xxx1xx
Strobed Output (Active)	xxxxx011	11111111	xxx011	xxx1xx
Strobed Output (TRI-STATE)	xxxxx111	11111111	xxx011	xxx1xx

• Strobed Input (Mode 1)

During strobed input operations, an external device can load data into port A with the $\overline{STB}$ signal. Data is input to the PA0–7 input latches on the leading (negative) edge of $\overline{STB}$, causing BF to go high (true). On the trailing (positive) edge of $\overline{STB}$ the data is latched and the interrupt signal, $\overline{INTR}$, becomes valid indicating to the CPU that new data is available. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output data latch for PC2 is set to 1.

When the CPU reads port A, address x'00, the trailing edge of the $\overline{RD}$ strobe causes BF and $\overline{INTR}$ to become inactive, indicating that the strobed input cycle has been completed.

• Strobed Output—Active (Mode 2)

During strobed output operations, an external device can read data from port A using the $\overline{STB}$ signal. Data is initially loaded into port A by the CPU writing to I/O address x'00. On the trailing edge of $\overline{WR}$, $\overline{INTR}$ is set inactive and BF becomes valid indicating new data is available for the external device. When the external device is ready to accept the data in port A it pulses the $\overline{STB}$ signal. The rising edge of $\overline{STB}$ resets BF and activates the $\overline{INTR}$ signal. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output latch for PC2 is set to 1. $\overline{INTR}$ in this mode indicates a condition that requires CPU intervention (the output of the next byte of data).

• Strobed Output—TRI-STATE (Mode 3)

The Strobed Output TRI-STATE Mode and the Strobed Output active (peripheral) bus mode function in a similar manner with one exception. The exception is that the data signals on PA0–7 assume the high impedance state at all times except when accessed by the $\overline{STB}$ signal. Thus, in addition to its timing function, $\overline{STB}$ enables port A outputs to active logic levels. This Mode 3 operation allows other data sources, in addition to the NSC831, to access the peripheral bus. Strobed Mode 3 is identical to Strobed Mode 2, except as indicated above.

Example Mode 1 (Strobed Input):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZATION			
Reset NSC831	H	L	Basic input mode all ports.
Load 01'H into MDR	H	L	Strobed input mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load 00'H into DDR A	H	L	Sets data direction register for port A to input; data from port A peripheral bus is available to the CPU if the $\overline{STB}$ signal is used, other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers.
Load 04'H into Port C Bit-Set Register	H	L	Sets output latch (PC2) to enable $\overline{INTR}$; $\overline{INTR}$ will latch active whenever $\overline{STB}$ goes low; $\overline{INTR}$ can be disabled by a bit-clear to PC2.*
OPERATION			
$\overline{STB}$ pulses low	L	H	Data on peripheral bus is latched into port A; $\overline{INTR}$ is cleared by a CPU read of port A or a bit-clear of $\overline{STB}$.
CPU reads Port A	H	L	CPU gets data from port A; $\overline{INTR}$ is cleared; peripheral is signalled to send next byte via an inactive BF signal. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).

*Port C can be read by the CPU at anytime, allowing polled operation instead of interrupt driven operation.

8.0 Functional Description (Continued)

Example Mode 2 (Strobed Output—active peripheral bus):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZE			
Reset NSC831	H	L	Basic input mode all ports.
Load 03'H into MDR	H	L	Strobed output mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load FF'H into DDR A	H	L	Sets data direction register for port A to output; data from port A is available to the peripheral if the $\overline{STB}$ signal is used other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers
Load 04'H into Port C Bit-Set Register	L	L	Sets output latch (PC2) to enable $\overline{INTR}$; active $\overline{INTR}$ indicates that CPU should send data; $\overline{INTR}$ becomes inactive whenever the CPU loads port A; $\overline{INTR}$ can be disabled by a bit-clear to $\overline{STB}$.*
OPERATION			
CPU writes to Port A	H	H	Data on CPU bus is latched into port A; $\overline{INTR}$ is set by the CPU write to port A; active BF indicates to peripheral that data is valid; Peripheral gets data from port A; $\overline{INTR}$ is reset active; The active $\overline{INTR}$ signals the CPU to send the next byte. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).
$\overline{STB}$ pulses low	L	L	

*Port C can be read by the CPU at any time, allowing polled operation instead of interrupt driven operation.

• Handshaking Signals

In the Strobed mode of operation, the lower 3-bits of port C transmit/receive the handshake signals (PC0 = $\overline{INTR}$, PC1 = BF, PC2 = $\overline{STB}$).

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the NSC831 to the CPU. In strobed input mode, the CPU reads the valid data at port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing data to port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving it the ability to control strobed data transfer. It is enabled or disabled, respectively, by setting or clearing bit 2 of the port C output data latch ($\overline{STB}$).

PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation.

Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear registers. The port C byte write command will not alter the output data latch of PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active low input from the peripheral device, signalling a data transfer. The NSC831 latches data on the rising edge of $\overline{STB}$ if the port bit is an input and the peripheral should latch data on the rising edge of $\overline{STB}$ if the port bit is an output.

BF (Buffer Full) is a high active output from the NSC831. For input port bits, it indicates that new data has been received from the peripheral. For output port bits, it indicates that new data is available for the peripheral.

Note: In either input or output mode the BF may be cleared by rewriting the MDR.

9.0 NSC831/883B MIL-STD-883 Class B Screening

National Semiconductor offers the NSC831D and NSC831E with full class B screening per MIL-STD-883 for Military/ Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

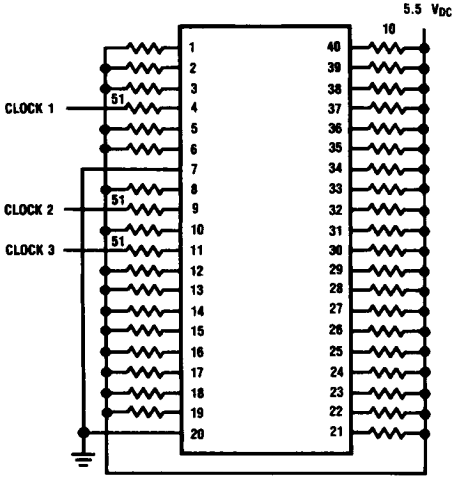
Electrical testing is performed in accordance with RETS831X, which tests or guarantees all of the electrical performance characteristics of the NSC831 data sheet. A copy of the current revision of RETS831X is available upon request. The following table is the MIL-STD-883 flow as of the date of publication.

100% Screening Flow

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010 B	100%
Stabilization Bake	1008C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010C 10 Cycles −65°C/ +150°C	100%
Constant Acceleration	2001E 30,000 Gs, Y1 Axis	100%
Fine Leak	1014 A or B	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS831X	100%
PDA	5% Max	
	+125°C AC and DC per RETS831X	100%
	−55°C AC and DC per RETS831X	100%
	+25°C AC per RETS831X	100%
QA Acceptance	5005	Sample per
Quality Conformance		Method 5005
External Visual	2009	100%

10.0 Burn-In Circuit

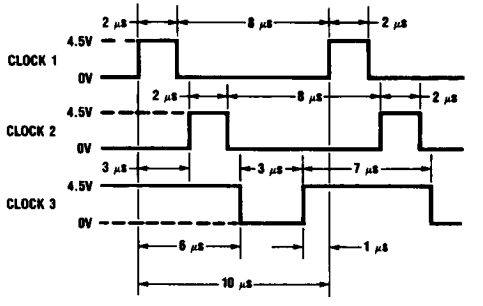
5242HR
NSC831AD/883B (Dual-In-Line)



TL/C/5594–13

11.0 Timing Diagram

Input Clocks



TL/C/5594–14

Note 1: All resistors ±5%, ¼ watt unless otherwise designated, 125°C operating life circuit.

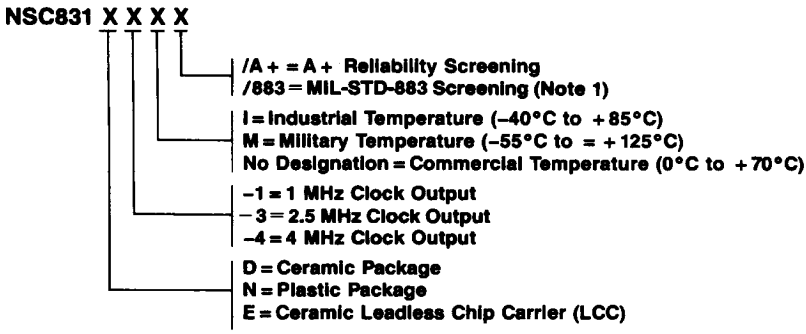
Note 2: E package burn-in circuit 5244HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V.

Note 5: Device to be cooled down under power after burn-in.

12.0 Ordering Information



TL/C/5594–15

Note 1: Do not specify a temperature option: all parts are screened to military temperature.

13.0 Reliability Information (NSC831)

Gate Count 1900
Transistor Count 7400