SIGNAL PROCESSING TECHNOLOGIES

HADC674Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI674A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 15 µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A. Included on chip are an internal reference, clock, and a sample-and-hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15 µs (max) conversion time of 10 or 20 volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit µP bus.

The HADC674Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

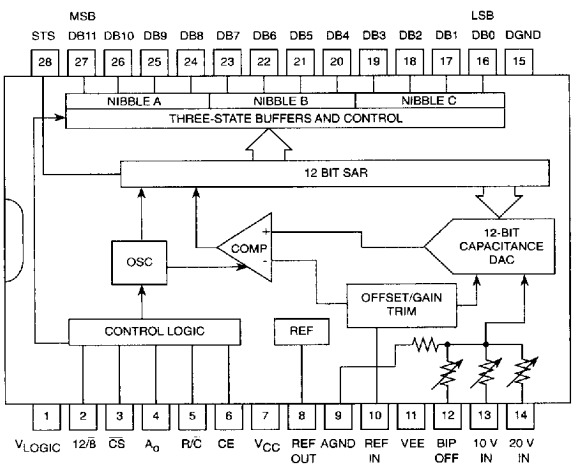
The BEMOS process and monolithic construction reduces power consumption and ground noise and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than that of currently available devices, and a negative power supply is not needed.

A standard military drawing is published under DESC number 5962-91690.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) ..... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) ..... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) ..... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) ..... ±16.5 V
20 V Vin Input Voltage (to AGND) ..... ±24 V

Output

Reference Output Voltage ..... Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation ..... 1000 mW
Thermal Resistance (θ_{jA}) ..... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	Bits
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	VI	11			12			12			Bits
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V, ±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5 -10		+5 +10	-5 -10		+5 +10	-5 -10		+5 +10	Volts Volts
Unipolar		VI	0 0		+10 +20	0 0		+10 +20	0 0		+10 +20	Volts Volts
Input Impedance 10 Volt Span 20 Volt Span		VI	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 kΩ kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not required for circuit operation											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation											
Power Dissipation +15 V, +5 V		 VI	 	 110	 150	 	 110	 150	 	 110	 150	 mW
Internal Reference Voltage Output Current[4]		VI VI	9.97	10	10.03 2	9.97	10	10.03 2	9.97	10	10.03 2	Volts mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		VI	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		VI	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	VI		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	VI			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	VI	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	VI	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads; external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

ELECTRICAL SPECIFICATIONS

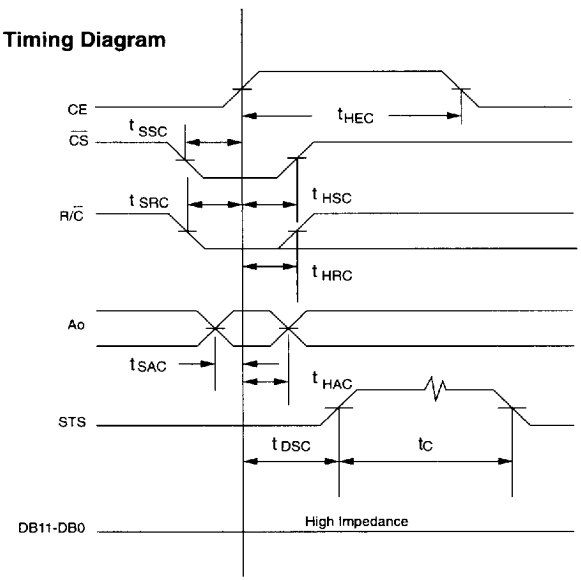
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[5]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	9	13	15	9	13	15	9	13	15	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	6	8	10	6	8	10	6	8	10	µs

Note 5: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

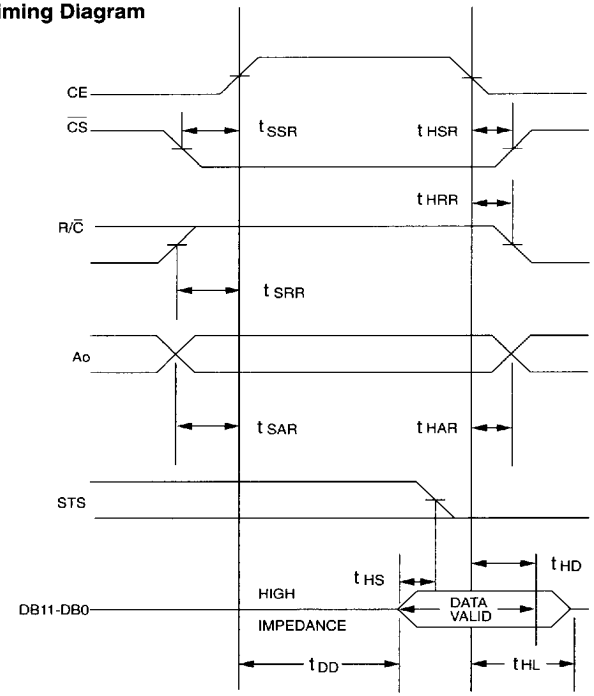
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 6: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370

ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE-AND-HOLD												
Acquisition Time		IV	1.2	1.7	2.0	1.2	1.7	2.0	1.2	1.7	2.0	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

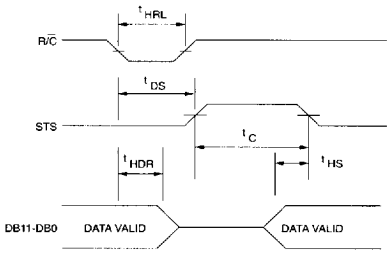
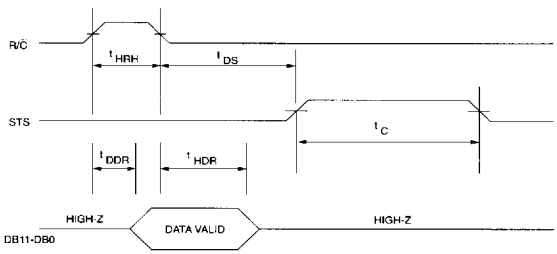


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from zero through full scale with all offset errors nulled out. (See figures 5 and 6.) The point used as zero occurs 1/2 LSB (1.22 mV for a 10 volt span) before the first code transition (all zeros to only the LSB on). Full scale is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value that falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value that falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification that guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type AC, BC, AM and BM grades that guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present. In practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

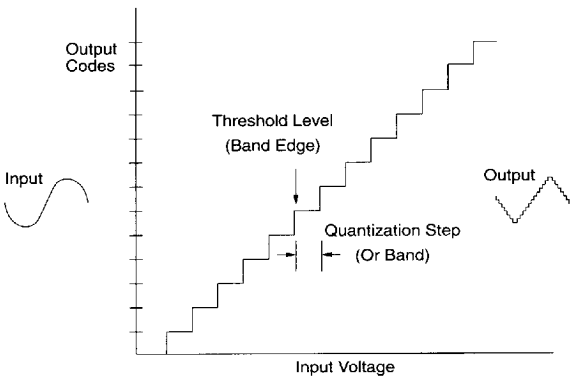
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q=FSR/2^N$ where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors. (See figures 5, 6 and 7.)

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

Figure 6 - Dynamic Conditions

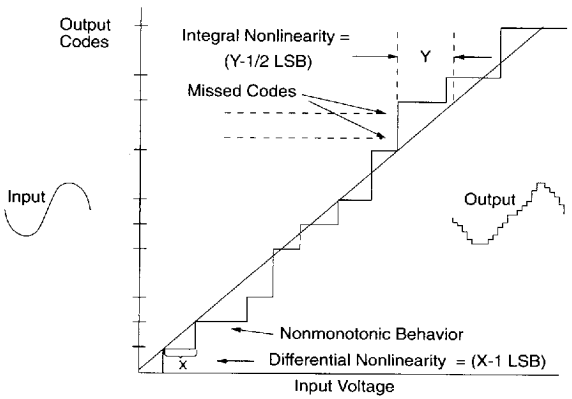
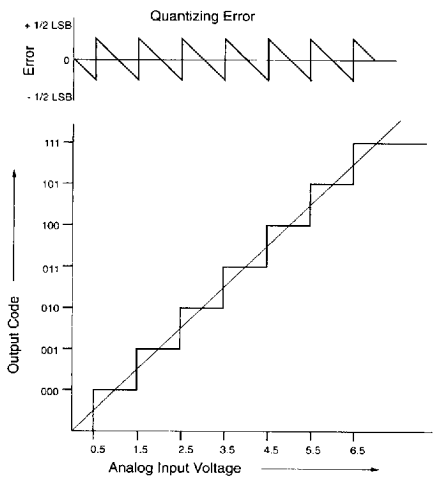


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

Gain is the slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample-and-hold function.

APERTURE JITTER

This is a specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates that converts high frequency signals with great accuracy. A sample-and-hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

This is the time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12 bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to one least significant bit (LSB) of the full scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates nonmonotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit analog-to-digital converter that consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample-and-hold, clock, output buffers and control circuitry to make possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it cannot be stopped or restarted and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC674Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample-and-hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

Note that even though the user may use an external sample-and-hold for very high frequency inputs, the internal sample-and-hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample-and-hold. This prevents transients occurring during conversion from being inflicted upon the attached sample-and-hold buffer. All other 674 circuits will cause a transient load current on the sample-and-hold which will upset the buffer output and may add error to the conversion itself.

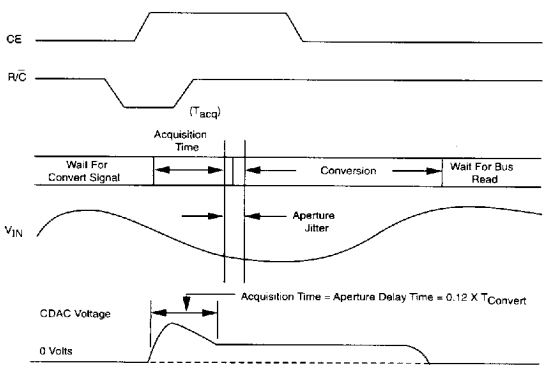
Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample-and-hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE-AND-HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC674Z and is controlled through the normal R/$\overline{C}$ control line. (Refer to figure 8.) When the R/$\overline{C}$ line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first two clock cycles are allocated to signal acquisition of the input by the CDAC. (This time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

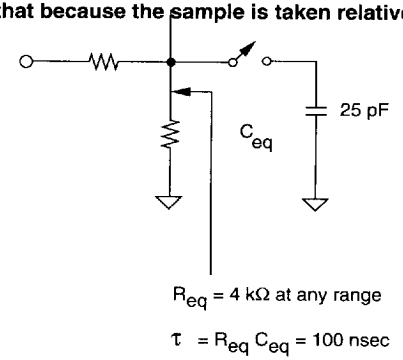
Figure 8 - Sample-and-hold Function



During T_{acq}, the equivalent circuit of the HADC674Z input is as shown in figure 9. (The time constant of the input is independent of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC674Z Input Circuit

Note that because the sample is taken relative to the R/$\overline{C}$ transition, T_{acq} is also the traditional "aperture delay" of this internal sample-and-hold.



Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =1.7 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate are included in the overall specifications for the HADC674Z.

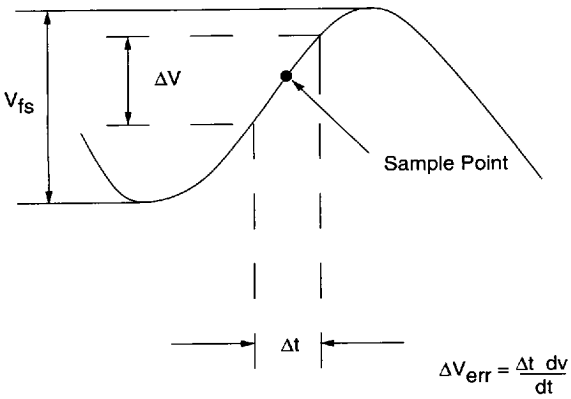
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample-and-hold is the uncertainty in the time that the actual sample is taken, i.e., the aperture jitter or T_{AJ}. The HADC674Z has a nominal aperture jitter of 8 nsec between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point. (See figure 10.) The magnitude of this change for a sine wave can be calculated:

$V_{err} \leq V_{fs}/2^{N+1}$ (where V_{err} is the allowable error voltage and V_{fs} is the full scale voltage)

Figure 10 - Aperture Uncertainty



From figure 10:

$SR=\Delta V/\Delta t=2\ \pi fVp$

Let $\Delta V = V_{err} = V_{fs}\,(2 - (N+1))$, $Vp = Vin/2$ and $\Delta t = t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{(N+1)} \geq \pi f V_{in}\ t_{AJ}$ or $f_{MAX} \leq V_{fs}/(\pi Vin\ t_{AJ})2^{(N+1)}$

For the HADC674Z, t_{AJ}=8 nsec, therefore $f_{max} \leq$5 kHz.

For higher frequency signal inputs, an external sample-and-hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in figure 11 and 12. The two typical interface circuits are for operating the HADC674Z in either an unipolar or bipolar input mode. Information on these connections and on conditions concerning board layout to achieve the best operation are discussed below.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as closely to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) are sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC. The analog and digital common pins should be tied together as closely to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370
SPT

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resistor and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

BIPOLAR

The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2. (See figure 12.) If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 with a 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 with a 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 11 - Unipolar Input Connections

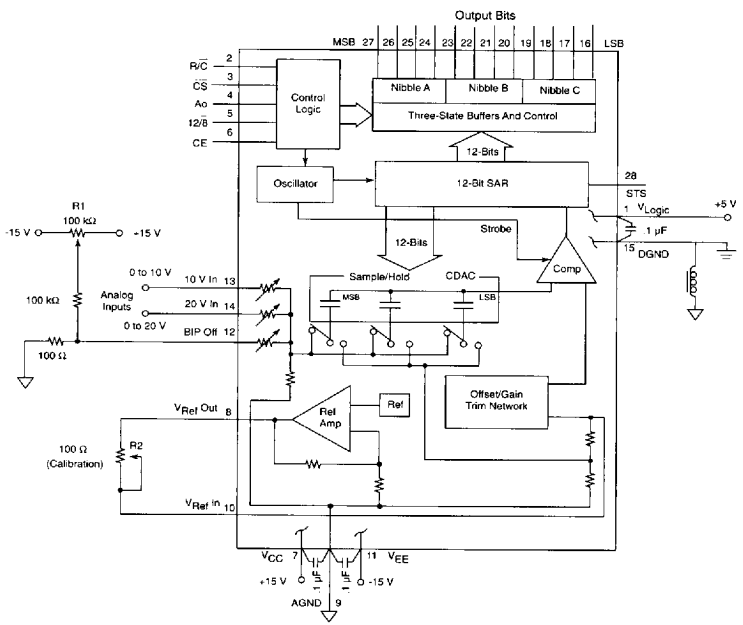
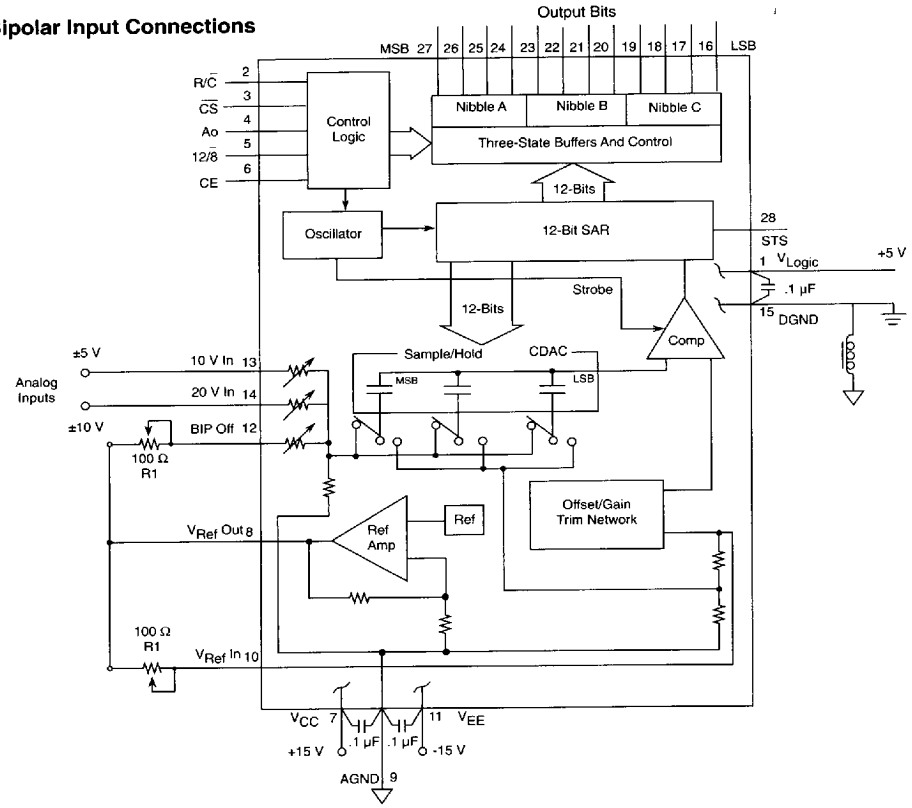


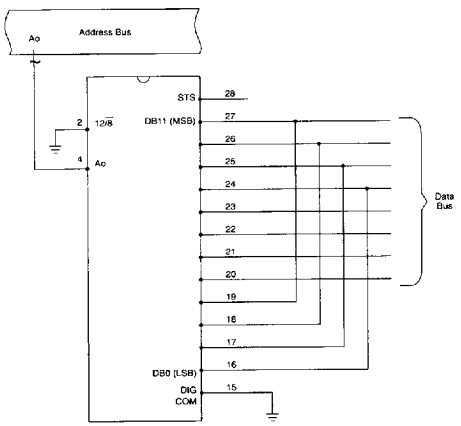
Figure 12 - Bipolar Input Connections



CONTROLLING THE HADC674Z

The HADC674Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the stand-alone mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 bits followed by 4 bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in table I, and the internal control logic is shown in a simplified schematic in figure 14.

Figure 13 - Interfacing the HADC674Z to an 8-bit Data Bus



4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Table I - Truth Table for the HADC674Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in figure 13 and table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic 1. Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

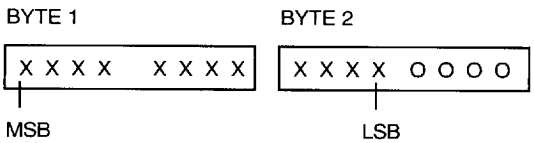
CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be set up at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This results in east interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is left justified data as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in figure 13 will never be enabled at the same time.

In figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

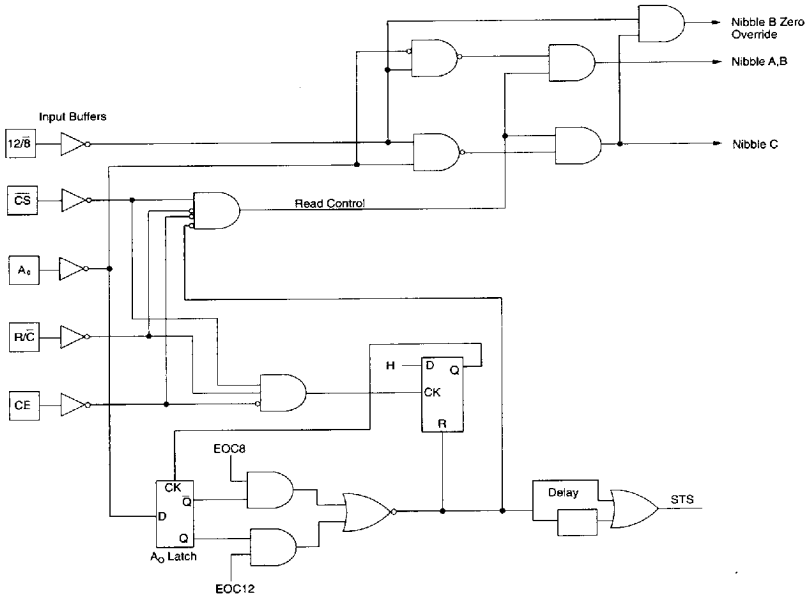
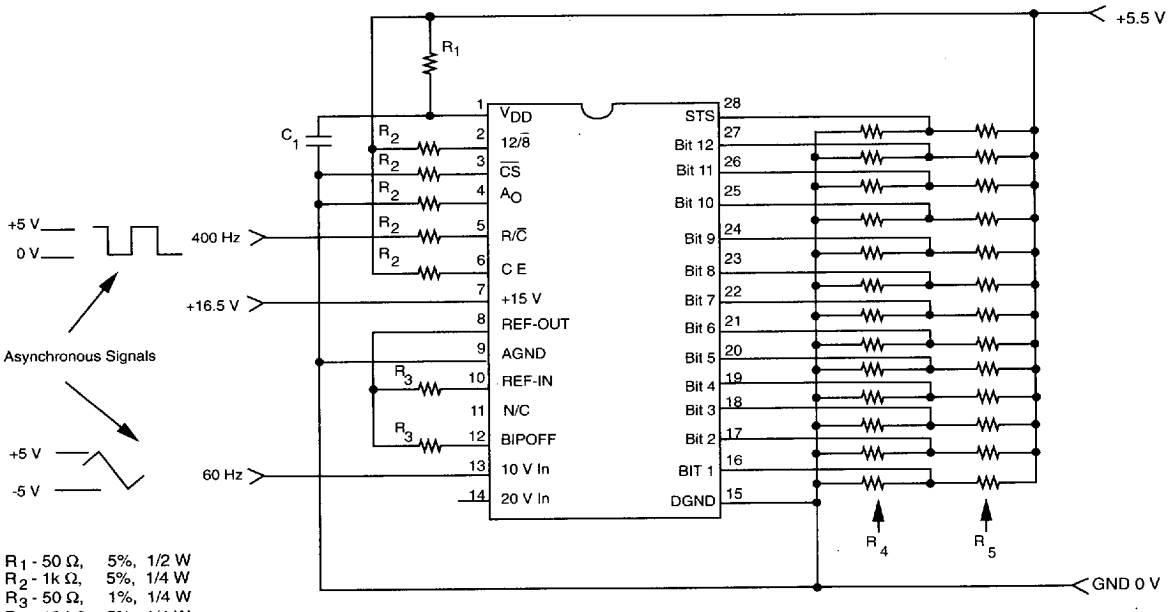


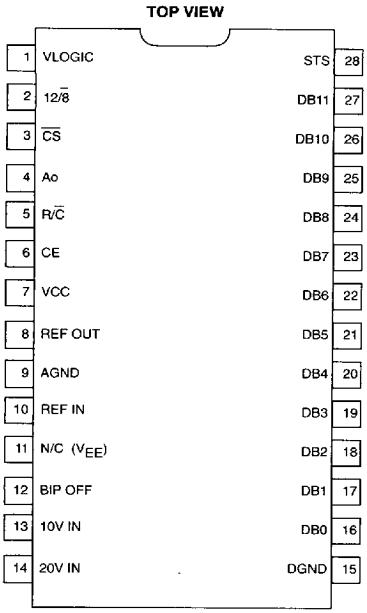
Figure 15 - Burn-In Schematic



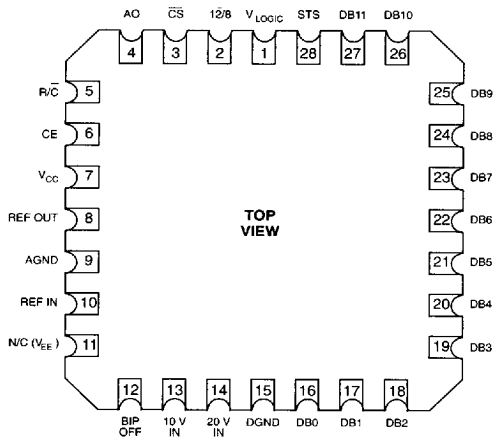
R_1 - 50 Ω, 5%, 1/2 W
R_2 - 1k Ω, 5%, 1/4 W
R_3 - 50 Ω, 1%, 1/4 W
R_4 - 10 kΩ, 5%, 1/4 W
R_5 - 3.3 kΩ, 5%, 1/4 W
C_1 - 1 µF, 5%

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370
SPT

PIN Assignment HADC674Z



28 LEAD DIP



28 Lead LCC

PIN Functions HADC674Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
$\overline{CE}$	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lids on the sidebrazed and LCC packages are internally connected to AGND.