HADC77100

8-BIT, 150 MSPS FLASH A/D CONVERTER

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- 150 MSPS Conversion Rate
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

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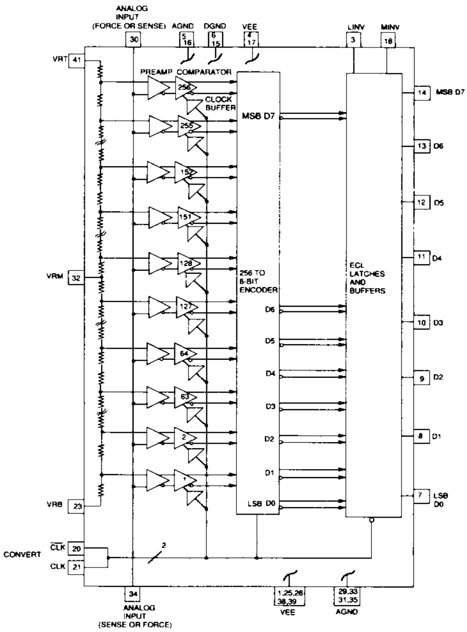
GENERAL DESCRIPTION

The HADC77100 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal with full scale frequency components to 50 MHz into 8-bit digital words at a 150 MSPS (TYP) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time and wide bandwidth. A single standard -5.2 volt power supply is required for operation of the HADC77100, with nominal power dissipation of 2.2 Watts. The part is packaged in a 42 Lead Ceramic Sidebrazed DIP which is pin compatible with the CX20116. Careful attention to the design and layout has provided a device with better linearity, lower noise floor, stable input characteristics, and lower data error rates. The HADC77100 is available in industrial and military temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
Negative Supply Voltage (V_{EE} TO GND) .... -7.0 to +0.5 V
Ground Voltage Differential .... -0.5 to +0.5 V

Input Voltage
Analog Input Voltage .... +0.5 V to V_{EE}
Reference Input Voltage .... +0.5 V to V_{EE}
Digital Input Voltage .... +0.5 V to V_{EE}
Reference Current VRT to VRB .... 25 mA

Output
Digital Output Current .... 0 to -25 mA

Temperature
Operating Temperature, ambient .... -65 to +105 °C
case .... +125 °C
junction .... +150 °C
Lead Temperature, (soldering 10 seconds). .... +300 °C
Storage Temperature .... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
DC ELECTRICAL CHARACTERISTICS										
Integral Linearity, 77100A	T_A = -25 to +85 °C	II			±1/2		±1/2		±1/2	LSB
	T_A = -55 to T_C	I			±1/2		±3/4		±3/4	LSB
Differential Linearity, 77100A (No missing codes)	T_A = -25 to +85 °C	II			±1/2		±1/2		±1/2	LSB
	T_A = -55 to T_C	I			±1/2		±3/4		±3/4	LSB
Integral Linearity, 77100B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77100B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT	T_A = -25 to +85 °C	II			±30		±30		±30	mV
	T_A = -55 to T_C	I			±30		±30		±30	mV
Offset Error VRB	T_A = -25 to +85 °C	II			±30		±30		±30	mV
	T_A = -55 to T_C	I			±30		±30		±30	mV
Input Voltage Range	T_A = -25 to +85 °C	II	-2.0		0.0	-2.0	0.0	-2.0	0.0	Volts
	T_A = -55 to T_C	I	-2.0		0.0	-2.0	0.0	-2.0	0.0	Volts
Input Capacitance	Over full input range	V		45						pF
Input Resistance		V		100						kΩ
Input Current	T_A = -25 to +85 °C	II		300	500		450		650	µA
	T_A = -55 to T_C	I		300	500		400		750	µA
Clock Synchronous Input Currents		V		40						µA
Supply Current	T_A = -25 to +85 °C	II		420	505		525		505	mA
	T_A = -55 to T_C	I		420	505		535		505	mA
Power Dissipation		II		2.18	2.63		2.73		2.63	mA
Ladder Resistance	T_A = -25 to +85 °C	II	100		300	100	300	80	300	Ω
	T_A = -55 to T_C	I	100		300	130	300	60	300	Ω
Reference Bandwidth		V		50						MHz

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
DIGITAL CHARACTERISTICS										
Output High Voltage	50 Ω to -2 V									
	T_A = -25 to +85 °C	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	Volts
	T_A = -55 to T_C	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	Volts
Output Low Voltage	50 Ω to -2 V									
	T_A = -25 to +85 °C	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	Volts
	T_A = -55 to T_C	I	-1.95	-1.80	-1.65	-1.95	-1.65	-2.00	-1.70	Volts
Input High Voltage (MINV, LINV)	T_A = -25 to +85 °C	II	-1.13		-0.81	-1.07	-0.67	-1.19	-0.87	Volts
	T_A = -55 to T_C	I	-1.13		-0.81	-1.07	-0.67	-1.22	-0.87	Volts
Input Low Voltage (MINV, LINV)	T_A = -25 to +85 °C	II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
	T_A = -55 to T_C	I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
AC ELECTRICAL CHARACTERISTICS										
Maximum Sample Rate	T_A = -25 to +85 °C	IV	125	150		125		125		MSPS
	T_A = -55 to T_C	I	100	150		100		100		MSPS
Clock Low Width, TPW0	T_A = -25 to +85 °C	II	5	3						ns
	T_A = -55 to T_C	I	5	3		5		5		ns
Clock High Width, TPW1	T_A = -25 to +85 °C	II	5	3						ns
	T_A = -55 to T_C	I	5	3		5		5		ns
Output Delay, TD	Differential Clock	V	3	4.2	5					ns
Output Delay Tempco	Differential Clock	V		15						ps/°C
Large Signal Bandwidth	Vin = F.S.	V		100						MHz
Small Signal Bandwidth	Vin=500 mV PP	V		175						MHz
Aperture Jitter		V		12						ps
Aperture Delay	Differential Clock T_A = -25 to +85 °C	V	0.3	1.8	2.3					ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C
Aperture Time		V		<100						ps
Acquisition Time	F.S. to ±1/2 LSB	V		5						ns
Input Slew Rate		V		800						V/µs
Total Dynamic Error	Vin = FS @ 3.58 MHz									
	T_A = -25 to +85 °C	I	44.2	48						dB
	T_A = -55 to T_C	I	44.2	48		43.2		43.5		dB
Total Dynamic Error, 77100A	Vin = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	28.2	33						dB
	T_A = -55 to T_C	I	28.2	33		27		27		dB
Signal to Noise Ratio	Vin = FS @ 3.58 MHz									
	T_A = -25 to +85 °C	I	46	49						dB
	T_A = -55 to T_C	I	46	49		45		45		dB

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
AC ELECTRICAL CHARACTERISTICS										
Signal to Noise Ratio, 77100A	Vin = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	33	38						dB
	T_A = -55 to T_C	I	33	38		32.5		32.5		dB
Total Harmonic Distortion	Vin = FS @ 3.58 MHz									
	T_A = -25 to +85 °C	I	49							dBc
	T_A = -55 to T_C	I	49	46		48		49		dBc
Total Harmonic Dist., 77100A	Vin = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	30	34						dBc
	T_A = -55 to T_C	I	30	34		27		28.5		dBc
Differential Gain	NTSC 40 IRE mod. ramp, Fc = 100 MSPS	V		1.0						%
Differential Phase	NTSC 40 IRE mod. ramp, Fc = 100 MSPS	V		.5						DEG

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

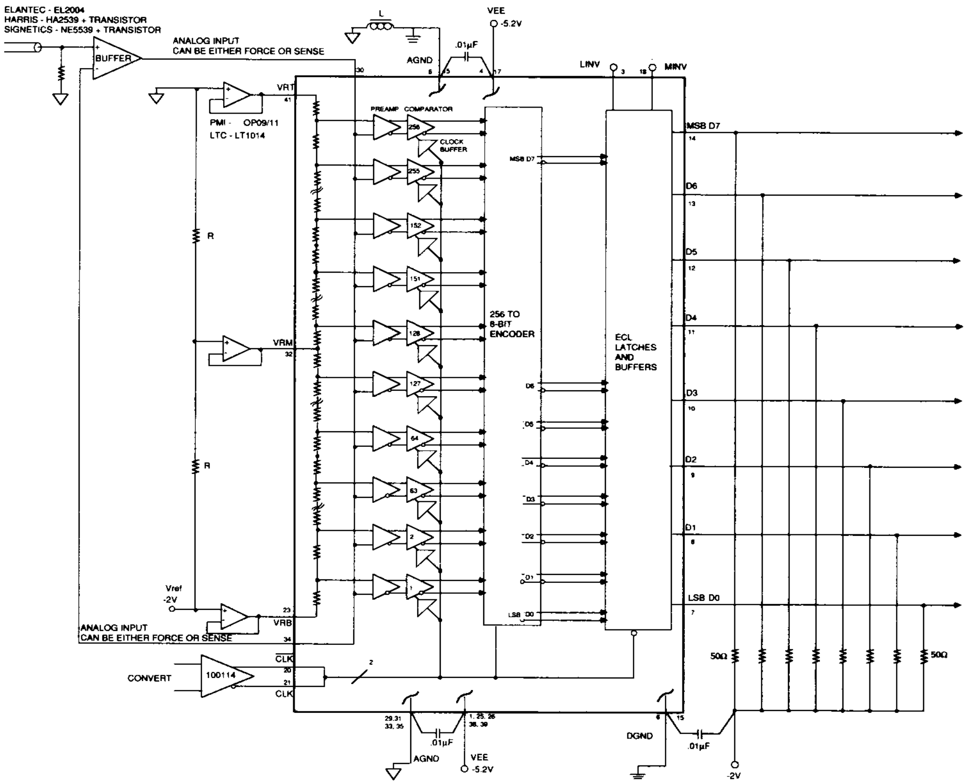
GENERAL DESCRIPTION

The HADC77100 is one of the fastest monolithic 8-bit parallel flash A/D converters available today. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 100 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash convertors. The preamplifiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The HADC77100 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77100 has an on board power supply bypass of 1500 pF to reduce external component needs. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Figure 5 - HADC77100 Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

The HADC77100 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 5 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 5.

VIN (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77100 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

CLK, $\overline{\text{CLK}}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{\text{CLK}}$ is internally biased to -1.3 V (see clock input circuit). It may be left open but a .01 µF bypass capacitor from $\overline{\text{CLK}}$ to AGND is recommended. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table II. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive 50 Ω to ECL levels when pulled down to -2 V When pulled down to -5.2 V the outputs can drive 130 Ω, to 1 kΩ loads.

VRB, VRM, VRT (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (VRB), mid-tap (VRM) and AGND (VRT). The reference pins and tap can be can be driven by op amps as shown in Figure 5 or VRM may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

N/C

All "Not Connected" pins should be tied to DGND on the left side of the package and to AGND of the right side of the package.

Table II - Output Coding

	MINV 0 LINV 0	MINV 0 LINV 1	MINV 1 LINV 0	MINV 1 LINV 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

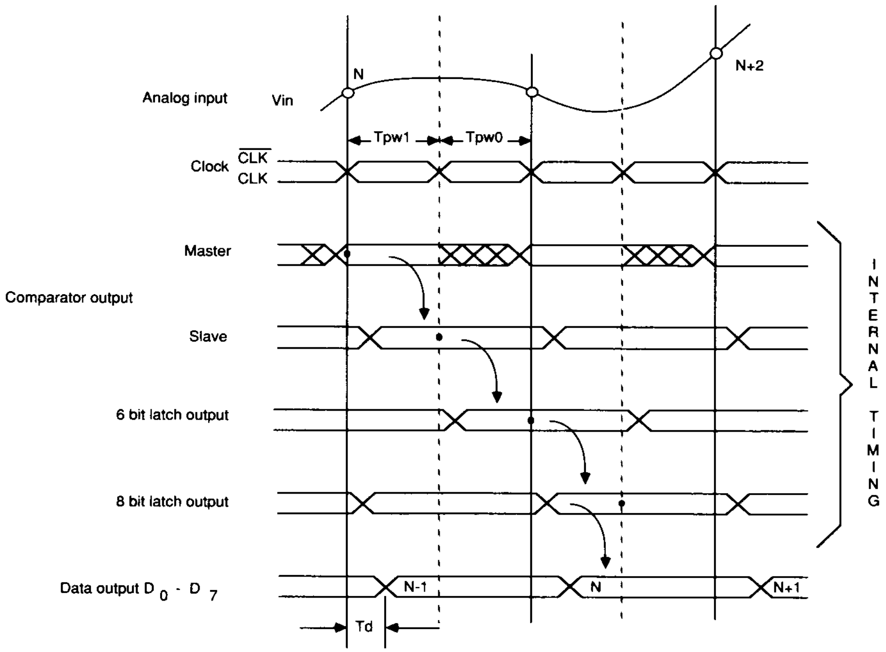
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

OPERATION

The HADC77100 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

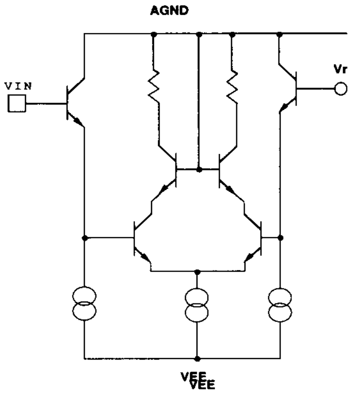
TIMING DIAGRAM



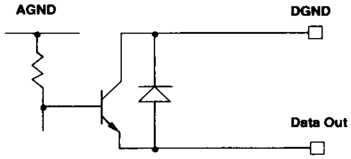
Dots (•) in the chart denote respective latch timings.

SUBCIRCUIT SCHEMATICS

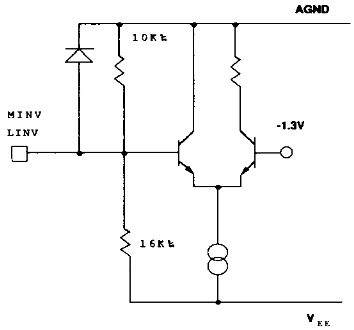
INPUT CIRCUIT



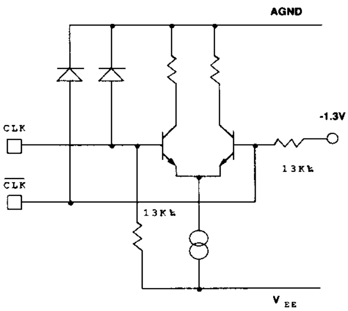
OUTPUT CIRCUIT



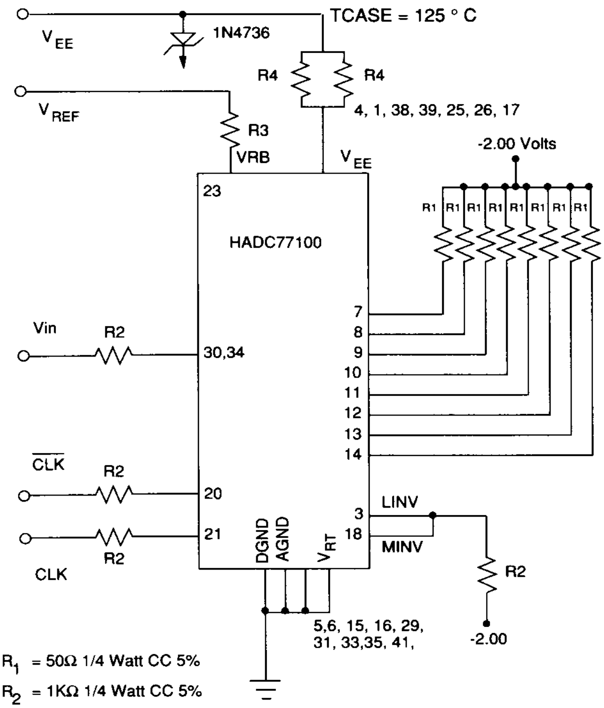
MINV, LINV INPUT CIRCUIT



CLOCK INPUT



BURN-IN CIRCUIT



R_1 = 50Ω 1/4 Watt CC 5%

R_2 = 1KΩ 1/4 Watt CC 5%

R_3 = 6.5Ω 1/4 Watt CC 5%

R_4 = 6.5Ω 1/2 Watt CC 5%

V_{REF} = -2.00 Volts

V_{EE} = -6.6 Volts

DEFINITION OF TERMS

A/D CONVERTER ERROR SUMMARY

SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 1B) while a static DC input level may appear close to the ideal (Figure 1A). That is why we are including many dynamic tests as well as the industry standard DC specifications.

TOTAL DYNAMIC ERROR (EFFECTIVE BITS)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These errors are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from the measured RMS error for the ideal sinewave and the measured actual RMS error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual RMS error}}{\text{ideal RMS error}}$$

Furthermore, total dynamic error (TDE) can be related to effective bits by the following formula:

$$\text{TDE(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = 8. Nonideal quantization bands represent differential nonlinearity errors see Figures 1A and 1B.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 1B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77100's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 1B points out two missed codes in the transfer function.

Figure 1A - Static Input Conditions

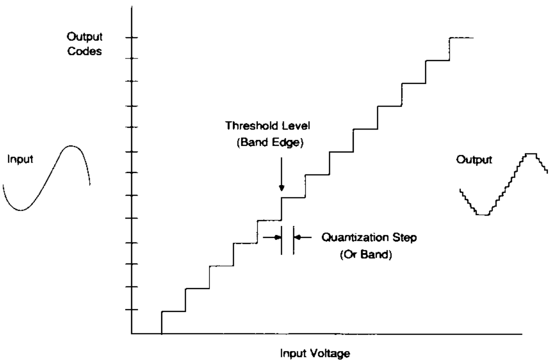
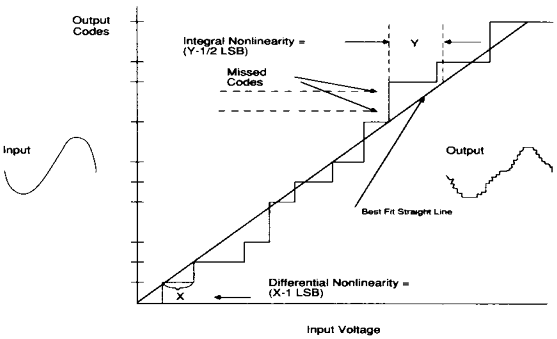


Figure 1B - Dynamic Conditions



INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 2A). Integral nonlinearity does not include any gain or offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 1B shows an integral nonlinearity error of 2 LSBs. The HADC77100's integral nonlinearity can be improved by using the external reference ladder tap as shown in Figure 5. The resulting effect on the linearity is shown in Figure 2B.

Figure 2A - Linearity Curve with no TAP adjustment

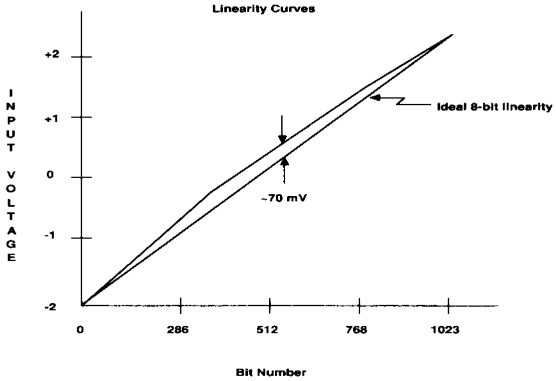
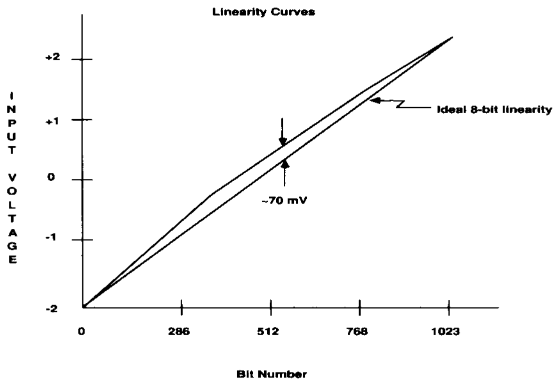


Figure 2B - Linearity Curve with TAP Forced to within .05 mV of Ideal



APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point see Figure 2C.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 3 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal waveforms.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10 MHz, then from Figure 3 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70 ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70 ps.

Aperture time and delay are very difficult to measure. However, these values are needed to make intelligent design decisions. SPT supplies these values for the HADC77100 based on both computer design simulations and verified by characterization of samples.

Figure 2C - Aperture Uncertainty

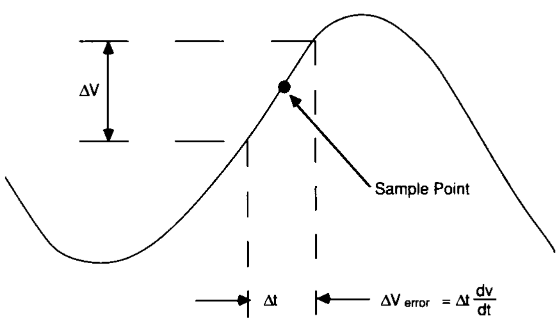
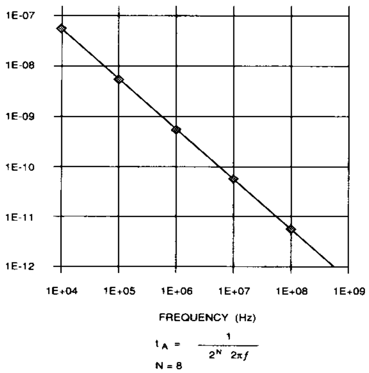


Figure 3 - Aperture Time - Sinewaves



CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 1.

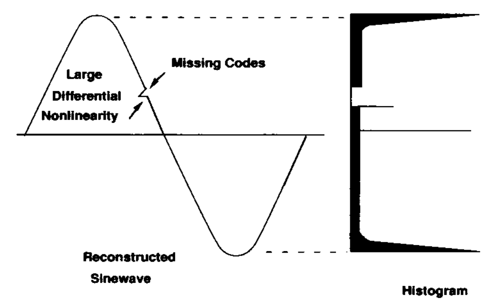
HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77100. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurrence along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts see Figure 4.

Figure 4 - Histogram Testing



In the histogram test, the A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table I.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77100. Using least squared error minimization techniques, an idealized sinewave fit to the data is calculated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A, f, q, DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave,

$$A_0\sin(2\pi f_0t+\theta_0)+DC_0$$

is then subtracted from the digitized time record. The RMS errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77100. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

DYNAMIC EVALUATION

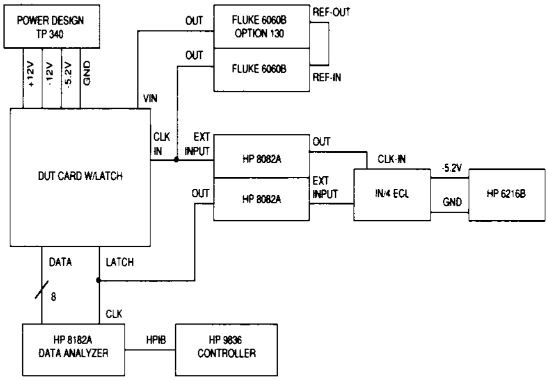


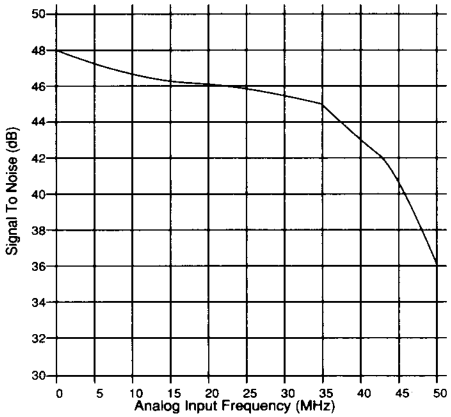
Table I - Tests

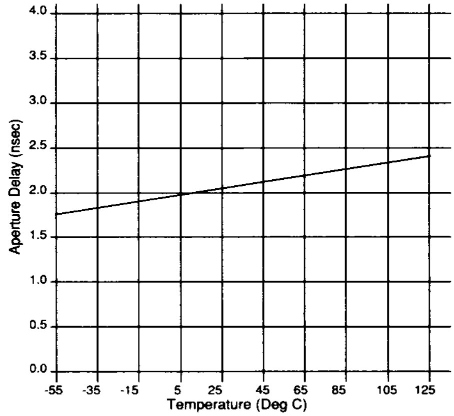
The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

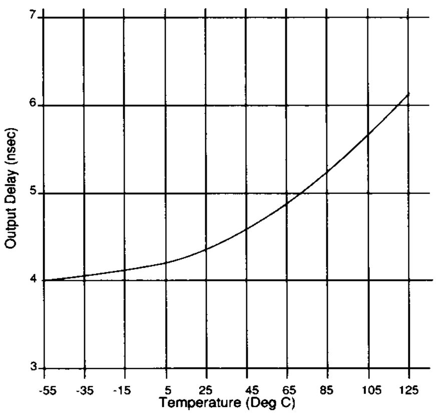
(Table from H.P. Product Note 5180A-2)

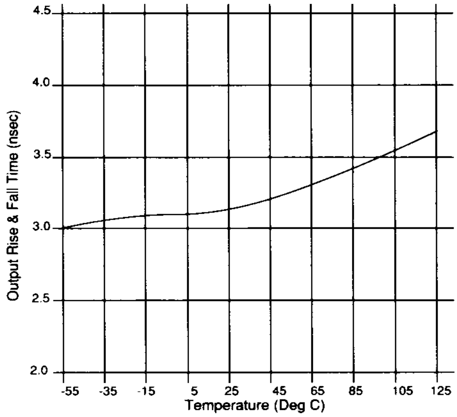
ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes.	Yes-shows up as elevated noise floor.	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts.	Yes-shows up as elevated noise floor.	Yes-part of RMS error	YES
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform).	Yes-shows up as harmonics of fundamental aliased into baseband.	Yes-part of RMS error	Yes
AAperature Uncertainty	No-averaged out. Can be measured with "phase locked" histrogram.	Yes-shows up as elevated noise floor.	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

CHARACTERIZATION GRAPHS



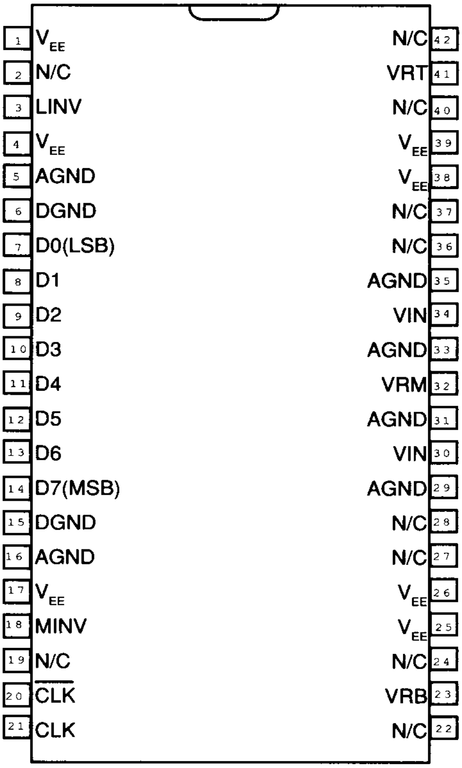






PIN ASSIGNMENT HADC77100

TOP VIEW



PIN FUNCTIONS HADC77100

NAME	FUNCTION
V_{EE}	Negative Supply Nominally -5.2 V
LINV	D0 through D6 Output Inversion Control Pin
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1~D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control
CLK	ECL Clock Input Pin
$\overline{CLK}$	ECL Clock Input Pin
VRB	Reference Voltage Bottom Nominally -2.0 V
AGND	Analog Ground
VIN	Analog Input Can be connected to the input signal or used as Sense
VRM	Reference Voltage Tap Middle
VRT	Reference Voltage, Top Nominally 0.0 V