

# HAT2093R

Silicon N Channel Power MOS FET  
High Speed Power Switching

# HITACHI

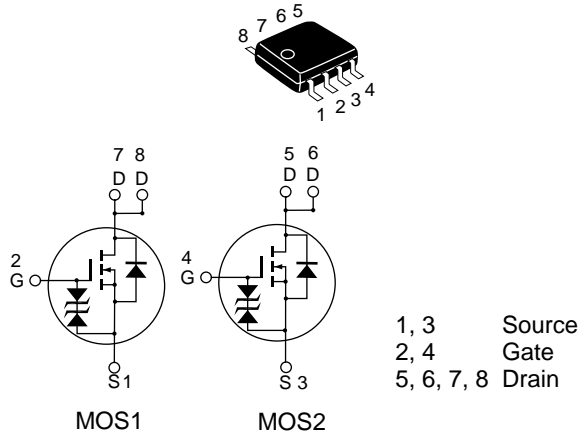
ADE-208-1237A (Z)  
2nd. Edition  
Jan. 2001

## Features

- Low on-resistance
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting

## Outline

SOP-8



**Absolute Maximum Ratings** ( $T_a = 25^{\circ}\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{\text{DSS}}$	30	V
Gate to source voltage	$V_{\text{GSS}}$	$\pm 20$	V
Drain current	$I_{\text{D}}$	9	A
Drain peak current	$I_{\text{D(pulse)}}^{\text{Note1}}$	72	A
Body-drain diode reverse drain current	$I_{\text{DR}}$	9	A
Channel dissipation	$P_{\text{ch}}^{\text{Note2}}$	2	W
Channel dissipation	$P_{\text{ch}}^{\text{Note3}}$	3	W
Channel temperature	$T_{\text{ch}}$	150	$^{\circ}\text{C}$
Storage temperature	$T_{\text{stg}}$	$-55$ to $+150$	$^{\circ}\text{C}$

Note: 1.  $PW \leq 10\mu\text{s}$ , duty cycle  $\leq 1\%$

2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10\text{s}$

3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10\text{s}$

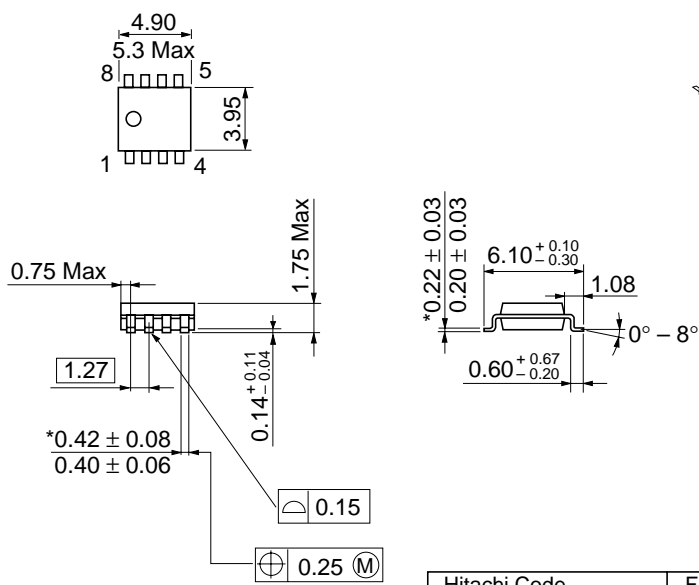
**Electrical Characteristics** (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10\text{V}$ , $I_D = 1\text{mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	18	23	$\text{m}\Omega$	$I_D = 4.5\text{A}$ , $V_{GS} = 10\text{V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	27	39	$\text{m}\Omega$	$I_D = 4.5\text{A}$ , $V_{GS} = 4.5\text{V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	9	15	—	S	$I_D = 4.5\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	750	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	$C_{oss}$	—	200	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	110	—	pF	$f = 1\text{MHz}$
Total gate charge	$Q_g$	—	12	—	nc	$V_{DD} = 10\text{ V}$
Gate to source charge	$Q_{gs}$	—	2.3	—	nc	$V_{GS} = 10\text{ V}$
Gate to drain charge	$Q_{gd}$	—	2.2	—	nc	$I_D = 9\text{ A}$
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$V_{GS} = 10\text{A}$ , $I_D = 4.5\text{A}$
Rise time	$t_r$	—	16	—	ns	$V_{DD} \cong 10\text{V}$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	$R_L = 2.22\Omega$
Fall time	$t_f$	—	7	—	ns	$R_g = 4.7\Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.85	1.10	V	$I_F = 9\text{A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	50	—	ns	$I_F = 9\text{A}$ , $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

Note: 4. Pulse test

Package Dimensions

As of January, 2001  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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