

HAT3004R

Silicon N and P Channel Power MOS FET

Application

High speed power switching

Features

- Low on-resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP-8DA
EIAJ Code	—
JEDEC Code	MS-012AA

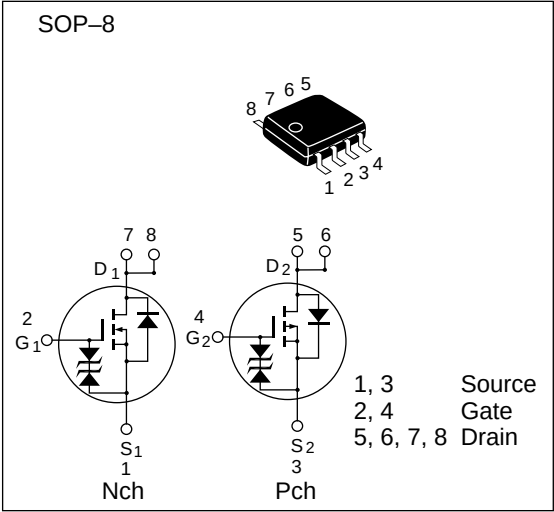


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V _{DSS}	30	−30	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	3.5	−2.5	A
Drain peak current	I _{D(pulse)} *	14	−10	A
Channel dissipation	P _{ch} ***	2.0		W
Channel dissipation	P _{ch} **	1.3		W
Channel temperature	T _{ch}	150		°C
Storage temperature	T _{stg}	−55 to +150		°C

* PW ≤ 10 μs, duty cycle ≤ 1 %

** 1 Drive operation : *** 2 Drive operation When using surface mounted on FR4 board

HAT3004R (N channel)

Table 2 Electrical Characteristics N Channel (Ta = 25°C)

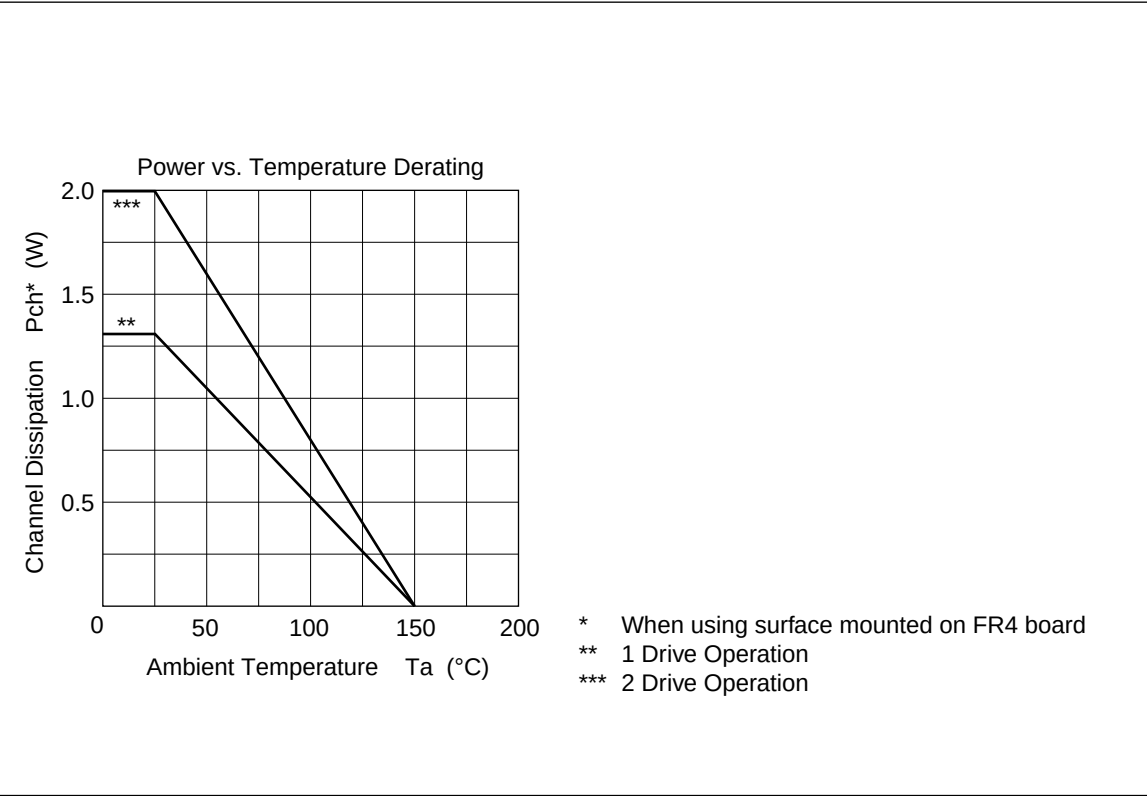
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.08)	0.1	Ω	$I_D = 2 \text{ A}$ $V_{GS} = 10 \text{ V}^*$
		—	(0.11)	0.15	Ω	$I_D = 2 \text{ A}$ $V_{GS} = 4 \text{ V}^*$
Forward transfer admittance	$ y_{fs} $	(2.0)	(3.0)	—	S	$I_D = 2 \text{ A}$ $V_{DS} = 10 \text{ V}^*$
Input capacitance	C_{iss}	—	(180)	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	(110)	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	(45)	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	(10)	—	ns	$V_{GS} = 4 \text{ V}$, $I_D = 2 \text{ A}$
Rise time	t_r	—	(60)	—	ns	$V_{DD} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	(25)	—	ns	
Fall time	t_f	—	(20)	—	ns	
Body-drain diode forward voltage	V_{DF}	—	(0.8)	—	V	$I_F = 3.5 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	$I_F = 3.5 \text{ A}$, $V_{GS} = 0$ $diF / dt = 20 \text{ A} / \mu\text{s}$

* Pulse Test

Table 2 Electrical Characteristics P Channel (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.13)	0.25	Ω	$I_D = -1 \text{ A}$ $V_{GS} = -10 \text{ V}^*$
		—	(0.2)	0.4	Ω	$I_D = -1 \text{ A}$ $V_{GS} = -4 \text{ V}^*$
Forward transfer admittance	$ y_{fs} $	(2.0)	(3.0)	—	S	$I_D = -1 \text{ A}$ $V_{DS} = -10 \text{ V}^*$
Input capacitance	C_{iss}	—	(250)	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	(150)	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	(60)	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	(10)	—	ns	$V_{GS} = -4 \text{ V}$, $I_D = -1 \text{ A}$
Rise time	t_r	—	(60)	—	ns	$V_{DD} = -10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	(20)	—	ns	
Fall time	t_f	—	(25)	—	ns	
Body-drain diode forward voltage	V_{DF}	—	(-0.8)	—	V	$I_F = -2.5 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	$I_F = -2.5 \text{ A}$, $V_{GS} = 0$ $diF / dt = 20 \text{ A} / \mu\text{s}$

* Pulse Test



Package Dimensions

Unit : mm

