H1853
H1853C

1800 CMOS Microprocessor Family
N-Bit 1 of 8 Decoder

HUGHES AIRCRAFT COMPANY

MICROELECTRONICS CENTER

DESCRIPTION

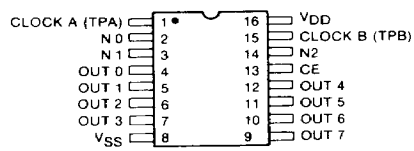
Hughes 1853 allows decoding of the 1802A microprocessor generated I/O lines (N0-N2) to provide direct control for up to seven input and seven output devices. The TPA and TPB clock inputs provide control signal output timing while the Chip Enable (CE) input allows multi-level I/O expansion for decoding. The 1853 can also be used as a general 1 of 8 decoder for memory system applications.

The 1853 operates over a 4-10.5 voltage range while the 1853C operates over a 4-6.5 voltage range. The 1853 is available in a 16 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request. form (H suffix) are available upon request.

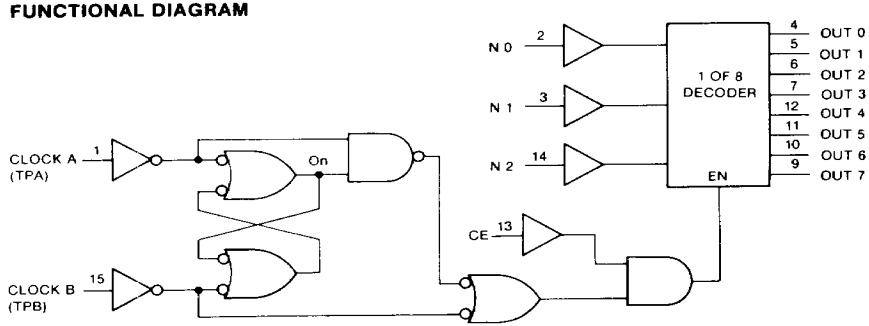
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor without Additional Components
- Provides Control for up to 7 Input and 7 Output Devices
- Low Power Dissipation
- Easy Expansion for Multi-Level I/O Systems through Chip Enable.
- Buffered Inputs and Outputs
- Strobed Outputs for Spike-Free Decoding

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to + 125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1853 ..... −0.5 to + 13 Volts
- 1853C ..... −0.5 to + 7 Volts

Input Voltage Range ..... V_{SS} −0.3V to V_{DD} + 0.3V

Storage Temperature Range (T_{stg}) ..... −65 to + 150°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = −55 to +125°C, V_{DD} = ±5%

Supply-Voltage Range	—	—	—	4	—	10.5	4	—	6.5	V
Recommended Input Voltage Range	—	—	—	VSS	—	VDD	VSS	—	VDD	V
Static Electrical Characteristics at T_A = −55°C to 125°C Unless Otherwise Specified										
Quiescent Device Current, I_L[4]	—	—	5	—	1	10	—	5	50	µA
	—	—	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	2.6	5.2	—	—	—	—	
Ouput High Drive (Source Current), I_{OH}	4.6	0,5	5	-1.15	-2.3	—	-1.15	-2.3	—	mA
	9.5	0,10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level, V_{OL}[1,3]	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}[3]	—	0,5	5	4.9	5	—	4.9	5	—	V
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
	1,9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	V
	1,9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}[4]	Any	0,5	5	—	—	±1	—	—	±1	µA
	Input	0,10	10	—	—	±1	—	—	—	
3-State Ouput Leakage Current, I_{OUT}[4]	0,5	0,5	5	—	—	±1	—	—	±1	µA
	0,10	0,10	10	—	—	±1	—	—	—	
Operating Current I_{DD1}[2,4]	0,5	0,5	5	—	50	500	—	50	100	µA
	0,10	0,10	10	—	150	1000	—	—	—	
Input Capacitance, C_{IN}[3]	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}[3]	—	—	—	—	10	15	—	10	15	pF

* Typical values are for T_A = +25°C and nominal voltage.

NOTE 1: I_{OL} = I_{OH} = 1 uA

NOTE 2: Operating current measured in a 1802A system at 2MHz with outputs floating.

NOTE 3: Design assured but not tested.

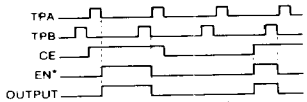
NOTE 4: Parameters guaranteed by other tests at −55°C.

OPERATING CONDITIONS, cont.

CHARACTERISTICS	CONDITIONS				LIMITS					UNITS
Dynamic Electrical Characteristics at T_A = −55 to +125°C, C_L = 50pF, V_{DD} = ±5%, V_{IH} = V_{DD}, V_{IL} = V_{SS}										
Propogation Delay Time:	—	—	5	—	175	275	—	175	275	ns
CE to Output, t_{EOH}, t_{EOL}	—	—	10	—	90	150	—	—	—	
N to Outputs, t_{NOH}, t_{NOL}	—	—	5	—	225	350	—	225	350	ns
	—	—	10	—	120	200	—	—	—	
Clock A to Output, t_{AO}	—	—	5	—	200	300	—	200	300	ns
	—	—	10	—	100	150	—	—	—	
Clock B to Output, t_{BO}	—	—	5	—	175	275	—	175	275	ns
	—	—	10	—	90	150	—	—	—	
Minimum Pulse Widths:	—	—	5	—	50	75	—	50	75	ns
Clock A, t_{CACA}	—	—	10	—	25	50	—	—	—	
Clock B, t_{CBCB} C8	—	—	5	—	50	75	—	50	75	
	—	—	10	—	25	50	—	—	—	

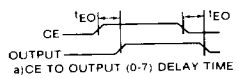
*Typical values are for TA = 25°C and nominal voltage.

TIMING DIAGRAMS

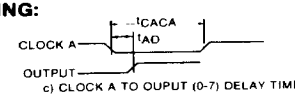


*OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY

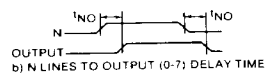
PROPOGATION DELAY TIMING:



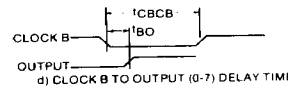
a)CE TO OUTPUT (0-7) DELAY TIME



c) CLOCK A TO OUPUT (0-7) DELAY TIME



b) N LINES TO OUTPUT (0-7) DELAY TIME



d) CLOCK B TO OUTPUT (0-7) DELAY TIME

APPLICATIONS EXAMPLES

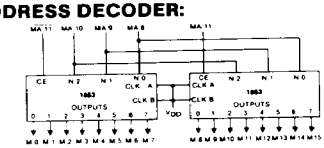
The Figure shows two 1853 used to decode 4K address into 16 groups of 256 address each.

MA 8 represents the 8th binary address bit. (i.e. 2^8 = 256)
M 0 will address 0-255
M 1 will address 256-511
M 15 will address 3840-4095

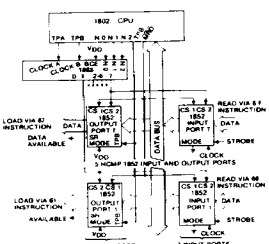
In the 1802A microprocessor systems, when more than three I/O ports are required, the N lines can be decoded to specify up to 7 different input and 7 different output channels as shown.

By executing Input instruction 69 (N lines = 001) for instance, the port 1 input register is enabled to the bus since MRD is high during the memory write cycle. The 1853 decode line 1 will also be active high during an output instruction, 61 (N lines = 001) but MRD is low during the memory read cycle disabling the memory read cycle disabling the port 1 input register from the bus. At TPB, the valid byte from memory is strobed into the port 1 output register.

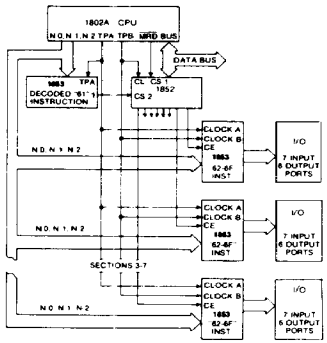
ADDRESS DECODER:



ONE LEVEL I/O SYSTEMS:



TWO LEVEL I/O SYSTEMS



In the 1802A microprocessor systems, when more than 7 input or 7 output ports are required, a two level I/O system can be designed as shown in the figure.

A 61 (N lines = 001) output instruction is first executed to place an 8-bit device selection code in the I/O device-select register, 1852. Subsequent execution of one of the 6 remaining output instructions (62-67) selects one of 48 output ports, or subsequent execution of one of the 7 input instructions (69-6F) selects one of the 56 input ports.

With additional decoding the total number of input and output ports can be further expanded.

SIGNAL DESCRIPTION

Clock A, Clock B: The selected outputs stay true from the trailing edge of the Clock A (TPA) input to the trailing edge of Clock B (TPB) input, if the chip is enabled. The transition of both the clock inputs at the trailing edge should be the high-to-low.

CE: The Chip Enable input enables the chip when high. All outputs will be low when CE = 0.

N 0, N 1, N 2: These three inputs select one of eight decoded outputs when the chip is enabled. N 0 is the least significant input, N 2 is the most significant input.

Output 0 - Output 7: One output can be selected at a time. The truth table is shown below.

TRUTH TABLE

CE	CLK A	CLK B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

1 = High Level
0 = Low Level
X = Don't Care
*Qn-1 = Enable remains in previous state.

N 2	N 1	N 0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

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