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Hitachi IC Memory
CompactFlash™/PC-ATA Standard

User's Manual

ADE-603-001
Rev. 1.0
11/27/97
Hitachi, Ltd.
Memory System Promotion Dept.

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Contents

Section 1 Flash Memory Cards

1.1 Introduction

As a flash memory card has no internal drive mechanism, it has the advantages of relatively low power consumption and greater tolerance of vibration when used in portable products in comparison with devices using hard disks or similar drive systems. This makes it an ideal storage medium for the age of mobile computing, in which machines are no longer confined to the desk top or the office. The flash memory card—or rather, various kinds of memory cards—first came to the attention of the market at virtually the same time as the advent of the early notebook personal computers.

Notebook PCs, with smaller memory and hard disk capacities than desktop machines, had to include provisions for the addition of memory and large-capacity auxiliary storage devices. These expansion slots later evolved into general-purpose slots that could accept fax/modem, LAN, and other kinds of cards, as well as flash memory cards. This marked the beginning of the PC card, as it is known in the market, and the electrical specifications, protocol, and mechanical form were established and standardized by PCMCIA*[1] (Personal Computer Memory Card International Association) and JEIDA*[2] (Japan Electric Industrial Development Association). The ability to incorporate the various functions mentioned above in a business-card-sized PC card is the result of remarkable advances in mounting technology and component miniaturization.

Similar advances were simultaneously being made in digital information devices of all kinds, and products began to appear of such small size as to make even the incorporation of a business-card-sized PC card difficult. Digital cameras and WindowsCE*[3] based handheld PCs are notable examples of such products.

Against this backdrop, SanDisk Corporation of the USA proposed a new flash memory card standard—CompactFlash™*[4]. This new standard has two special features: first , a postage-stamp size of 42.8 mm (H) × 36.4 mm (W) × 3.3 mm (T), giving a cubic capacity approaching 1/4 that of the PC card, and second, the use of the existing PC-ATA*[5] and True-IDE*[6] interface standards, providing a high degree of compatibility with notebook PCs and similar systems currently on the market. This compatibility allows system designers to use existing chip sets*[7] and know-how when designing new products using CompactFlash™, while the compact size offers a greater degree of freedom in terms of product design.

Note: * See Appendix C, Glossary.

Hitachi has released both cards compatible with the PCMCIA standard and cards compatible with the CompactFlash™ standard, using Hitachi flash memory. In the following descriptions, “CF” is used to refer to CompactFlash™, and “PC-ATA cards” to refer to cards compatible with the PCMCIA standard.

This user’s manual describes CF and PC-ATA card specifications and the use of these cards.

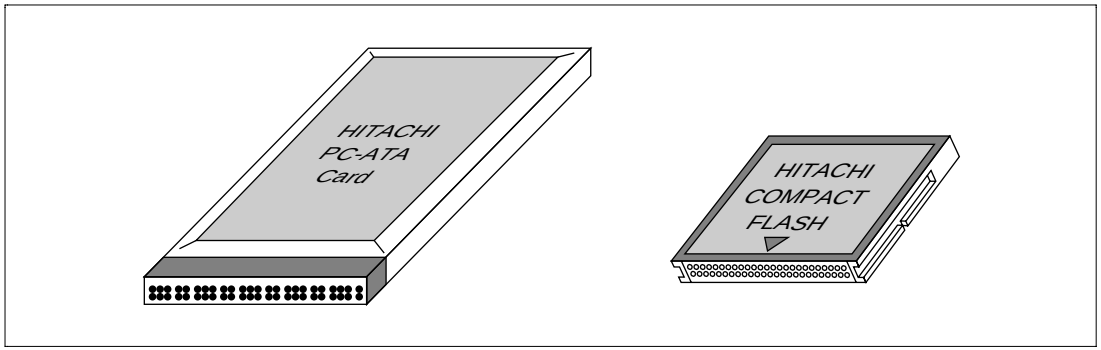


Figure 1.1 PC-ATA Card and CompactFlash™ Outlines

1.2 PCMCIA (JEIDA) and CFA

1.2.1 PCMCIA (Personal Computer Memory Card International Association)

The PCMCIA (Personal Computer Memory Card International Association) is the body that decides the physical and electrical specifications of PC cards.

A PC card is about the size of a business card, and uses a 68-pin two-piece connector. Moves to establish PC card standards date back to 1985 when JEIDA (Japan Electric Industrial Development Association) began drawing up standards for SRAM and other memory cards*[8]. The PCMCIA was established in 1989, with the participation of American personal computer manufacturers, including IBM and Apple. Since that time, the PCMCIA and JEIDA have worked jointly toward standardization. The world's first standard was PCMCIA 1.0/JEIDA 4.0, but this included areas lacking full compatibility. Also, since this standard was intended for memory cards, it could not be used for driving fax/modem and other I/O cards. This problem was solved with the creation of PCMCIA 2.0/JEIDA 4.2 in 1991, when the standard term "PC card" was adopted. At the present time, various kinds of cards are available, including SCSI, fax/modem, LAN, ISDN, HDD, and flash memory types.

A major advantage of PC cards is that, as long as a PC card slot is available, the card is basically independent of the type of machine. In other words, any PC card should work in any type of machine. In practice, however, this is not necessarily the case, owing to differences in PC card controllers and driver software.

Further information on PCMCIA standards is available from:

Personal Computer Memory Card International Association
2635 North First Street, Suite 209
San Jose, CA 95134, USA

Note: * See Appendix C, Glossary.

1.2.2 CFA (CompactFlash™ Association)

The CFA (CompactFlash™ Association) is a body established for the promotion of the new CompactFlash™ flash card standard proposed by SanDisk Corporation of the USA. CF is a trademark of SanDisk Corporation, and is licensed to the CFA. A CF card is of postage-stamp size, with an area of about 1/3 (and a cubic capacity of close to 1/4) that of a PC card, and also uses a smaller 50-pin two-piece connector. Electrically, it conforms to PCMCIA PC-ATA specifications and True-IDE specifications, offering an interface with an extremely high degree of compatibility that includes existing specifications.

Further information on the CFA is available from:

CompactFlash™ Association
PO Box 51537
Palo Alto, CA 94303
http:www.compactflash.org

1.2.3 PC-ATA and True-IDE Specifications

PC-ATA specifications and True-IDE specifications are both standards for handling flash cards and HDDs. Originally, these specifications all began with the IDE specifications*[10] which were devised as a means of directly connecting an HDD to the PC-AT bus*[11] (generally known as the ISA bus) used in the IBM-PC*[12].

The IDE standard, proposed by Western Digital Corporation and Compaq Corporation of the USA, came into widespread use because of the simplicity of its interface, but there was not always full compatibility between different companies' products. ANSI (American National Standards Institute*[16]) therefore drew up detailed standards based on the IDE specifications, covering virtually all areas from the shape of the connector to the software interface, with the aim of eliminating the problem of compatibility. These together comprise the ATA standard*[13]. The ATA standard is reviewed on an ad hoc basis to keep pace with advances in the PC field. The general enhanced IDE*[14] standard is currently designated ATA3. In general, an HDD described as IDE-compatible conforms to these ATA specifications. The *PC-ATA specifications*, for handling memory cards and HDDs, are the result of transporting the ATA standard into the PC card field. While the PC card standards offer an extremely high degree of general applicability in their support for cards of all kinds, including SCSI and LAN cards, tasks such as initialization and acquisition of card attributes have to be carried out by the host. Assuming that, for embedded applications, only a flash card can be used from the start, these PC card limitations (initialization and acquisition of card attributes) impose an extremely heavy burden on the system. It would therefore be useful to have a standard whereby a flash card behaves like an HDD as soon as the power is turned on. This demand is met by the *True-IDE standard*. The True-IDE standard thus falls outside the category of PC card standards. Consequently, although a flash card contains flash memory, its interface is the same as that for HDD control. To put it another way, a flash card cannot be controlled by treating it as flash memory.

Note: * See Appendix C, Glossary.

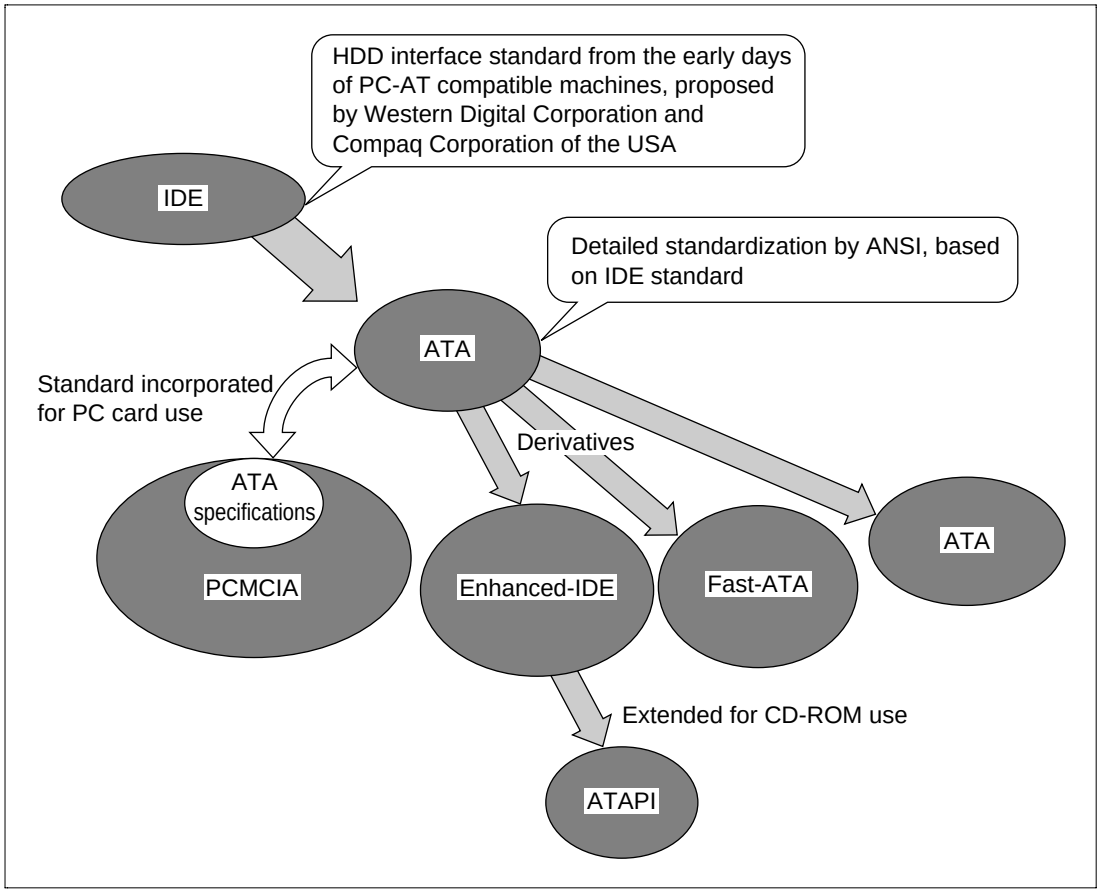


Figure 1.2 Evolution of ATA Standard

2.1 PC-ATA Card Specifications

Basic Specifications: Conformity to PC card specifications

- Interface
  Conformity to PCMCIA PC-ATA specifications
- External dimensions
  Conformity to PCMCIA specifications Type II (54.0 mm × 85.6 mm × 5.0 mm)

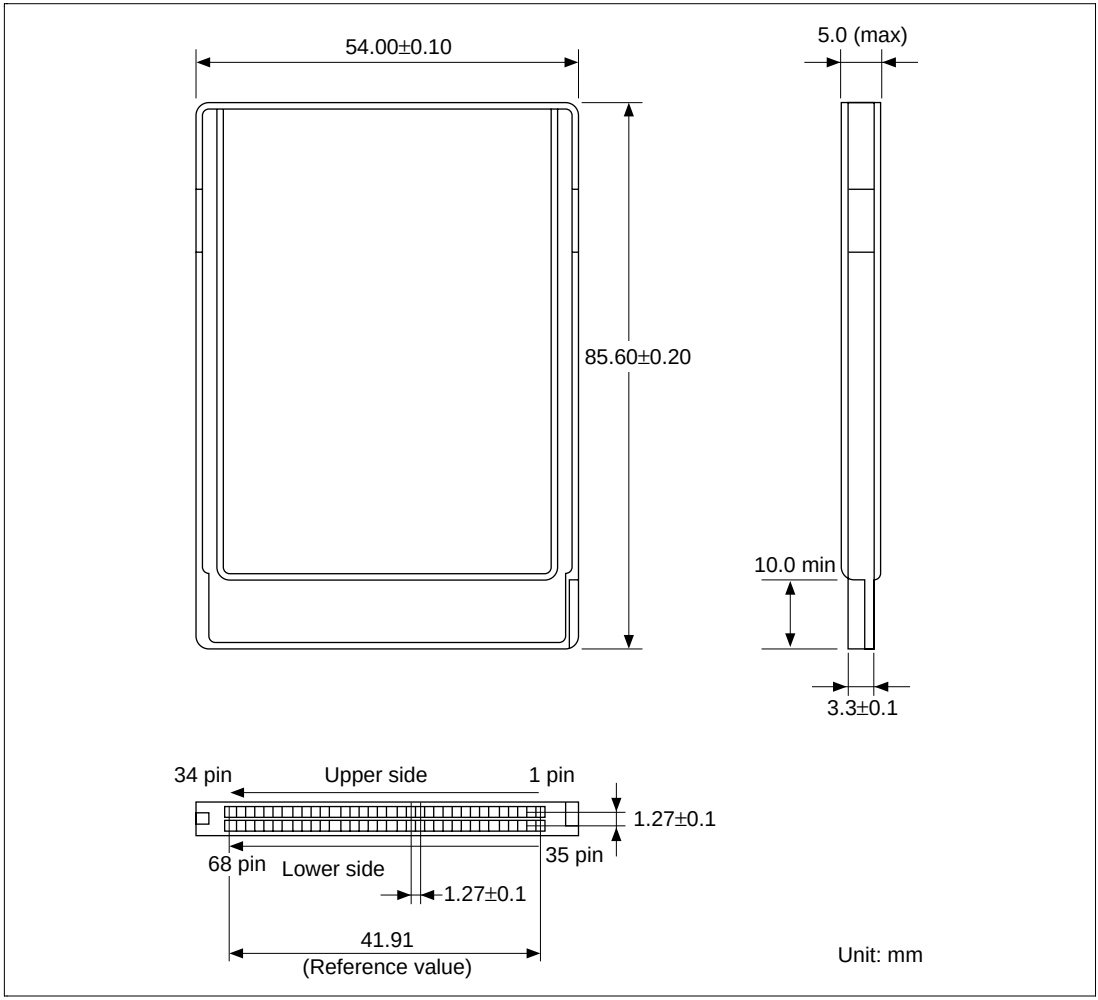


Figure 2.1 PC-ATA Specification External Dimensions

- Performance (representative example: HB286075A1)
  - Transfer speed: 8-Mbyte/second burst
  - Write speed: 250 kbytes/second
  - Guaranteed rewrites (per logical sector): 100,000
    (for rewriting of a DOS file of about 500 kB)
  - Error rate: Max. 10^{-14} bits

- Electrical characteristics, etc. (representative example: HB286075A1)
  - Power supply voltage: 3.3 V ±5%/5 V ±10%
  - Sleep/standby current: 2 mA/3 mA max.
  - Sector read/write current: 75 mA/100 mA max.
  - Operating temperature: 0 to +60°C
  - Storage temperature: –20 to +65°C

- Pin assignment table

Table 2.1 PC Card Specification Pin Assignments

	Mode			Mode	
	PCMCIA ATA			PCMCIA ATA	
Pin No.	Memory Card	I/O Card	Pin No.	Memory Card	I/O Card
1	GND	GND	35	GND	GND
2	D3	D3	36	$\overline{CD1}$	$\overline{CD1}$
3	D4	D4	37	D11	D11
4	D5	D5	38	D12	D12
5	D6	D6	39	D13	D13
6	D7	D7	40	D14	D14
7	$\overline{CE1}$	$\overline{CE1}$	41	D15	D15
8	A10	A10	42	$\overline{CE2}$	$\overline{CE2}$
9	$\overline{OE}$	$\overline{OE}$	43	$\overline{VS1}$	$\overline{VS1}$
10	—	—	44	RFU	$\overline{IORD}$
11	A9	A9	45	RFU	$\overline{IOWR}$
12	A8	A8	46	—	—
13	—	—	47	—	—
14	—	—	48	—	—
15	$\overline{WE}$	$\overline{WE}$	49	—	—
16	RDY/BUSY	$\overline{IREQ}$	50	—	—
17	V_{CC}	V_{CC}	51	V_{CC}	V_{CC}
18	—	—	52	—	—
19	—	—	53	—	—
20	—	—	54	—	—
21	—	—	55	—	—
22	A7	A7	56	—	—
23	A6	A6	57	$\overline{VS2}$	$\overline{VS2}$
24	A5	A5	58	RESET	RESET
25	A4	A4	59	$\overline{WAIT}$	$\overline{WAIT}$
26	A3	A3	60	RFU	$\overline{INPACK}$
27	A2	A2	61	$\overline{REG}$	$\overline{REG}$
28	A1	A1	62	BVD2	$\overline{SPKR}$
29	A0	A0	63	BVD1	$\overline{STSCHG}$
30	D0	D0	64	D8	D8
31	D1	D1	65	D9	D9
32	D2	D2	66	D10	D10
33	WP	$\overline{IOIS16}$	67	$\overline{CD2}$	$\overline{CD2}$
34	GND	GND	68	GND	GND

2.2 CompactFlash™ Specifications

Basic Specifications: Conformity to CompactFlash™ specifications

- Interface
  - — Conformity to PCMCIA PC-ATA specifications
    Support for memory mode and I/O mode
    * Can be mounted in a PC card slot, using an adapter.
  - — Conformity to True-IDE (True-Integrated Device Electronics) specifications

- External dimensions
  Conformity to CompactFlash™ specifications (42.8 mm × 36.4 mm × 3.3 mm)

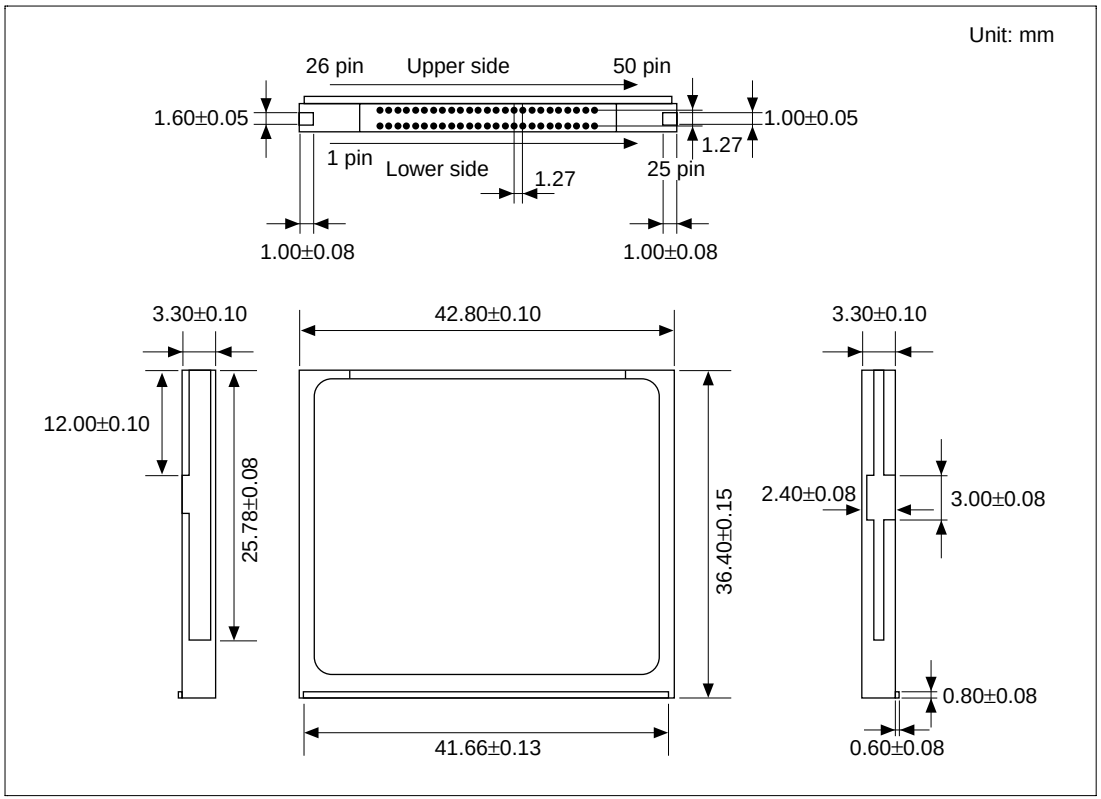


Figure 2.2 CompactFlash™ External Dimensions

- Performance (representative example: HB286015C2)
  - — Transfer speed: 8 Mbytes/second
  - — Write speed: 400 kbytes/second (8 MB: 250 kbytes/second)
  - — Guaranteed rewrites (per logical sector): 100,000
    (for rewriting of a DOS file of about 500 kB)
  - — Error rate: Max. 10^{-14} bits

- Electrical characteristics, etc. (representative example: HB286015C2)
  - — Power supply voltage: 3.3 V ±5%/5 V ±10%
  - — Sleep/standby current: 0.6 mA/1.0 mA max.
  - — Sector read/write current: 75 mA/100 mA max.
  - — Operating temperature: 0 to +60°C
  - — Storage temperature: –20 to +65°C

- Pin assignment table

Table 2.2 CompactFlash™ Pin Assignments

	Mode				Mode		
	PCMCIA ATA				PCMCIA ATA		
Pin No.	Memory Card	I/O Card	True-IDE	Pin No.	Memory Card	I/O Card	True-IDE
1	GND	GND	GND	26	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
2	D3	D3	D3	27	D11	D11	D11
3	D4	D4	D4	28	D12	D12	D12
4	D5	D5	D5	29	D13	D13	D13
5	D6	D6	D6	30	D14	D14	D14
6	D7	D7	D7	31	D15	D15	D15
7	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	32	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
8	A10	A10	A10	33	$\overline{VS1}$	$\overline{VS1}$	$\overline{VS1}$
9	$\overline{OE}$	$\overline{OE}$	$\overline{ATASEL}$	34	$\overline{IORD}$	$\overline{IORD}$	$\overline{IORD}$
10	A9	A9	A9	35	$\overline{IOWR}$	$\overline{IOWR}$	$\overline{IOWR}$
11	A8	A8	A8	36	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
12	A7	A7	A7	37	RDY/BUSY	$\overline{IREQ}$	INTRQ
13	V_{CC}	V_{CC}	V_{CC}	38	V_{CC}	V_{CC}	V_{CC}
14	A6	A6	A6	39	—	—	$\overline{CSEL}$
15	A5	A5	A5	40	$\overline{VS2}$	$\overline{VS2}$	$\overline{VS2}$
16	A4	A4	A4	41	RESET	RESET	$\overline{RESET}$
17	A3	A3	A3	42	$\overline{WAIT}$	$\overline{WAIT}$	IORDY
18	A2	A2	A2	43	—	$\overline{INPACK}$	$\overline{INPACK}$
19	A1	A1	A1	44	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
20	A0	A0	A0	45	BVD2	$\overline{SPKR}$	$\overline{DASP}$
21	D0	D0	D0	46	BVD1	$\overline{STSCHG}$	$\overline{PDIAG}$
22	D1	D1	D1	47	D8	D8	D8
23	D2	D2	D2	48	D9	D9	D9
24	WP	$\overline{IOIS16}$	$\overline{IOIS16}$	49	D10	D10	D10
25	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$	50	GND	GND	GND

Section 3 Functions in Each Flash Card Operating Mode

3.1 Introduction

Hitachi flash cards—both PC-ATA cards and CF—conform to PCMCIA PC-ATA specifications. The PC-ATA specifications are one set of specifications within the PCMCIA standard, comprising specifications for handling SRAM cards and flash memory cards in the same way as hard disk drives. This means that, as with hard disks in general, all read/write instructions, etc., are issued as commands via a register, and the card decodes the instructions and executes the corresponding operations. A flash card can therefore be thought of as a miniature hard disk drive rather than as ordinary memory.

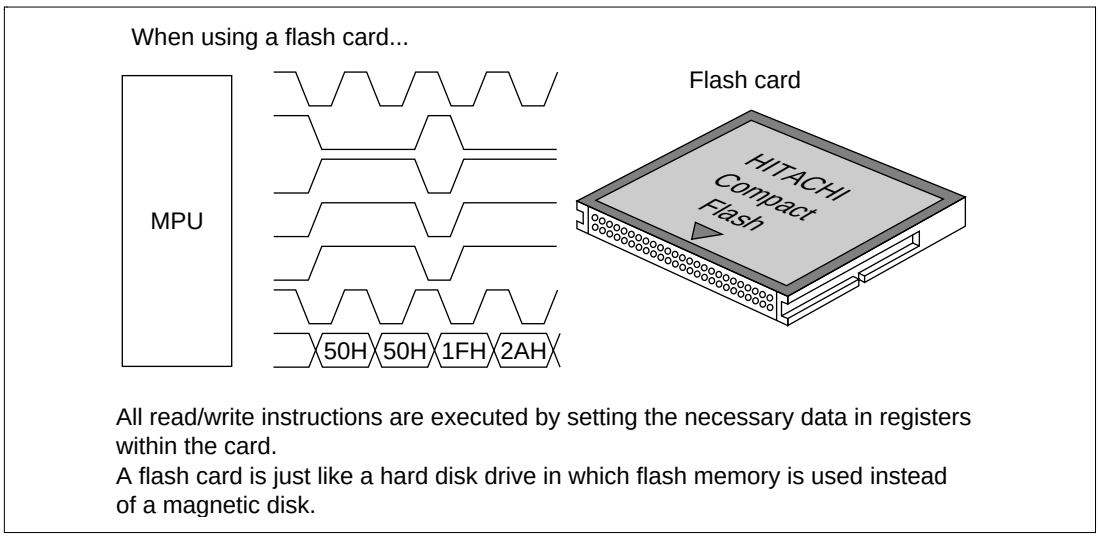
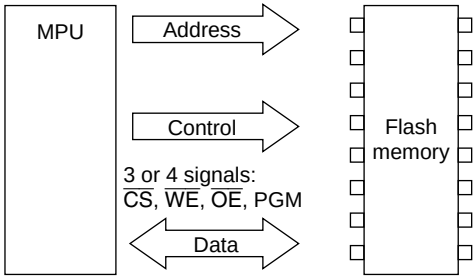


Figure 3.1 Conceptual Diagram of Flash Card Interface

One disadvantage of flash cards, therefore, may be that, unlike ordinary memory, they cannot be driven by simple interface circuitry and driver software. However, chip sets supporting PC cards for use in notebook PCs which are already available on the market can be used, and the advantage of being able to use a card of a different capacity in the future simply by switching cards, with no need to change the peripheral circuitry, far outweighs this disadvantage. This section covers the minimum information required when using a card (acquisition of card attribute information, and access to control registers).

When using EP/EEPROM memory...

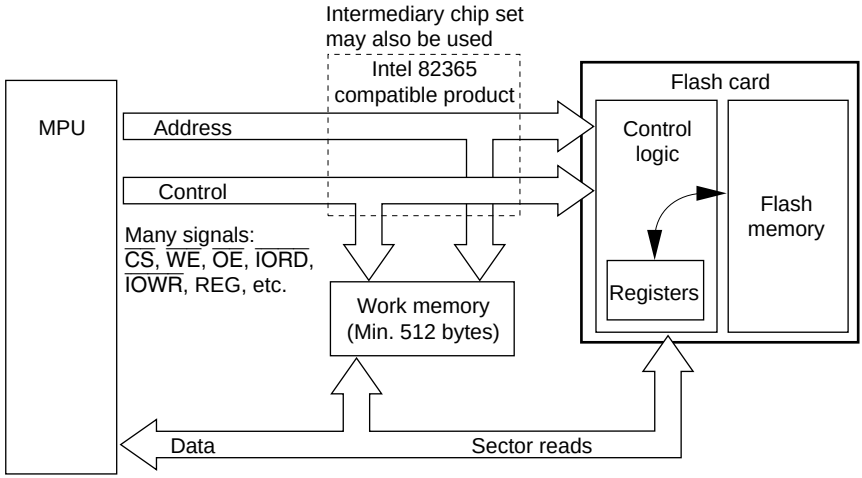


Small-scale/specific use, etc.
Systems in which states do not change greatly and only a few variables have to be stored

Advantage
Data can be written and read simply by setting the address and controlling the control pins.

Disadvantage
If the capacity or manufacturer is changed, the peripheral circuitry must be redesigned.

When using a flash card...



Large-scale/general use
Systems in which many system state variables have to be stored and managed

Advantages
The same interface circuit can be used even if the memory capacity is changed.
Large-capacity memory can be installed comparatively easily, and memory capacity can be selected in a scalable fashion.

Disadvantage
System configuration and control programs are complex.

Figure 3.2 Differences in System Size and Features with Use of a Card and Memory

3.2 Card Register Configuration

Flash memory card data is accessed via registers, as in the case of hard disk drives, etc. The actual operations can be itemized as read/write operations, mode setting, card attribute acquisition, and so on. Broadly speaking, PC-ATA cards and CF can operate in accordance with (1) PC-ATA specifications or (2) True-IDE specifications. This section and sections 3.3 and 3.4 are concerned with the PC-ATA specifications. For use of a PC-ATA card or CF in PC-ATA mode, continue reading from here. If the card is to be handled in accordance with the True-IDE specifications, skip forward to section 3.5.

(Switching between PC-ATA mode and the True-IDE specifications depends on how the flash card input pins are set at power-on. Once the card has been started up in a particular mode, it cannot be switched unless the power is turned on again. This problem is discussed in section 4.)

When the card is handled in accordance with the True-IDE specifications, the control registers can be broadly divided into two regions. One is the attribute region, used to set and manage the operating mode and store the card attributes, and the other is the task file region, used for data write and read instructions.

Attribute Region: The attribute region consists of a configuration register section for setting and managing the operation status of the card, and a CIS section for storing card attribute information, located in the address spaces shown below. The configuration register section is further subdivided into four registers.

The register names are shown below.

- Register names
  - — Configuration register section (configuration registers: 200h–206h)
    - Configuration option register (address 200h in attribute memory)
    - Configuration and status register (address 202h in attribute memory)
    - Pin replacement register (address 204h in attribute memory)
    - Socket and copy register (address 206h in attribute memory)
  - — CIS section (card information structure: 000h–168h in attribute memory)

Note: The minimum register requirements are described in section 4. For details, see the appendices.

When a card is mounted in a system by insertion in a PC card slot, it is first necessary to determine what the inserted card is. Then settings appropriate to the card must be made.

First, the CIS section must be accessed to find out what kind of card has been inserted. The CIS section contains essential information concerning the card, such as the settings that should be made, the operating voltage, and the addresses at which the registers that perform card

management and control (the configuration registers) are located. Note that the CIS section is a ROM area in which only read access is possible, and which cannot be written to by the host.

Next, it is necessary to specify the location of control-related registers and make the appropriate settings, based on information from the CIS section. These control-related registers are called the configuration registers.

The CIS section and configuration registers are both in an area called the card attribute region. The write access sequence for this region is shown in table 3.1, and detailed timing specifications are given in tables 3.2 and 3.3.

Write-related information applies only to accesses to the configuration registers, since the CIS section is a read-only area.

As shown in table 3.1, the attribute region is allocated to the even byte (D0–D7) parts of even addresses in the card., and consists entirely of 8-bit registers. Odd byte (D8–D15) parts are invalid data. Mapping of the task file region described later is also performed by these registers.

Note: The configuration registers are used to set the operating mode of the card. It might therefore be supposed that switching between PC-ATA specifications and True-IDE specifications in a flash card can also be performed by means of these registers, but this is not the case. These registers can only be used with the PC-ATA specifications. Whether a flash card is set to the PC-ATA specifications or True-IDE specifications depends on the input pin settings when the power is turned on; once the card has been started up in a particular mode, the mode can only be changed by turning on the power again.

Table 3.1 Attribute Region Access

- Attribute region
  - — Configuration register access

Register Name	R/W	$\overline{CE2}$	$\overline{CE1}$	$\overline{REG}$	$\overline{OE}$	$\overline{WE}$	A10	A9	A8–A4	A3	A2	A1	A0	D15–D8	D7–D0
Configuration Option REG. Add 200h	R	×*1	L	L	L	H	0	1	0	0	0	0	0	High-Z	Even byte data
	W				H	L								Don't care	
Card Status REG. Add 202h	R				L	H	0	1	0	0	0	1	0	High-Z	
	W				H	L								Don't care	
Pin Replacement REG. Add 204h	R				L	H	0	1	0	0	1	0	0	High-Z	
	W				H	L								Don't care	
Socket and Copy REG. Add 206h	R				L	H	0	1	0	0	1	1	0	High-Z	
	W				H	L								Don't care	

  - — CIS access

Register Name	R	$\overline{CE2}$	$\overline{CE1}$	$\overline{REG}$	$\overline{OE}$	$\overline{WE}$	A10–A0	D15–D8	D7–D0
CIS REG. Add 000h–0FEh	R*2	×*2	L	L	L	H*2	× Corresponds to addresses 000h–0FEh	High-Z	Even byte

Notes: 1. In the attribute section, as with accesses to other main memory, even byte/odd byte switching can be performed using $\overline{CE1}$ and $\overline{CE2}$. However, in the attribute section, only even bytes are valid. Therefore, when a word access is executed (16-bit width, $\overline{CE1}$ and $\overline{CE2}$ low), invalid data is output when the odd byte part (D15–D8) is read, and input data is ignored when the odd byte part is written.

2. The CIS section is a read-only area that stores card attribute information. It cannot be written to. Only even bytes are valid, as with other registers in the attribute region.

Table 3.2 Attribute Memory Read Timing

	Speed Version		300 ns	
No.	**Item**	**Symbol**	**Min [ns]**	**Max [ns]**
1	Read cycle time	t_{CR}	250	
2	Address access time	t_A (Add)		250
3	Card enable access time	t_A (CE)		250
4	Output enable access time	t_A (OE)		125
5	Output disable time from CE	t_{DIS} (CE)		100
6	Output disable time from OE	t_{DIS} (OE)		100
7	Address setup time	t_{SU} (Add)	30	
8	Output enable time from CE	t_{EN} (CE)	5	
9	Output enable time from OE	t_{EN} (OE)	5	
10	Data vaild from address change	t_V (Add)	0	

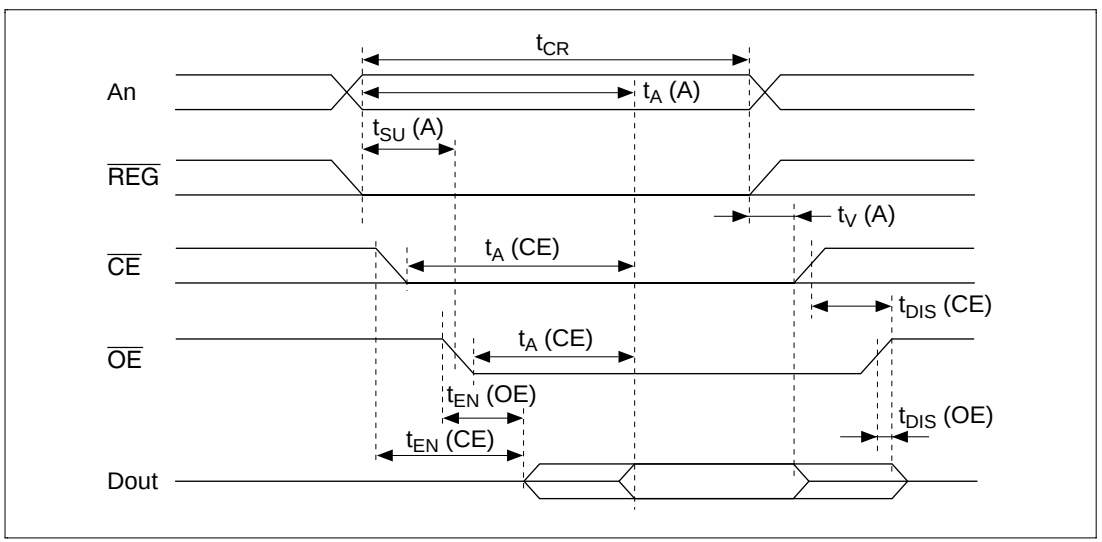


Figure 3.3 Attribute Memory Read Timing Chart

Note: The attribute memory read access time is stipulated as 300 ns or more. Data placed on Dout is the data output from the CF and transferred to the host. When a burst read is performed, either $\overline{CE}$ or $\overline{OE}$ must be driven high.

Table 3.3 Attribute Memory Write Timing

	Speed Version		250 ns	
No.	**Item**	**Symbol**	**Min [ns]**	**Max [ns]**
1	Write cycle time	t_{CW}	250	
2	Write pulse width	t_W (WE)	150	
3	Address setup time	t_{SU} (Add)	30	
4	Write recovery time	t_{REC} (WE)	30	
5	Data setup time for WE	t_{SU} (D-WEH)	80	
6	Data hold time	t_H (D)	30	

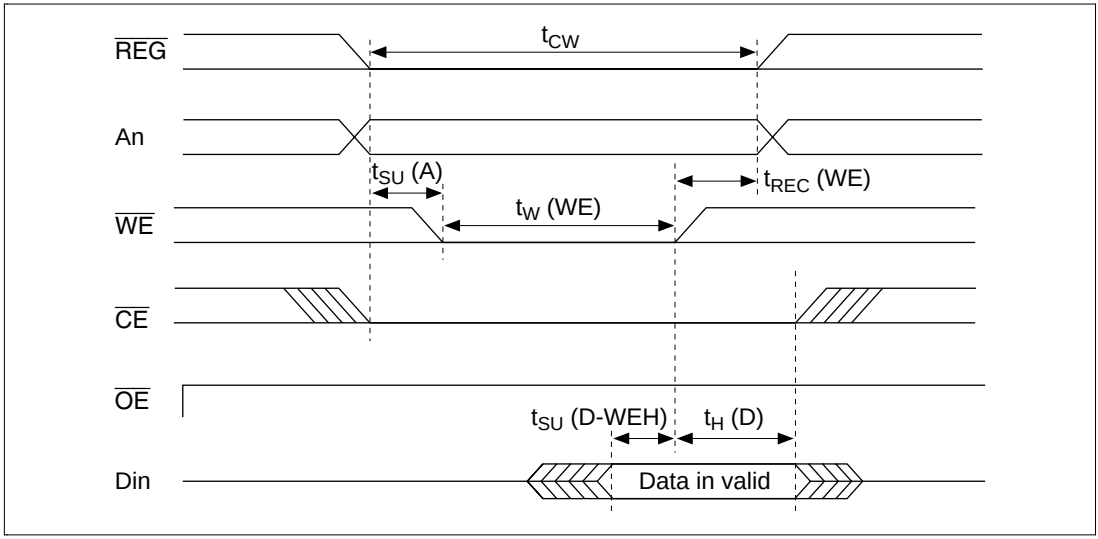


Figure 3.4 Attribute Memory Write Timing Chart

Note: The attribute memory write access time is stipulated as 250 ns or more. Data placed on Din is the data output from the host and transferred to the card. With a flash card, writes cannot be performed to the CIS section, so this timing applies only to writes to the configuration registers.

Memo

Aren't flash cards only used in personal computers and digital cameras?

Flash cards may be thought of as only being used for data storage in notebook PCs and digital cameras. It is true that PC-ATA cards and CompactFlash™ were designed to be inserted into a PC card slot, but flash cards are not only used as HD or FD replacements in PC card slots. Although the control method is different from that used up to now, since the cards contain flash memory it is natural that they should be able to be used as program ROM.

For example, with a general-purpose sequence that handles a large program, if it is necessary to change the program according to its intended use, a flash card could be used instead of writing data in program ROM. Program replacement can be achieved simply by switching cards. In a system in which the program size and number of variables may increase in the future, an initial small-capacity card could be replaced when necessary at a later date with a larger-capacity card.

There is no need for a special device to write data to a card or verify its contents; this can be done using an ordinary personal computer. By adopting a slightly different perspective and looking at flash cards as system components, a variety of different uses can be found.

Task File Region: The task file region contains the following registers, and is used for data exchange (reading/writing) between the card and the host.

- Register names
  - Data register
  - Drive head register
  - Error register
  - Status register
  - Feature register
  - Alternate status register
  - Sector count register
  - Command register
  - Sector number register
  - Device control register
  - Cylinder low register
  - Cylinder high register
  - Drive address register

Note: For details of register settings, see the descriptions of task file register contents in the appendices.

The addresses at which these registers are located are changed by settings in the configuration option register in the attribute region. The operating mode and interface pin functions are also changed.

There are four operating modes, selected by a setting in the configuration option register.

- Memory mode
- Primary I/O mode
- Secondary I/O mode
- Contiguous I/O mode

The basic handling is the same in the primary, secondary, and contiguous I/O modes, the only differences being in the mapping of the task file registers. There are thus basically two operating modes, memory mode and I/O mode. These are described in sections 3.3 and 3.4.

3.3 Memory Mode

Both PC-ATA cards and CF enter memory mode at power-on or in a hardware reset. Therefore, while no particular settings are required concerning the operating mode, it is preferable to make settings in the configuration option register. The configuration option register settings shown in table 3.4 place the card in memory mode.

In memory mode, read and write operations are performed by controlling $\overline{\text{WE}}$ and $\overline{\text{OE}}$. At this time, $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ must be held high. This mode is useful when driving a card using a CPU with no $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ signals, a CISC microcomputer, or a RISC microcomputer. When using a microcomputer that has $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ signals and is capable of control by IN/OUT instructions, it may be more convenient to use I/O mode.

The pin interface in memory mode is shown in tables 3.7 and 3.8.

For the method of accessing the registers, and timing details, see tables 3.4 to 3.6, etc.

Table 3.4 Memory Mode

Configuration Option Register (Attribute 200h)

Setting	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
Register	R/W	SRST	LevReg	0	0	0	0	0	0

Note: Normally, the card enters memory mode when powered on.

Allocation: 0–F, 400–7FF

Register No.	Register Name	R/W	$\overline{CE2}$	$\overline{CE1}$	$\overline{REG}$	$\overline{RD}$	$\overline{WR}$	A10	A9–A4	A3	A2	A1	A0	Offset	Attribute
0*1	Even data	R	*1	L	H	L	H	0	×	0	0	0	0	0	R/W
		W				H	L								
1*1	Error REG	R				L	H	0		0	0	0	1	1	R only
	Feature REG	W				H	L								W onry
2	Sector count	R				L	H	0		0	0	1	0	2	R/W
		W				H	L								
3	Sector no	R				L	H	0		0	0	1	1	3	R/W
		W				H	L								
4	Cylinder low	R				L	H	0		0	1	0	0	4	R/W
		W				H	L								
5	Cylinder high	R				L	H	0		0	1	0	1	5	R/W
		W				H	L								
6	Select card/head	R				L	H	0		0	1	1	0	6	R/W
		W				H	L								
7	Status	R				L	H	0		0	1	1	1	7	R only
	Command	W				H	L								W only
8*2	Dup. even data	R				L	H	0		1	0	0	0	8	R/W
		W				H	L								
9*2	Dup. odd data	R				L	H	0		1	0	0	1	9	R/W
		W				H	L								
10*2	Dup. error REG	R				L	H	0		1	1	0	1	D	R only
	Dup. feature REG	W				H	L								W only
11	Alt status	R				L	H	0		1	1	1	0	E	R only
	Drive control	W				H	L								W only
12	Drive address	R				L	H	0		1	1	1	1	F	R only
	Reserved	W				H	L								W only
8*3	Dup. even data	R				L	H	1		×	×	×	0	8	R/W
		W				H	L								
9*3	Dup. odd data	R				L	H	1		×	×	×	1	9	R/W
		W				H	L								

$\overline{IORD}$, IOWR: Fixed high

Notes: 1. Note that the meaning of the data differs depending on whether byte access or word access is used on register 0.

- Byte access
  $\overline{CE1}$ low, $\overline{CE2}$ high: The even byte is accessed first, followed by the odd byte.
  $\overline{CE1}$ high, $\overline{CE2}$ low: Register 1 ErrorREG. or FeaturesREG is accessed.
- Word access
  $\overline{CE1}$, $\overline{CE2}$ low: Operates as a word register via D15–D0. A0 is ignored. In this case, the format is for EvenRD Data + ErrorREG (when reading) or EvenWR Data + Features REG. (when writing) to exist in the same word.

2. The contents of registers 8–10 are a duplicate of the data in registers 0 and 1. Thus the following access methods are possible.
   - Byte access
     — When consecutive byte accesses are performed on register 0 (8), the even-byte data is accessed first, followed by the odd-byte data.
     — By performing byte access to register 9 and register 8, in that order, the odd-byte data is accessed first, followed by the even-byte data.
     — By performing byte access to register 8 and register 9, in that order, the even-byte data is accessed first, followed by the odd-byte data.
     — When access is performed alternately to register 0 and register 8, the even-byte data is accessed first, followed by the odd-byte data.

     Byte access cannot be performed on register 9, either singly or consecutively. It must always be paired with register 8, and used only for extracting odd-byte data from word data.
   - Word access
     — As in note 1 above. Register 8 can also be handled in the same way as register 0.

3. Data is placed in order in the 1-kbyte memory space from 400 to 7FF, starting at the selected address.

   Of this data, even-address data can be accessed via register 8, and odd-address data via register 9. Use of this function allows functions such as block transfer to be implemented between memory areas in the card. However, note that this involves accessing a FIFO starting with a certain address, and does not mean that the sector buffer in the CF can be accessed randomly.

Table 3.5 Common Memory Read Timing

No.	Item	Symbol	Min [ns]	Max [ns]
1	Output enable access time	t_A (OE)		125
2	Output disable time from OE	t_{DIS} (OE)		100
3	Address setup time	t_{SU} (Add)	30	
4	Address hole time	t_H (Add)	20	
5	CE setup before OE	t_{SU} (CE)	0	
6	CE hold following OE	t_H (CE)	20	
7	Wait delay falling from OE	t_V (WIT-OE)		35
8	Data setup for wait release	t_V (WIT)		0
9	Wait width time (default speed)	t_W (WIT)		350

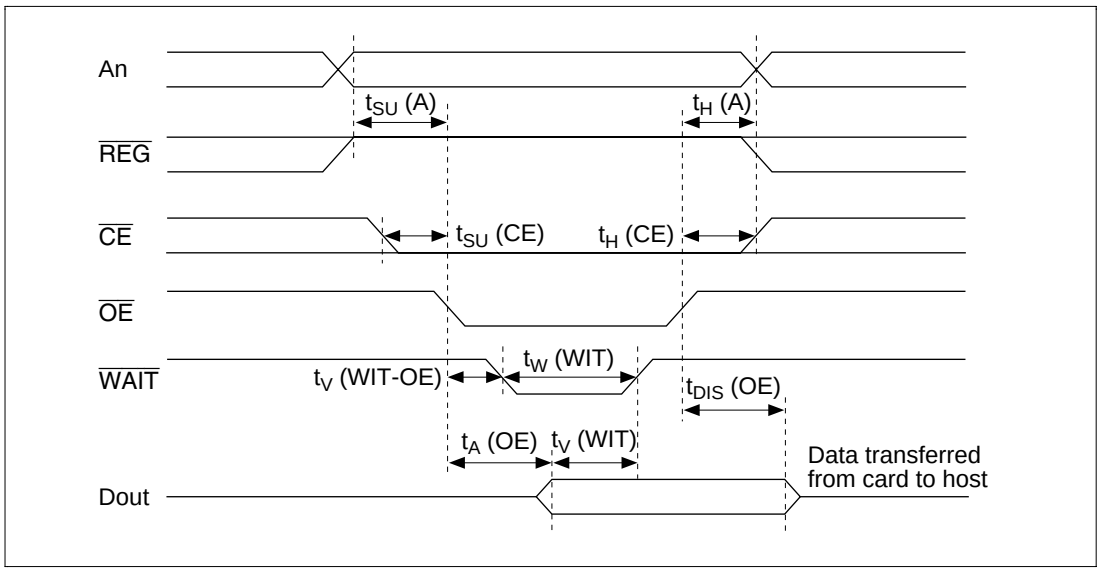


Figure 3.5 Common Memory Read Timing Chart

Note: The $\overline{\text{WAIT}}$ maximum load is one 50 pF LS-TTL in total.
The $\overline{\text{WAIT}}$ maximum width (slowest mode operation) is stipulated by the CIS section.
If the $\overline{\text{OE}}$ cycle-to-cycle time is longer than $\overline{\text{WAIT}}$ signal width, the $\overline{\text{WAIT}}$ signal may be ignored.

Table 3.6 Common Memory Write Timing

No.	Item	Symbol	Min [ns]	Max [ns]
1	Data setup before WE	t_{SU} (D-WEH)	80	
2	Data hold following WE	t_H (D)	30	
3	WE pulse Width	t_W (WE)	150	
4	Address setup time	t_{SU} (Add)	30	
5	CE setup before WE	t_{SU} (CE)	0	
6	Write recovery	t_{REC} (WE)	30	
7	Address hold time	t_H (Add)	20	
8	CE hold following WE	t_H (CE)	20	
9	Wait delay falling from WE	t_V (WIT-WE)		35
10	WE high from wait release	t_V (WT)	0	
11	Wait width time	t_V (WIT)		350

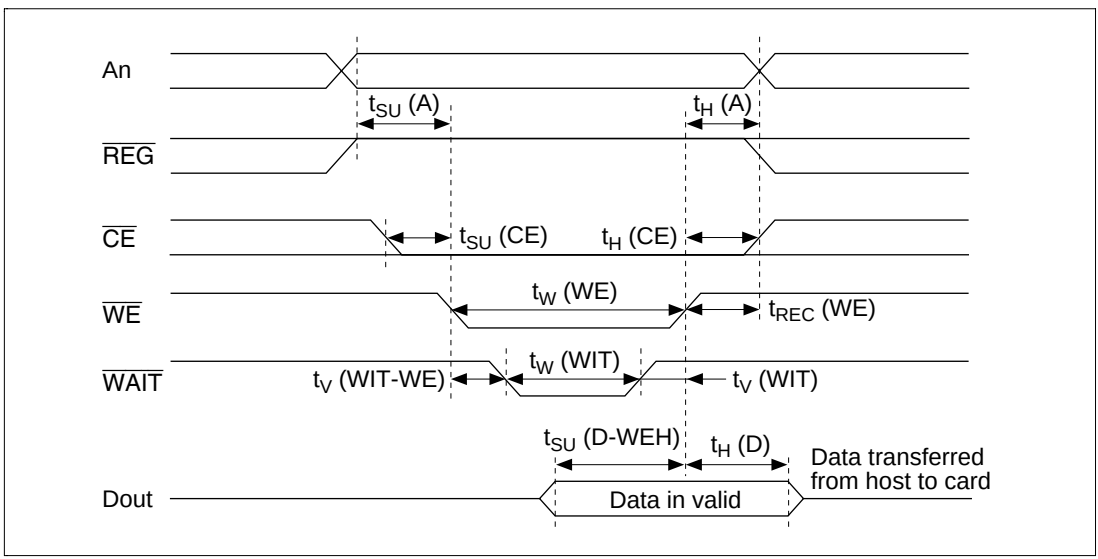


Figure 3.6 Common Memory Write Timing Chart

Note: The $\overline{\text{WAIT}}$ maximum load is one 50 pF LS-TTL in total.
The $\overline{\text{WAIT}}$ maximum width (slowest mode operation) is stipulated by the CIS section.
If the $\overline{\text{WE}}$ cycle-to-cycle time is longer than $\overline{\text{WAIT}}$ signal width, the $\overline{\text{WAIT}}$ signal may be ignored.

Table 3.7 Pin Arrangement in Memory Mode

CompactFlash™

Pin No.	Memory Card	Pin No.	Memory Card
1	GND	26	$\overline{CD1}$
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	$\overline{CE1}$	32	$\overline{CE2}$
8	A10	33	$\overline{VS1}$
9	$\overline{OE}$	34	$\overline{IORD}$
10	A9	35	$\overline{IOWR}$
11	A8	36	$\overline{WE}$
12	A7	37	RDY/BUSY
13	V_{CC}	38	V_{CC}
14	A6	39	—
15	A5	40	$\overline{VS2}$
16	A4	41	RESET
17	A3	42	$\overline{WAIT}$
18	A2	43	—
19	A1	44	$\overline{REG}$
20	A0	45	BVD2
21	D0	46	BVD1
22	D1	47	D8
23	D2	48	D9
24	WP	49	D10
25	$\overline{CD2}$	50	GND

Table 3.7 Pin Arrangement in Memory Mode (cont)

PC-ATA Card

Pin No.	Memory Card	Pin No.	Memory Card
1	GND	35	GND
2	D3	36	$\overline{CD1}$
3	D4	37	D11
4	D5	38	D12
5	D6	39	D13
6	D7	40	D14
7	$\overline{CE1}$	41	D15
8	A10	42	$\overline{CE2}$
9	$\overline{OE}$	43	$\overline{VS1}$
10	—	44	RFU
11	A9	45	RFU
12	A8	46	—
13	—	47	—
14	—	48	—
15	$\overline{WE}$	49	—
16	RED/BUSY	50	—
17	V_{CC}	51	V_{CC}
18	—	52	—
19	—	53	—
20	—	54	—
21	—	55	—
22	A7	56	—
23	A6	57	$\overline{VS2}$
24	A5	58	RESET
25	A4	59	$\overline{WAIT}$
26	A3	60	RFU
27	A2	61	$\overline{REG}$
28	A1	62	BVD2
29	A0	63	BVD1
30	D0	64	D8
31	D1	65	D9
32	D2	66	D10
33	WP	67	$\overline{CD2}$
34	GND	68	GND

Table 3.8 Pin Functions in Memory Mode

Abbreviation	Pin No. Compact Flash	Pin No. PC-ATA Card	Input/ Output	Function
V_{CC}	13, 38	17, 51	Input	Power supply pins
GND	1, 50	1, 34, 35, 68	Input	GND pins
D0–D15	21, 22, 23, 2, 3, 4, 5, 6, 47, 48, 49, 27, 28, 29, 30, 31	30, 31, 32, 2, 3, 4, 5, 6, 64, 65, 66, 37, 38, 39, 40, 41	Input/ Output	Data bus. D0–D7 comprise the even byte of a word, and D8–D15 the odd byte. D0 and D8 are the respective LSBs.
A0–A10	20, 19, 18, 17, 16, 15, 14, 12, 11, 10, 8	29, 28, 27, 26, 25, 24, 23, 22, 12, 11, 8	Input	Address bus. A10 is the MSB, and A0 the LSB.
$\overline{CE1}$, $\overline{CE2}$	7, 32	7, 42	Input	$\overline{CE1}$ is used for even address control and $\overline{CE2}$ for odd address control. Both are active-low.
$\overline{OE}$	9	9	Input	This pin is used to read the contents of both attribute and common areas. Active-low.
$\overline{WE}$	36	15	Input	This pin is used to write the contents of both attribute and common areas. Active-low.
$\overline{IORD}$	34	44	Input	Not used in memory mode. It is recommended that this pin be pulled high.
$\overline{IOWR}$	35	45	Input	Not used in memory mode. It is recommended that this pin be pulled high.
RDY/ BUSY	37	16	Output	Goes low during internal initialization operations performed automatically at power-on and in a reset. Proceed to the next operation when this pin goes high.
$\overline{CD1}$, $\overline{CD2}$	26, 25	36, 67	Output	Used by the host to determine whether a card is inserted. These pins are connected to GND inside the card.
WP	24	33	Output	Originally intended to indicate whether the write-protect state is in effect, but as this card has no write-protect function, the output of this pin is always low.

Table 3.8 Pin Functions in Memory Mode (cont)

Abbre-viation	Pin No. Compact Flash	Pin No. PC-ATA Card	Input/ Output	Function
$\overline{REG}$	44	61	Input	Input pin for switching between common and attribute area access. Drive high for common area access, and low for attribute area access. As the attribute area section is allocated to even addresses, D8–D15 are invalid in word access mode. In byte access, odd addresses are invalid.
BVD1	46	63	Output	Originally intended to indicate the card's internal battery voltage level, but as this card has no battery, the output of this pin is always high.
BVD2	45	62	Output	Originally intended to indicate the card's internal battery voltage level, but as this card has no battery, the output of this pin is always high.
RESET	41	58	Input	All registers in the card can be cleared by high-level input at this pin. Initialization is then started, and RDY/BSY output goes high.
WAIT	42	59	Output	I/O access or memory access cycle execution is kept waiting while the output of this pin is low.
$\overline{INPACK}$	43	60	Output	Not used in memory card mode.
$\overline{VS1}$, $\overline{VS2}$	33, 40	43, 57	Output	These pins indicate the required input voltage value for this card (CIS information).

3.4 I/O Mode (Primary/Secondary/Contiguous)

The card enters memory mode immediately after being powered on and in a hardware reset. Therefore, in order to use the card in I/O mode, the configuration option register in the attribute region must be set for the card as shown in tables 3.9 to 3.11.

In I/O mode, reading and writing is performed by controlling $\overline{IORD}$ and $\overline{IOWR}$. $\overline{WE}$ and $\overline{OE}$ must be held high.

This mode may be useful when using an MPU that has $\overline{IORD}$ and $\overline{IOWR}$ signals.

The pin interface in I/O mode is shown in tables 3.14 and 3.15. For the method of accessing the registers, and timing details, see tables 3.9 to 3.13, etc.

Table 3.9 Primary I/O Mode

Configuration Option Register (Attribute 200h)

Setting	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
Register	R/W	SRST	LevReg	0	0	0	0	1	0

Allocation: 1F0–1F7, 3F6–3F7
Interrupt: IRQ14
Drive no.: 0 (1 is not supported)

Register No.	Register Name	R/W	$\overline{CE2}$	$\overline{CE1}$	$\overline{REG}$	$\overline{IORD}$	$\overline{IOWR}$	A9–A4	A3	A2	A1	A0
0*2	Even RD data	R	*1	L	L	L	H	1F	0	0	0	0
		W				H	L					
1*2	Error REG.	R				L	H			0	0	1
	Feature REG.	W				H	L					
2	Sector count	R				L	H			0	1	0
		W				H	L					
3	Sector no	R				L	H			0	1	1
		W				H	L					
4	Cylinder low	R				L	H			1	0	0
		W				H	L					
5	Cylinder high	R				L	H			1	0	1
		W				H	L					
6	Select card/ head	R				L	H			1	1	0
		W				H	L					
7	Status	R				L	H			1	1	1
	Command	W				H	L					
8	Alt status	R				L	H	3F		1	1	0
	Drive control	W				H	L					
9	Drive address	R				L	H			1	1	1
	Reserved	W				H	L					

$\overline{WE}$, $\overline{OE}$: Fixed high

Note: 1. Note that the meaning of the data differs depending on whether byte access or word access is used on register 0.

- Byte access
  $\overline{CE1}$ low, $\overline{CE2}$ high: The even byte is accessed first, followed by the odd byte.
  $\overline{CE1}$ high, $\overline{CE2}$ low: Register 1 Error REG. or Features.REG. is accessed.
- Word access
  $\overline{CE1}$, $\overline{CE2}$ low: Operates as a word register via D15–D0. A0 is ignored. In this case, the format is for Even RD Data + Error REG. (when reading) or Even WR Data + Features REG. (when writing) to exist in the same word.

Table 3.10 Secondary I/O Mode

Configuration Option Register (Attribute 200h)

Setting	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
Register	R/W	SRST	LevReg	0	0	0	1	1	0

Allocation: 170–177, 376–377
Interrupt: IRQ14
Drive no.: 0 (1 is not supported)

Register No.	Register Name	R/W	$\overline{CE2}$	$\overline{CE1}$	$\overline{REG}$	$\overline{IORD}$	$\overline{IOWR}$	A9–A4	A3	A2	A1	A0
0*2	Even RD data	R	*1	L	L	L	H	17	0	0	0	0
		W				H	L					
1*2	Error REG.	R				L	H			0	0	1
	Feature REG.	W				H	L					
2	Sector count	R				L	H			0	1	0
		W				H	L					
3	Sector No	R				L	H			0	1	1
		W				H	L					
4	Cylinder low	R				L	H			1	0	0
		W				H	L					
5	Cylinder high	R				L	H			1	0	1
		W				H	L					
6	Select card/ head	R				L	H			1	1	0
		W				H	L					
7	Status	R				L	H			1	1	1
	Command	W				H	L					
8	Alt Status	R				L	H	37		1	1	0
	Drive control	W				H	L					
9	Drive Address	R				L	H			1	1	1
	Reserved	W				H	L					

$\overline{WE}$, $\overline{OE}$: Fixed high

Note: 1. Note that the meaning of the data differs depending on whether byte access or word access is used on register 0.

- Byte access
  $\overline{CE1}$ low, $\overline{CE2}$ high: The even byte is accessed first, followed by the odd byte.
  $\overline{CE1}$ high, $\overline{CE2}$ low: Register 1 Error REG. or Features REG. is accessed.
- Word access
  $\overline{CE1}$, $\overline{CE2}$ low: Operates as a word register via D15–D0. A0 is ignored. In this case, the format is for Even RD Data + Error REG. (when reading) or Even WR Data + Features REG. (when writing) to exist in the same word.

Table 3.11 Contiguous I/O Mode

Configuration Option Register (Attribute 200h)

Setting	OPERATION	D7	D6	D5	D4	D3	D2	D1	D0
Register	R/W	SRST	LevReg	0	0	0	0	0	1

Allocation: Allocated to 16 contiguous bytes starting at any I/O address.

Register No.	Register Name	R/W	$\overline{CE2}$	$\overline{CE1}$	$\overline{REG}$	$\overline{IORD}$	$\overline{IOWR}$	Other Add	A3	A2	A1	A0	Offset	Attribute
0*1	Even data	R	*1	L	L	L	H	*3	0	0	0	0	0	R/W
		W				H	L							
1*1	Error REG.	R				L	H		0	0	0	1	1	R only
	Feature REG.	W				H	L							W only
2	Sector count	R				L	H		0	0	1	0	2	R/W
		W				H	L							
3	Sector No	R				L	H		0	0	1	1	3	R/W
		W				H	L							
4	Cylinder low	R				L	H		0	1	0	0	4	R/W
		W				H	L							
5	Cylinder high	R				L	H		0	1	0	1	5	R/W
		W				H	L							
6	Select card/ head	R				L	H		0	1	1	0	6	R/W
		W				H	L							
7	Status	R				L	H		0	1	1	1	7	R only
	Command	W				H	L							W only
8*2	Dup. even data	R				L	H		1	0	0	0	8	R/W
		W				H	L							
9*2	Dup. odd data	R				L	H		1	0	0	1	8	R/W
		W				H	L							
10*2	Dup. error REG.	R				L	H		1	1	0	1	D	R only
	Dup. feature REG.	W				H	L							W only
11	Alt status	R				L	H		1	1	1	0	E	R only
	Drive control	W				H	L							W only
12	Drive address	R				L	H		1	1	1	1	F	R only
	Reserved	W				H	L							W only

$\overline{WE}$, $\overline{OE}$: Fixed high

Notes: 1. Note that the meaning of the data differs depending on whether byte access or word access is used on register 0.

- Byte access
  $\overline{CE1}$ low, $\overline{CE2}$ high: The even byte is accessed first, followed by the odd byte.
  $\overline{CE1}$ high, $\overline{CE2}$ low: Register 1 Error REG. or Features REG. is accessed.
- Word access
  $\overline{CE1}$, $\overline{CE2}$ low: Operates as a word register via D15–D0. A0 is ignored. In this case, the format is for Even RD Data + Error REG. (when reading) or Even WR Data + Features REG. (when writing) to exist in the same word.

2. The contents of registers 8–10 are a duplicate of the data in registers 0 and 1. Thus the following access methods are possible.

- Byte access
  - When consecutive byte accesses are performed on register 0 (8), the even-byte data is accessed first, followed by the odd-byte data.
  - By performing byte access to register 9 and register 8, in that order, the odd-byte data is accessed first, followed by the even-byte data.
  - By performing byte access to register 8 and register 9, in that order, the even-byte data is accessed first, followed by the odd-byte data.
  - When access is performed alternately to register 0 and register 8, the even-byte data is accessed first, followed by the odd-byte data.

    Byte access cannot be performed on register 9, either singly or consecutively. It must always be paired with register 8, and used only for extracting odd-byte data from word data.
- Word access
  - As in note 1 above. Register 8 can also be handled in the same way as register 0.

3. With CompactFlash™, address lines other than A0–A3 are ignored when accessing the above task file region address space.

Note: Although there are three I/O modes—primary, secondary, and contiguous—the only difference is in the mapping of the task file registers; the access timing is the same for all three modes.

Specifications Common to Primary, Secondary, and Contiguous Modes

Table 3.12 I/O Read Timing

No.	Item	Symbol	Min [ns]	Max [ns]
1	Data delay after IORD	t_D (IORD)		100
2	Data hold following IORD	t_H (IORD)	0	
3	IORD width time	t_{WIORD}	165	
4	Address setup before IORD	t_{SUA} (IORD)	70	
5	Address hold following IORD	t_{HA} (IORD)	20	
6	$\overline{CE}$ setup before IORD	t_{SUCE} (IORD)	5	
7	$\overline{CE}$ hold following IORD	t_{HCE} (IORD)	20	
8	$\overline{REG}$ setup before IORD	t_{SUREG} (IORD)	5	
9	$\overline{REG}$ hold following IORD	t_{HREG} (IORD)	0	
10	$\overline{INPACK}$ delay falling from IORD	$t_{DFINPACK}$ (IORD)	0	45
11	$\overline{INPACK}$ delay rising from IORD	$t_{DRINPACK}$ (IORD)		45
12	$\overline{IOIS16}$ delay falling from IORD	$t_{DFIOIS16}$ (Add)		35
13	$\overline{IOIS16}$ delay rising from IORD	$t_{DRIOIS16}$ (Add)		35
14	$\overline{Wait}$ delay falling from IORD	t_{DWIT} (IORD)		35
15	Data delay from wait rising	t_D (WIT)		0
16	$\overline{Wait}$ width time (default speed)	t_W (WIT)		350

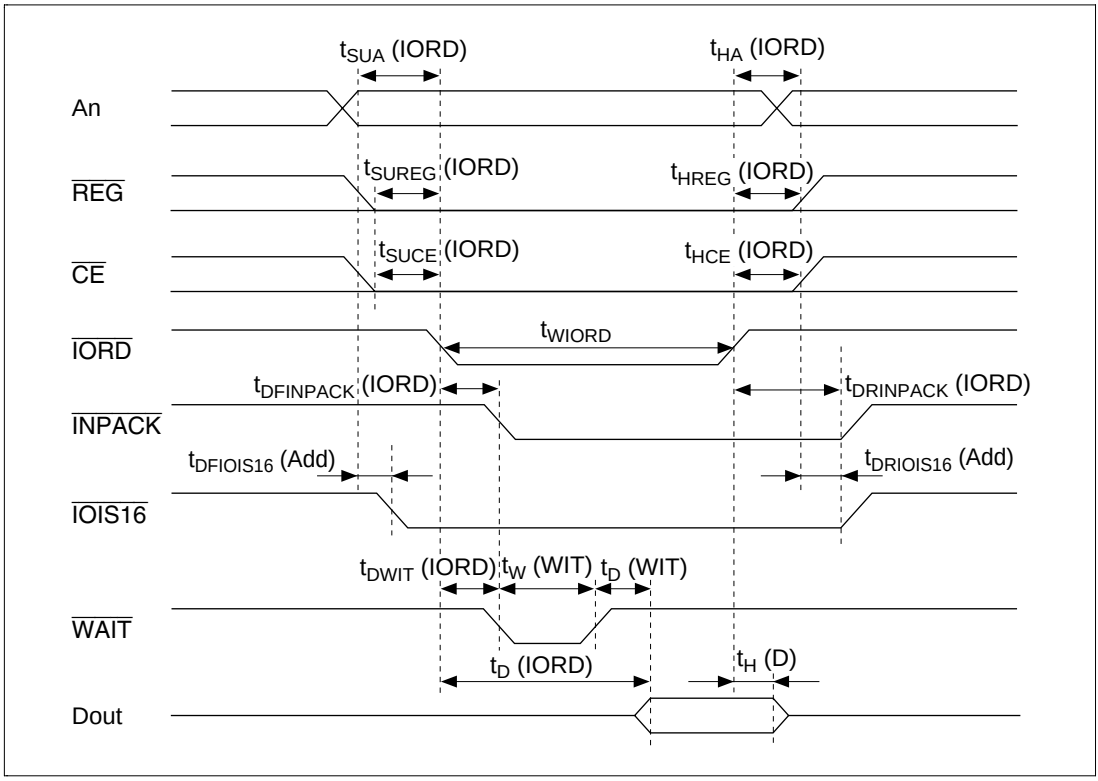


Figure 3.7 I/O Read Timing Chart

Note: The maximum load for $\overline{\text{WAIT}}$, $\overline{\text{INPACK}}$, and $\overline{\text{IOIS16}}$ is one 50 pF LS-TTL in total. In a read, the time from the point at which $\overline{\text{WAIT}}$ goes high until $\overline{\text{IORD}}$ goes high is 0 ns or more.

Table 3.13 I/O Write Timing

No.	Item	Symbol	Min [ns]	Max [ns]
1	Data setup before IOWR	t_{SU} (IOWR)	60	
2	Data hold following IOWR	t_{H} (IOWR)	30	
3	IOWR pulse width	t_{WIOWR}	165	
4	Address setup before IOWR	t_{SUA} (IOWR)	70	
5	Address hold following IOWR	t_{HA} (IOWR)	20	
6	$\overline{CE}$ setup before IOWR	t_{SUCE} (IOWR)	5	
7	$\overline{CE}$ hold following IOWR	t_{HCE} (IOWR)	20	
8	$\overline{REG}$ setup before IOWR	t_{SUREG} (IOWR)	5	
9	$\overline{REG}$ hold following IOWR	t_{HREG} (IOWR)	0	
10	$\overline{IOIS16}$ delay falling from IOWR	$t_{DFIOIS16}$ (Add)		35
11	$\overline{IOIS16}$ delay rising from IOWR	$t_{DRIOIS16}$ (Add)		35
10	$\overline{WAIT}$ delay falling from IOWR	t_{DWIT} (IOWR)		35
11	IOWR high from $\overline{WAIT}$ high	t_{DRIOWR} (WIT)	0	
11	$\overline{WAIT}$ width time (default speed)	t_{W} (WIT)		350
	(Set feature speed < 68 mA)			700

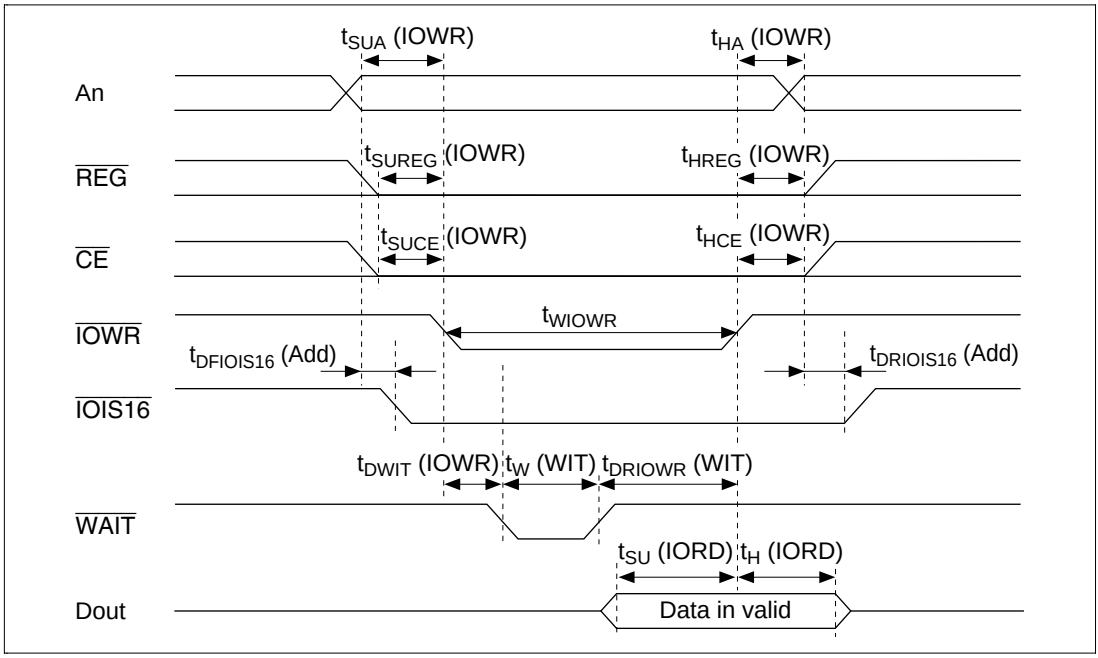


Figure 3.8 I/O Write Timing Chart

Note: The maximum load for $\overline{\text{WAIT}}$, $\overline{\text{INPACK}}$, and $\overline{\text{IOIS16}}$ is one 50 pF LS-TTL in total. In a write, the time from the point at which $\overline{\text{WAIT}}$ goes high until $\overline{\text{IOWR}}$ goes high is 0 ns or more.

Table 3.14 Pin Arrangement in I/O Mode

CompactFlash™

Pin No.	Memory Card	Pin No.	Memory Card
1	GND	26	$\overline{CD1}$
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	$\overline{CE1}$	32	$\overline{CE2}$
8	A10	33	$\overline{VS1}$
9	$\overline{OE}$	34	$\overline{IORD}$
10	A9	35	$\overline{IOWR}$
11	A8	36	$\overline{WE}$
12	A7	37	$\overline{IREQ}$
13	V_{CC}	38	V_{CC}
14	A6	39	—
15	A5	40	$\overline{VS2}$
16	A4	41	RESET
17	A3	42	$\overline{WAIT}$
18	A2	43	$\overline{INPACK}$
19	A1	44	$\overline{REG}$
20	A0	45	$\overline{SPKR}$
21	D0	46	$\overline{STSCHG}$
22	D1	47	D8
23	D2	48	D9
24	$\overline{IOIS16}$	49	D10
25	$\overline{CD2}$	50	GND

Table 3.14 Pin Arrangement in I/O Mode (cont)

PC-ATA Card

Pin No.	Memory Card	Pin No.	Memory Card
1	GND	35	GND
2	D3	36	$\overline{CD1}$
3	D4	37	D11
4	D5	38	D12
5	D6	39	D13
6	D7	40	D14
7	$\overline{CE1}$	41	D15
8	A10	42	$\overline{CE2}$
9	$\overline{OE}$	43	$\overline{VS1}$
10	—	44	$\overline{IORD}$
11	A9	45	$\overline{IOWR}$
12	A8	46	—
13	—	47	—
14	—	48	—
15	$\overline{WE}$	49	—
16	$\overline{IREQ}$	50	—
17	V_{CC}	51	V_{CC}
18	—	52	—
19	—	53	—
20	—	54	—
21	—	55	—
22	A7	56	—
23	A6	57	$\overline{VS2}$
24	A5	58	RESET
25	A4	59	$\overline{WAIT}$
26	A3	60	$\overline{INPACK}$
27	A2	61	$\overline{REG}$
28	A1	62	$\overline{SPKR}$
29	A0	63	$\overline{STSCHG}$
30	D0	64	D8
31	D1	65	D9
32	D2	66	D10
33	$\overline{IOIS16}$	67	$\overline{CD2}$
34	GND	68	GND

Table 3.15 Pin Functions in I/O Mode

Abbreviation	Pin No. Compact Flash	Pin No. PC-ATA Card	Input/ Output	Function
V_{CC}	13, 38	17, 51	Input	Power supply pins
GND	1, 50	1, 34, 35, 68	Input	GND pins
D0–D15	21, 22, 23, 2, 3, 4, 5, 6, 47, 48, 49, 27, 28, 29, 30, 31	30, 31, 32, 2, 3, 4, 5, 6, 64, 65, 66, 37, 38, 39, 40, 41	Input/ Output	Data bus. D0–D7 comprise the even byte of a word, and D8–D15 the odd byte. D0 and D8 are the respective LSBs.
A0–A10	20, 19, 18, 17, 16, 15, 14, 12, 11, 10, 8	29, 28, 27, 26, 25, 24, 23, 22, 12, 11, 8	Input	Address bus. A10 is the MSB, and A0 the LSB.
$\overline{CE1}$, $\overline{CE2}$	7, 32	7, 42	Input	$\overline{CE1}$ is used for even address control and $\overline{CE2}$ for odd address control. Both are active-low.
$\overline{OE}$	9	9	Input	This pin is used to read the contents of both attribute and common areas. Active-low.
$\overline{WE}$	36	15	Input	This pin is used to write the contents of both attribute and common areas. Active-low.
$\overline{IORD}$	34	44	Input	Used to read data from the I/O task file area. This pin is only valid when the card is set as an I/O card. Active-low.
$\overline{IOWR}$	35	45	Input	Used to write data to the I/O task file area. This pin is only valid when the card is set as an I/O card. Active-low.
$\overline{IREQ}$	37	16	Output	Interrupt request pin. When output is low, the card is requesting software service by the host. When output is high, the card is not requesting anything from the host.
$\overline{CD1}$, $\overline{CD2}$	26, 25	36, 67	Output	Used by the host to determine whether a card is inserted. These pins are connected to GND inside the card.
$\overline{IOIS16}$	24	33	Output	The output of this pin goes low when a task file register is accessed in 16-bit access mode.

Table 3.15 Pin Functions in I/O Mode (cont)

Abbreviation	Pin No. Compact Flash	Pin No. PC-ATA Card	Input/ Output	Function
$\overline{\text{REG}}$	44	61	Input	Input pin for switching between common and attribute area access. Drive high for common area access, and low for attribute area access. As the attribute area section is allocated to even addresses, D8–D15 are invalid in word access mode. In byte access, odd addresses are invalid.
$\overline{\text{STSCHG}}$	46	63	Output	Used to modify the configuration status register in the attribute memory area. Only valid in I/O card mode.
$\overline{\text{SPKR}}$	45	62	Output	As this card has no digital audio output function, the output of this pin is always high.
$\overline{\text{RESET}}$	41	58		All registers in the card can be cleared by high-level input at this pin. Initialization is then started, and RDY/BSY output goes high.
$\overline{\text{WAIT}}$	42	59	Output	I/O access or memory access cycle execution is kept waiting while the output of this pin is low.
$\overline{\text{INPACK}}$	43	60	Output	Used for input data buffer control. Selects the card and executes an I/O read cycle for the address pins. If the card gives an I/O read cycle reaction, a low level is output from the card.
$\overline{\text{VS1}}$	33, 40	43, 57	Output	Indicates the required input voltage value for this card (CIS information).
$\overline{\text{CSEL}}$	39	39	Input	Not used in memory card mode or I/O card mode.

3.5 True-IDE Specifications

The following requirements must be met in order to use a flash card in accordance with the True-IDE specifications. If these requirements are not met, the card will probably start up in memory mode. Once a card starts up as a PC-ATA card, it will operate as such until its power is turned off. True-IDE specifications cannot be selected by modifying registers during operation or by a reset.

- True-IDE setting procedure and precautions

1. Set the flash card $\overline{OE}$ pin ($\overline{ATASEL}$) to GND during the transition from power-off to power-on.
2. The $\overline{OE}$ pin ($\overline{ATASEL}$) must then be held low during use as a True-IDE specification card.

Notes:
1. When starting up as a True-IDE specification card, only I/O access is enabled.
2. Only the task file region can be accessed.
3. No memory areas can be accessed (including the attribute region); i.e., the $\overline{WE}$ and $\overline{OE}$ input pins cannot be used. It is recommended that $\overline{WE}$ and $\overline{OE}$ be pulled high.
4. The card will operate as a PC-ATA specification card if the $\overline{OE}$ setting is incorrect (including an incorrect setting due to noise, etc.) when performing hot-line insertion or removal, and particularly in the power-off → power-on sequence.
5. The selection of PC-ATA or True-IDE specifications is determined only in the power-on sequence. The state of $\overline{OE}$ is not checked in a reset.

When the True-IDE specifications are used, the access method is simpler than in other modes. The necessary peripheral circuitry is also comparatively small in scale, making this mode suitable for embedded applications. Once a card is used with the PC-ATA specifications, this does not mean that it can no longer be used as a PC card. For example, a flash card used as a True-IDE specification card in the user's own system can be used as a PC card without any problem if inserted in the PC card slot of a notebook PC.

In this case, however, although identification as hardware is possible, it will not be possible to read or write data if the actual file formats of the user's system and the PC are different. It is therefore advisable to use DOS format or similar file management in one's own system so that files can also be read in a PC environment.

The pin interface when using the True-IDE specifications is shown in tables 3.19 and 3.20. For the method of accessing the registers, and timing details, see tables 3.16 to 3.18, etc.

Table 3.16 True-IDE Specification Access

Register No.	Register Name	R/W	$\overline{CE2}$	$\overline{CE1}$	$\overline{IORD}$	$\overline{IOWR}$	A2	A1	A0	Attribute
0	Even data	R	H	L	L	H	0	0	0	R/W
		W			H	L				
1	Error REG.	R			L	H	0	0	1	R only
	Feature REG.	W			H	L				W only
2	Sector count	R			L	H	0	1	0	R/W
		W			H	L				
3	Sector no	R			L	H	0	1	1	R/W
		W			H	L				
4	Cylinder low	R			L	H	1	0	0	R/W
		W			H	L				
5	Cylinder high	R			L	H	1	0	1	R/W
		W			H	L				
6	Select card/head	R			L	H	1	1	0	R/W
		W			H	L				
7	Status	R			L	H	1	1	1	R only
	Command	W			H	L				W only
8	Alt status	R	L	H	L	H	1	1	0	R only
	Drive control	W			H	L				W only
9	Drive address	R			L	H	1	1	1	R only
	Reserved	W			H	L				W only

Table 3.17 True-IDE Read Timing

No.	Item	Symbol	Min [ns]	Max [ns]
1	Data delay after IORD	t_D (IORD)		100
2	Data hold following IORD	t_H (IORD)	0	
3	IORD width time	t_{WIORD}	165	
4	Address setup before IORD	t_{SUA} (IORD)	70	
5	Address hold following IORD	t_{HA} (IORD)	20	
6	CE setup before IORD	t_{SUCE} (IORD)	5	
7	CE hold following IORD	t_{HCE} (IORD)	20	
8	IOIS16 delay falling from IORD	$t_{DFIOIS16}$ (Add)		35
9	IOIS16 delay rising from IORD	$t_{DRIOIS16}$ (Add)		35

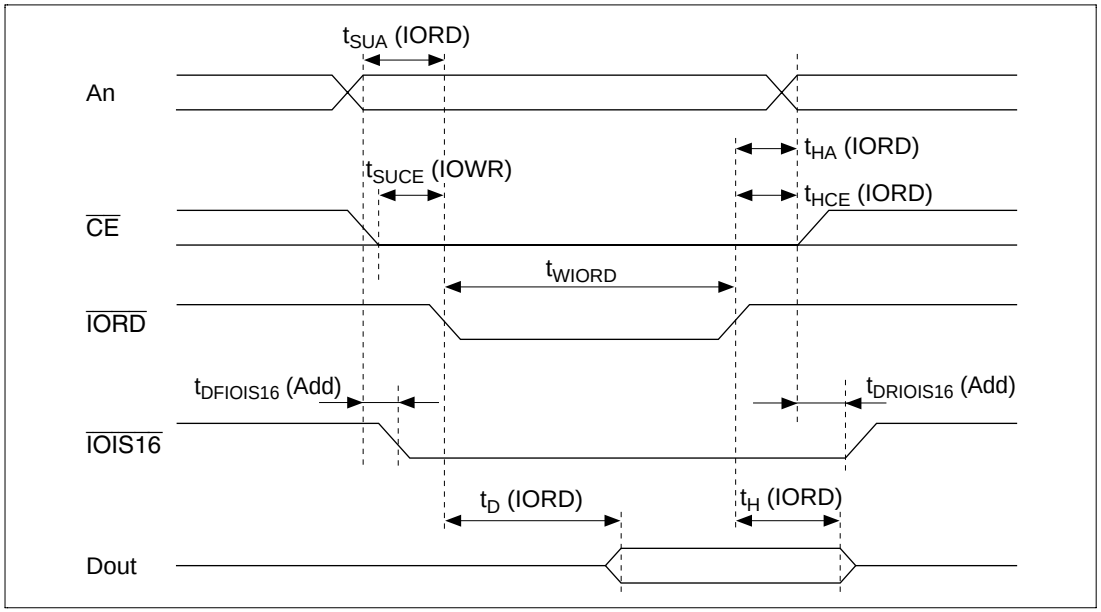


Figure 3.9 True-IDE Read Timing Chart

Note: The maximum load for $\overline{\text{WAIT}}$, $\overline{\text{INPACK}}$, and $\overline{\text{IOIS16}}$ is one 50 pF LS-TTL in total. In a read, the time from the point at which $\overline{\text{WAIT}}$ goes high until $\overline{\text{IORD}}$ goes high is 0 ns or more.

Table 3.18 True-IDE Write Timing

No.	Item	Symbol	Min [ns]	Max [ns]
1	Data setup before IOWR	t_{SU} (IOWR)	60	
2	Data hold folowing IOWR	t_{H} (IOWR)	30	
3	IOWR pulse width	t_{WIOWR}	165	
4	Address setup before IOWR	t_{SUA} (IOWR)	70	
5	Address hold following IOWR	t_{HA} (IOWR)	20	
6	CE setup before IOWR	t_{SUCE} (IOWR)	5	
7	CE hold following IOWR	t_{HCE} (IOWR)	20	
8	IOIS16 delay falling from IOWR	$t_{DFIOIS16}$ (Add)		35
9	IOIS16 delay rising from IOWR	$t_{DRIOIS16}$ (Add)		35

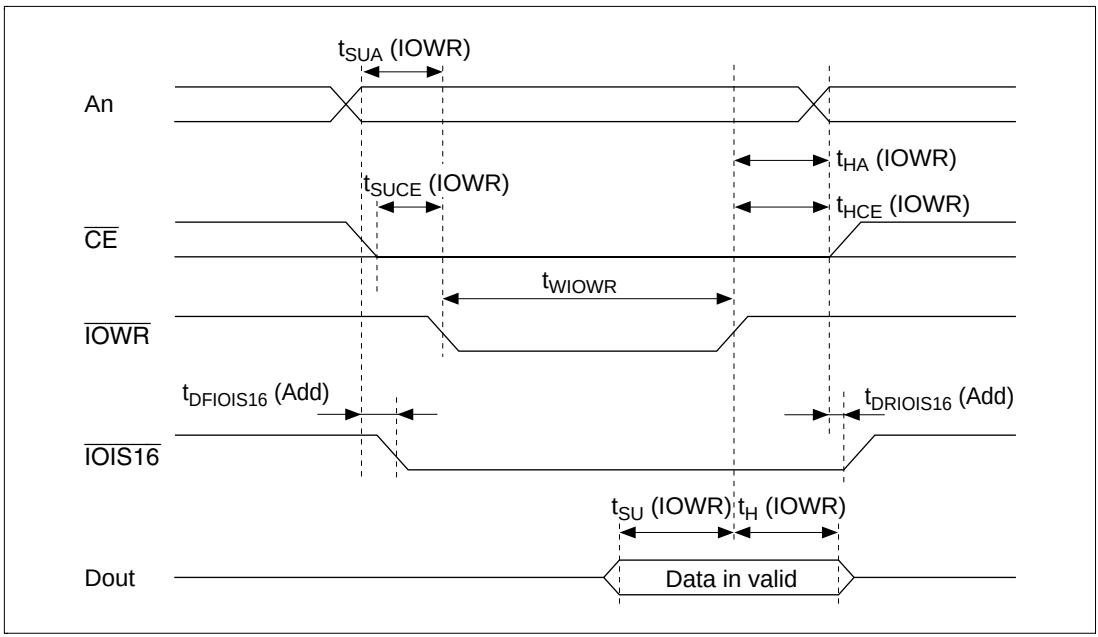


Figure 3.10 True-IDE Write Timing Chart

Note: The maximum load for $\overline{\text{WAIT}}$, $\overline{\text{INPACK}}$, and $\overline{\text{IOIS16}}$ is one 50 pF LS-TTL in total. In a write, the time from the point at which $\overline{\text{WAIT}}$ goes high until $\overline{\text{IOWR}}$ goes high is 0 ns or more.

Table 3.19 Pin Arrangement when Using True-IDE Specifications

CompactFlash™

Pin No.	True-IDE	Pin No.	True-IDE
1	GND	26	$\overline{CD1}$
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	$\overline{CE1}$	32	$\overline{CE2}$
8	A10	33	$\overline{VS1}$
9	$\overline{ATASEL}$	34	$\overline{IORD}$
10	A9	35	$\overline{IOWR}$
11	A8	36	$\overline{WE}$
12	A7	37	INTRQ
13	V_{CC}	38	V_{CC}
14	A6	39	$\overline{CSEL}$
15	A5	40	$\overline{VS2}$
16	A4	41	$\overline{RESET}$
17	A3	42	IORDY
18	A2	43	$\overline{INPACK}$
19	A1	44	$\overline{REG}$
20	A0	45	$\overline{DASP}$
21	D0	46	$\overline{PDIAG}$
22	D1	47	D8
23	D2	48	D9
24	$\overline{IOIS16}$	49	D10
25	$\overline{CD2}$	50	GND

Table 3.20 Pin Functions when Using True-IDE Specifications

Abbre-viation	Pin No. CompactFlash™	Input/Output	Function
V_{CC}	13, 38	Input	Power supply pins
GND	1, 50	Input	GND pins
D0–D15	21, 22, 23, 2, 3, 4, 5, 6, 47, 48, 49, 27, 28, 29, 30, 31	Input/Output	Data bus. D0–D7 comprise the even byte of a word, and D8–D15 the odd byte. D0 and D8 are the respective LSBs.
A0–A10	20, 19, 18, 17, 16, 15, 14, 12, 11, 10, 8	Input	One register in the task file area can be selected using A0–A2. Other address pins should be dropped to GND on the host side.
$\overline{CE1}$, $\overline{CE2}$	7, 32	Input	$\overline{CE2}$ is used to select the alternate status register and device control register in the task file area. $\overline{CE1}$ is used to select other registers in the task file area.
$\overline{ATASEL}$	9	Input	True-IDE mode can be selected by dropping this pin to GND on the host side.
$\overline{WE}$	36	Input	Not used. Connect to V_{CC} on the host side.
$\overline{IORD}$	34	Input	Used to read data from the I/O task file area. This pin is only valid when the card is set as an I/O card. Active-low.
$\overline{IOWR}$	35	Input	Used to write data to the I/O task file area. This pin is only valid when the card is set as an I/O card. Active-low.
$\overline{INTRQ}$	37	Output	Pin for interrupt requests to the host. Active when the output is high.
$\overline{CD1}$, $\overline{CD2}$	26, 25	Output	Used by the host to determine whether a card is inserted. These pins are connected to GND inside the card.
$\overline{IOIS16}$	24	Output	A low level at this pin indicates that the card is requesting a word data transfer cycle.
$\overline{REG}$	44	Input	Not used. Connect to V_{CC} on the host side.
$\overline{PDIAG}$	46	Output	The Pass Diagnostic signal in the master-slave handshake protocol.
$\overline{DASP}$	45	Output	The Disk Active/Slave Present signal in the master-slave handshake protocol.
RESET	41		Low-level input to this pin from the host causes a hardware reset.

Table 3.20 Pin Functions when Using True-IDE Specifications (cont)

Abbre-viation	Pin No. CompactFlash™	Input/Output	Function
$\overline{\text{WAIT}}$	42	Output	I/O access or memory access cycle execution is kept waiting while the output of this pin is low.
—	43	Output	Not used. Leave open.
$\overline{\text{VS1}}$	33, 40	Output	Indicates the required input voltage value for this card (CIS information).
$\overline{\text{CSEL}}$	39	Input	Pulled up internally. Dropping this pin to GND selects master mode, while leaving it open selects slave mode.

Section 4 Basic Operation and Method of Use of Flash Cards

This section describes the tasks that should be performed when a flash card is powered on, and the basic ATA commands used when actually reading the card.

ATA commands are basically a set of instructions for controlling an ATA-specification hard disk drive, but as they comprise an extremely rationalized set of instructions, they can also be used for other storage media devices. These commands are used to execute flash card reads, writes and other operations.

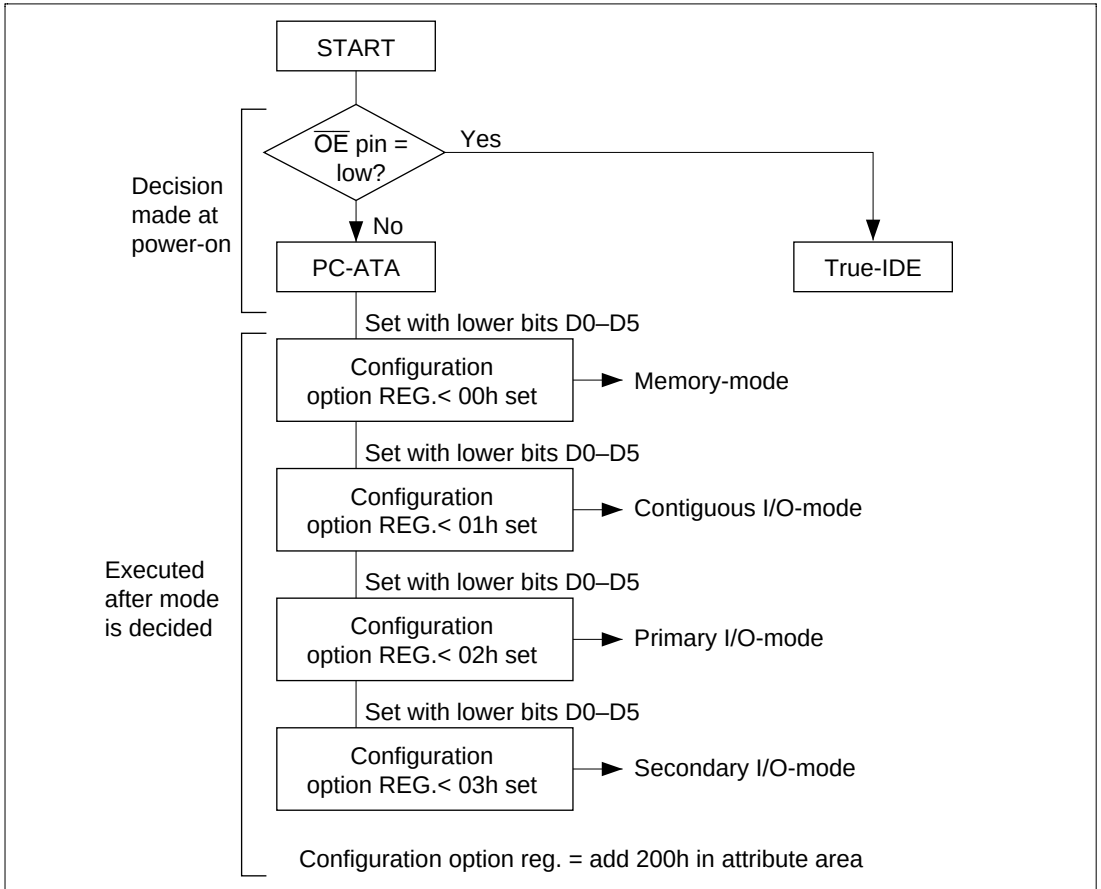
4.1 Start-Up in Each Mode

The flash cards covered in this manual are the PC-ATA card (a PC card type flash card) and the postage-stamp sized CF. With both of these cards, either of the following modes can be selected by a pin setting at power-on.

1. PC-ATA specification mode
2. True-IDE specification mode

The PC-ATA specification mode is further subdivided into four access modes. When the card is powered on, a transition is made to the respective address mode according to settings made in the configuration registers.

Figure 4.1 shows an outline flowchart of the access mode setting procedure. The setting procedures in each access mode are described in the following section.



Note: The lower 6 bits (D0–D5) of the configuration option register are used for mode setting. D6 determines whether level or pulse mode is used for the interrupt signal.
D6 < 1: Level-mode interrupts
D6 < 0: Pulse-mode interrupts

D7 is the software reset bit.
D7 < 1: Software reset executed
* All registers are cleared to 0.
D7 < 0: Software reset cleared

Figure 4.1 Flash Card Access Mode Setting Flowchart

4.1.1 Switching between True-IDE and PC-ATA Specifications

Switching between True-IDE and PC-ATA specifications is performed at power-on.

Once the card starts up in a particular mode, the mode can only be switched by powering on again.

The mode cannot be switched by means of a hardware or software reset.

Mode switching is performed by confirming the $\overline{\text{ATASEL}}$ (OE pin) potential. $\overline{\text{ATASEL}}$ (OE pin) checking is only performed at power-on.

Table 4.1 shows the relationship between the $\overline{\text{ATASEL}}$ potential referenced at power-on and switching between PC-ATA specifications and True-IDE specifications.

Table 4.1 Mode Switching

No.	Mode	$\overline{\text{ATASEL}}$ Potential	Notes
1	PC-ATA	H	Subsequently operates as $\overline{\text{OE}}$
2	True-IDE	L	Subsequently must constantly be held low

Note: If the $\overline{\text{ATASEL}}$ potential is set to the low level on the host side at power-on, but the card identifies a high level due to noise, etc., the card will start up in PC-ATA mode. Adequate noise prevention measures are therefore required for this pin.

4.2 Access Mode Switching when Using PC-ATA Specifications

In broad terms, the PC-ATA specifications include two access modes:

1. Memory Mode
2. I/O mode

The I/O mode is further subdivided into the following three access modes:

1. Primary I/O mode
2. Secondary I/O mode
3. Contiguous I/O mode

There are thus four access modes in all. (See section 3 for the access method in each mode, and timing details.)

The differences between these operating modes are determined by the addresses to which the host allocates the task file register section with respect to the card.

The register that sets these operating modes is the configuration option register in the attribute region. The location of the task file region is determined by a setting in this register. Basically, the task file registers can be allocated to both memory space and I/O space according to the setting in this register.

The ability to change task file region addresses in this way is essential in order to maintain the general applicability of the PC card. For example, while a memory card supports the four access modes listed above, with fax, SCSI, and other cards, there are cases where only I/O mode access is enabled, or where a task file region address is booked as the address of another I/O device for reasons related to control on the host side. A flexible approach to register allocation is necessary in order to avoid problems in such cases.

What, then, is the best access mode to use, as viewed from the system side?

In a system using an MPU with no I/O-related pins such as IOWR and IORD, for example, it may be easier to use the card in memory mode, since both the attribute region and the task file region are allocated to memory space in this mode. In other words, control can be performed with the RD and WR signals, without the need for IOWR and IORD. In I/O mode, on the other hand, the $\overline{RD}$ and $\overline{WR}$ signals are used for read and write accesses to the attribute region, while the IOWR and IORD signals are used for accesses to the task file region. The number of signals used is thus greater than in memory mode.

In any case, the access mode should be set for the card according to the system in which it is used.

4.2.1 Initialization (Access Mode Setting, Etc.)

After powering on in PC-ATA mode, as described in section 4.1.1, the first requirement is to acquire card attribute data from the CIS section. The CIS section, as the name Card Information Structure suggests, is a memory area that holds card attribute information. This information includes the card's operating voltage, the address of the configuration register section, and so on. The CIS section is a ROM area in which only read access can be performed.

At first glance, reading the card information may seem unnecessary when always using a card of the same model and capacity from the same manufacturer. In some cases, there may be no problem if reading of the card attribute information is ignored. But with the possibility of future revisions in the standards, sufficient system flexibility should be provided to enable any manufacturer's cards to be used. It is therefore probably advisable to enable a CIS section read to be performed in terms of hardware, even if a card attribute check is not performed by the driver software.

The CIS section holds a large amount of card attribute information. Actually reading all of this data would be a considerable task, but the contents of the six registers shown in table 4.2, at least, should be acquired.

Table 4.2 CIS Section Data Acquisition

No.	Tuple Identifier	Tuple Code	Description and Comments
1	01h	CISTPL_DEVICE	Device information. This tuple information is not necessary for memory cards, but is essential for fax, LAN, and other I/O cards.
2	15h	CISTPL_VERS_1	Product information. Includes the product information string, product name, product number, and other manufacturer information.
3	1Ah	CISTPL_CONF	Crucial information. Indicates the locations of the configuration registers and their presence. Configuration register allocation should be set on the basis of this information.
4	1Bh	CISTPL_CE	Configuration table entry. Appropriate configuration items are specified, including I/O space, interrupts, memory, etc.
5	20h	CISTPL_MANFID	Manufacturer's identification. Holds the name of the card manufacturer.
6	21h	CISTPL_FUNCID	Function identifier. Provides function information concerning the card. Also includes system initialization information.

If information other than that shown above is needed, refer to the appendices or the data sheet.

The most important information in the above table is item 3, CISTPL_CONF, which holds the addresses of the configuration registers. In current (June 1997) cards, the configuration registers are assigned to even addresses starting at 200h in the attribute region, but this allocation may change in the future. The configuration register address allocation should therefore be determined on the basis of information read from the CIS section.

The internal arrangement of the configuration registers, and the various settings, are described on the following pages.

Register Name: Configuration Option
Address: 200h in attribute memory
Use: Card mode setting, interrupt level setting, software reset

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Conf0–5: The host can set the card access mode by making settings as shown in the following table.

	Conf2–5	**Conf1**	**Conf0**
Memory	0	0	0
Contiguous I/O	0	0	1
Primary I/O	0	1	0
Secondary I/O	0	1	1

Note: Conf2–5 must always be cleared to 0.

LevelREQ: This bit is used to switch the interrupt signal mode.
0: Pulse mode interrupts
1: Level mode interrupts

SRESET: This bit can be used to execute a software reset.
1. Set SRESET bit (D7) to 1: Reset executed
2. Wait for time required for reset: 250 ms or more
3. Clear SRESET bit (D7) to 0: Reset cleared
   The reset is not cleared unless SRESET is cleared to 0.
   This differs from the case of hardware reset execution.

A reset clears all configuration register bits.

Register Name: Card Configuration & Status
Address: 202h in attribute memory
Use: Indicates the card status.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed: Indicates that 1 has been set in either the CRdy or CWProt bit in Pin ReplacementREG.
In I/O mode, the $\overline{\text{STSCHG}}$ pin output is held low if this bit is set when the SigChg bit is 1.

SigChg: Clearing of this bit to 0 by the host allows the Changed bit and $\overline{\text{STSCHG}}$ bit to be disabled by the card. In this case, the $\overline{\text{STSCHG}}$ signal output is always “High level”

IOis8 When 8-bit I/O access is performed, the host should set this bit to 1.
With CompactFlash™, this bit has no meaning, since whether 8- or 16-bit access is used is of no particular concern.

PwrDwn: Setting this bit to 1 switches to power saving mode. Clearing this bit to 0 restores normal mode.
When this bit changes, the card sets “Busy” and the Busy state is maintained until the mode changes.
Hitachi cards also have an automatic power saving mode, so there will probably be few occasions to use this bit.

INT: This bit indicates the interrupt state. It is set to 1 by the card when the host issues a read request, etc., to the card, and remains set to 1 until the interrupt source has been serviced.
This bit can be disabled by the $\overline{\text{IEN}}$ bit in the device control register. In this case, this bit holds a value of 0.

Register Name: Pin Replacement
Address: 204h in attribute memory
Use: Indicates the card status.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	0	0	Rdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

Rdy/-Bsy: The host can identify the Rdy/-Bsy state by reading the state of this bit.
In I/O access mode, in particular, the Rdy/-Bsy bit is replaced by the IREQ pin, but in this case too, the Rdy/-Bsy state can be identified by means of this bit.

CRdy/-Bsy: When the Rdy/-Bsy bit changes, the card sets this bit to 1.
This bit can be modified by the host.

RWProt: Indicates whether the card is in the write-protect state.
Hitachi cards do not support a write-protect function, so this bit is always cleared to 0. Support for this function is not included in the CompactFlash™ standards, either.

CWProt: When the RWProt bit changes, the card sets this bit to 1. Since the RWProt bit is never used, this bit is always 0.
This bit can be modified by the host.

MRdy/-Bsy: Functions as a mask for write information to the CRdy/-Bsy bit. See the table below.

MWProt: Functions as a mask for write information to the CWProt bit. See the table below.

	Written by Host			
Initial Value of (C) Status	**“C” Bit**	**“M” Bit**	**Final “C” Bit**	**Command**
0	×	0	0	Unchanged
1	×	0	1	Unchanged
×	0	1	0	Cleared by host
×	1	1	1	Set by host

Register Name: Socket and Copy
Address: 206h in attribute memory
Use: Used for drive number setting.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive#	0	0	0	0
Write	0	0	0	Drive#	×	×	×	×

Reserved: Reserved for future use. When actually used, cleared to 0.

Drive#: Indicates the number assigned to the drive in a system with a twin card configuration.
With CompactFlash™, a twin card configuration is not supported, so this bit should always be cleared to 0.

4.3 Switching Access Modes when Using True-IDE Specifications

Holding $\overline{\text{ATASEL}}$ (the OE pin) low when power is turned on causes the flash card to operate as a True-IDE specification card. The $\overline{\text{ATASEL}}$ pin must then be held low continuously.

There are not a number of different access modes, as in the case of the PC-ATA specifications. The task file region is fixed and access is only possible in the I/O space, giving in effect only one access mode.

The features of these specifications are as follows.

(1) The location of the task file region is fixed, and cannot be varied.
(2) Form (1), it follows that access mode setting and other initialization tasks are not necessary.
(3) Only I/O space can be accessed.
(4) From (3), it follows that access is not possible anywhere in the memory space, including the attribute region. With the PC-ATA specifications, therefore, its is not possible to access the configuration registers or the CIS section.

For information on accesses after start-up, see the description of the True-IDE specifications in section 3.

These specifications comprise a single, independent set of specifications, and are not a part of the PC card standard, as in the case of the PC-ATA specifications.

The merit of these specifications is precisely that they are exclusively for handling a flash card as a hard disk drive. Therefore, if the system side is specialized toward these specifications, it cannot support a variety of different cards as in the case of the PCMCIA standard. These specifications thus lack general applicability, but on the other hand, enable extremely simple circuitry and driver software to be used.

Now that PC-ATA specifications and True-IDE specifications have been described, there is the question of the choice of slot—PC-ATA compatible or True-IDE compatible—considered from the system side.

True-IDE Specification Compatibility: If the user is prepared to use a card slot exclusively for dedicated flash memory card use, as long as an auxiliary storage medium can be mounted, use with the True-IDE specifications is the easiest approach. Actual access is easy, and there are far fewer control signals than in the case of a PC card, so that peripheral circuitry and driver software for the card can also be kept simple. This is the best solution if a flash card is to be used simply as a storage medium.

However, if a card slot supporting only the True-IDE specifications is decided on, it will not be possible to support cards with different functions, as provided for in the PCMCIA standard, and it will probably never be possible to insert anything but a True-IDE specification flash card.

PC-ATA Specification Compatibility (PCMCIA Standard Compatibility): If the possibility of using cards with various functions, such as fax/LAN and SCSI cards, in addition to flash cards is considered, it is obvious that the design should provide for a card slot offering PCMCIA compatibility. However, the operating circuitry is rather more complex than for the use of a True-IDE specification card slot, and support must be provided for a variety of driver software, so that the scale of both hardware and software can be expected to be greater. In this case, hardware implementation will be made easier by using an MPU already equipped with a PCMCIA interface, or a commercially available PC card controller chip.

MPUs equipped with a PCMCIA interface include the SH7708 and SH7709 (SH3) in Hitachi's SuperH microcomputer series.

4.4 Overview of ATA Commands

ATA commands are codes for controlling actual read/write operations, that are set in the command register, one of the registers in the task file region. A flash card has approximately 30 commands, but for the sake of brevity only the following five basic commands are outlined here.

1. Format
2. Erase Sector(s)
3. Stand-By
4. Read Sector(s)
5. Write Sector(s)

These commands are described below.

Table 4.3 lists the registers referenced by each command.

Table 4.3 Basic ATA Commands

No.	Class	Command Name	Code [Hex]	FR	SC	SN	CY	DH	LBA
1	2	Format track	50	—	Y	—	Y	Y	Y
2	1	Erase sector(s)	C0	—	Y	Y	Y	Y	Y
3	1	Stand by	E2 or 96	—	—	—	—	D	—
4	1	Read sector(s)	20 & 21	—	Y	Y	Y	Y	Y
5	2	Write sector(s)	30 & 31	—	Y	Y	Y	Y	Y

The meaning of the abbreviations used in table 4.3 is as follows.

FR	Feature register
SC	Sector count
SN	Sector number
CY	Cylinder registers
DH	Card/drive/head register
LBA	Logical block address mode

“Y” in the table means that the register is referenced when the ATA command is executed. For the drive/head register, “Y” means that both the “Drive” and “Head” parameters are referenced, while “D” means that only the “Drive” parameter is referenced.

ATA commands are divided into classes according to the execution mode, as shown below.

Class 1	Bsy is set within 400 ns after command execution.
Class 2	Bsy is set and the sector buffer for receiving write data from the host is prepared within 400 ns after command execution. DRQ is set within 700 µs, and Bsy is cleared within 400 ns after this.
Class 3	Bsy is set and the sector buffer for receiving write data from the host is prepared within 400 ns after command execution. DRQ is set within 20 ms, and Bsy is cleared within 400 ns after this.

Further details of ATA commands can be found in the specifications issued by the following organizations:

1. ATA1 or ATA2 standard issued by ANSI (American National Standards Institute)
2. CompactFlash™ standard specification issued by the CFA
3. PCMCIA2.1 issued by the PCMCIA
4. Hitachi flash card data sheet

Command Name: Format Track

Bit		7	6	5	4	3	2	1	0
Command	7	50							
C/D/H	6	1	LBA	1	Drive	Head (LBA27–24)			
Cyl High	5	Cylinder High							
Cyl Low	4	Cylinder Low							
Sec Num	3	× (LBA7–0)							
Set Cnt	2	Count (LBA mode only)							
Feature	1	×							

When a card receives this command, it writes FF to all 32 sectors for the specified drive, cylinder, and head. In executing this command, it is assumed that write data is transferred from the host in the same way as with the WriteSector(s) command, but the received data is not actually written. The purpose of this is to maintain compatibility with the standard ATA commands.

When operating in LBA mode, the card writes the numeric value specified in the SectorCount register to the sectors.

Command Name: Erase Sector

Bit		7	6	5	4	3	2	1	0
Command	7	C0							
C/D/H	6	1	LBA	1	Drive	Head (LBA27–24)			
Cyl High	5	Cylinder High (LBA23–16)							
Cyl Low	4	Cylinder Low (LBA15–8)							
Sec Num	3	Sector Number (LBA7–0)							
Set Cnt	2	Sector Count							
Feature	1	×							

This command is basically only an erase command, but in fact also handles updating of header information. Consequently, it is also assumed that errors will occur due to write abnormalities, and so this must be taken into account when writing programs.

Note: Header information: Corresponds to HDD servo information.
There is individual header information for each sector, containing information such as the logical address of the sector and the number of times the sector has been rewritten.

Command Name: Stand By

Bit		7	6	5	4	3	2	1	0
Command	7	E2 or 96							
C/D/H	6	×			Drive	×			
Cyl High	5	×							
Cyl Low	4	×							
Sec Num	3	×							
Set Cnt	2	×							
Feature	1	×							

After receiving this command, the card generates an interrupt immediately after (1) Bsy setting → (2) sleep mode transition* → Bsy clearing processing.

Standby mode can only be cleared by issuance of another command by the host.

When standby is cleared, reset processing can be carried out, but this is not essential.

Note: * Corresponds to standby mode in the ATA standard.

Command Name: Read Sector(s)

Bit		7	6	5	4	3	2	1	0
Command	7	20 & 21							
C/D/H	6	1	LBA	1	Drive	Head (LBA27–24)			
Cyl High	5	Cylinder High (LBA23–16)							
Cyl Low	4	Cylinder Low (LBA15–8)							
Sec Num	3	Sector Number (LBA7–0)							
Set Cnt	2	Sector Count							
Feature	1	×							

When this command is issued, the number of sectors set in the SectorCount register can be read, starting at the sector set in the SectorNumber register. A value of 01H to 0FFH can be set in the SectorCount register. Inputting 00H is equivalent to inputting FFH.

When the card receives this command, it performs the following operations:

1. If there is unprocessed data left in the sector buffer for any reason, the card waits until that data has been processed.

2. Bsy setting → data setting in sector buffer → DRQ setting → Bsy clearing

3. Interrupt generation

4. Data can then be fetched from the sector buffer.

5. If the processing ends normally, the following data is set in the CommandBlock register:
   — Last read cylinder number, head number, and sector number

6. If the processing ends abnormally, the operation in which the error occurred is aborted, and the following data is set in the CommandBlock register:
   — Cylinder number, head number, and sector number at which the error occurred
   The data in the sector buffer is the data of the sector in which the error occurred.

Command Name: Write Sector(s)

Bit		7	6	5	4	3	2	1	0
Command	7	30 & 31							
C/D/H	6	1	LBA	1	Drive	Head (LBA27–24)			
Cyl High	5	Cylinder High (LBA23–16)							
Cyl Low	4	Cylinder Low (LBA15–8)							
Sec Num	3	Sector Number (LBA7–0)							
Set Cnt	2	Sector Count							
Feature	1	×							

When this command is issued, the number of sectors set in the SectorCount register can be written, starting at the sector set in the SectorNumber register. A value of 01H to FFH can be set in the SectorCount register. Inputting 00H is equivalent to inputting FFH.

When the card receives this command, it performs the following operations:

1. Bsy setting → data setting in sector buffer → DRQ setting → Bsy clearing

2. Waits for 512 bytes of data to be sent by the host.
   An interrupt is not generated at this time, as in the case of a read operation.
   The host must not perform data transfer until $\overline{\text{Bsy}}$ is cleared.

3. If the processing ends normally, the following data is set in the CommandBlock register:
   — Last read cylinder number, head number, and sector number

4. If the processing ends abnormally, the operation in which the error occurred is aborted, and the following data is set in the CommandBlock register:
   — Cylinder number, head number, and sector number at which the error occurred
   The data in the sector buffer is the data of the sector in which the error occurred.
   The host can find out what kind of error occurred in which sector by accessing the CommandBlock register.

Section 5 Application Examples for Systems with Embedded CF

When a flash card is used for an embedded application, the application can be implemented most easily by using the True-IDE specifications. If the use of PC cards for various purposes is envisaged, it is probably better to use a PC card controller chip employed in notebook PCs, etc., or to use an MPU with a PCMCIA interface (such as the SH3, SH7708, or SH7709 in Hitachi's SuperH microcomputer series) as the CPU. This is because, while the level of general applicability is high with the PC-ATA specifications, a large number of conditions have to be satisfied, resulting in a proportionate increase in the size of both hardware and software. Thus it is extremely difficult to implement peripheral circuitry using TTL devices, etc.

If the True-IDE specifications are used, on the other hand, an interface circuit can be implemented very easily, as shown in figure 5.1, Block Diagram, on the next page. The down side is that it is not possible to use a variety of PC cards. This configuration only provides for the use of a flash card in the same way as a hard disk drive.

5.1 True-IDE Interface Block Circuit

5.1.1 Outline

Use of this circuit presupposes the following conditions. This circuit should not be used unless these conditions are accepted.

- This circuit is subject to the conditions listed in section 5.1.2, Notes, and is only a reference example.
- Hitachi, Ltd., accepts no responsibility for any problems arising out of the use of this circuit.
- No engineering services have been implemented with regard to the contents of this circuit.
- This circuit may be freely used by anybody.

5.1.2 Notes

(1) Hitachi PCMCIA PC-ATA specification card: Use an HB286***AT or later model.

(2) (1) or Hitachi CompactFlash™: Use an HB286***C*.

(3) Use the True-IDE specifications.

(4) The third party below provides support for driver software. Inquiries should be directed to the address shown.

AI Corporation, Production Department
IIjima Bldg. 6F, Nishi-Gotanda 2-25-2, Shinagawa-ku, Tokyo
Tel: (03) 3493-7981
Fax: (03) 3493-7993

Sample Interface Circuit when Using True-IDE Mode

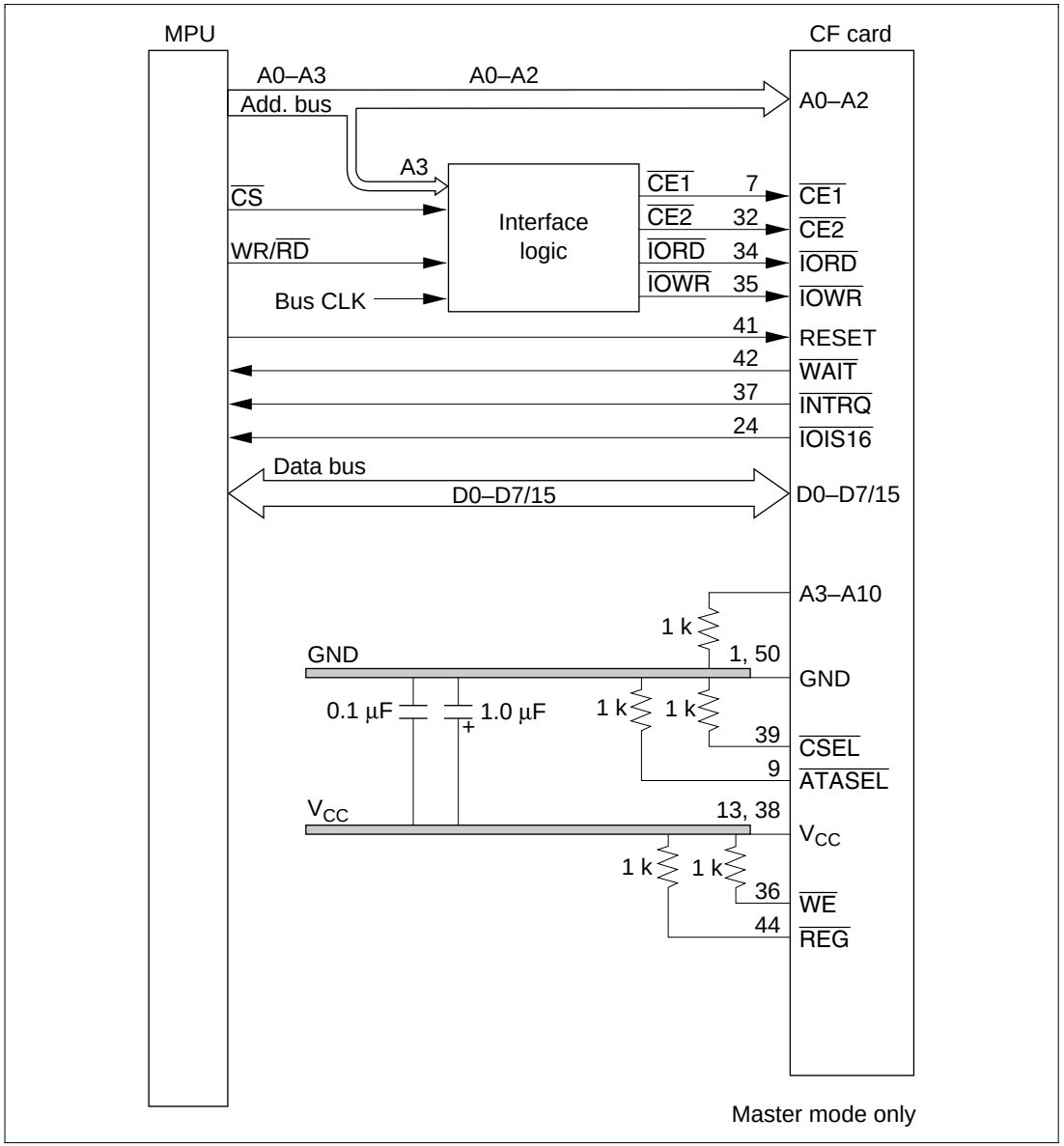


Figure 5.1 Block Diagram

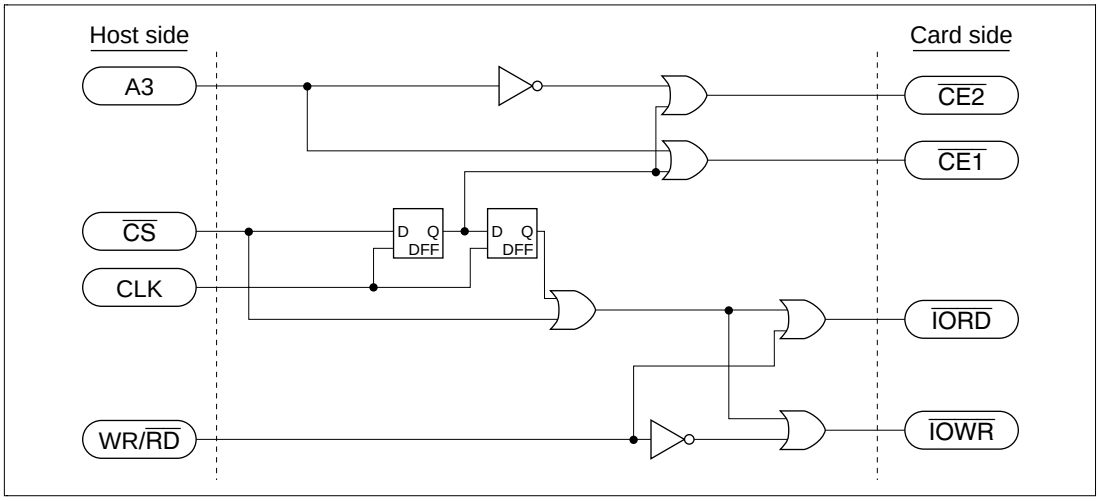


Figure 5.2 Interface Logic

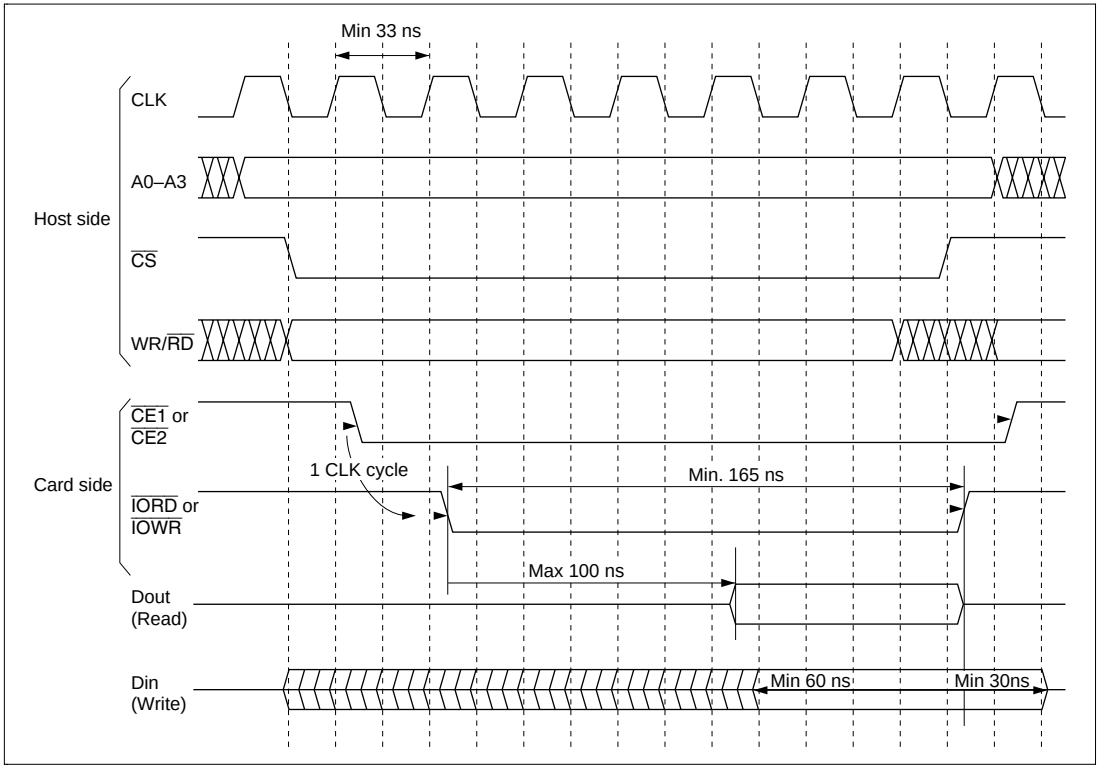


Figure 5.3 Interface Logic Timing Waveforms

Table 5.1 True-IDE Mode Access

Register No.	Register Name	R/W	WR/$\overline{RD}$	A3	A2	A1	A0	Attribute
0	Even data	R	L	0	0	0	0	R/W
		W	H					
1	Error REG.	R	L	0	0	0	1	R only
	Feature REG.	W	H					W only
2	Sector count	R	L	0	0	1	0	R/W
		W	H					
3	Sector no	R	L	0	0	1	1	R/W
		W	H					
4	Cylinder low	R	L	0	1	0	0	R/W
		W	H					
5	Cylinder high	R	L	0	1	0	1	R/W
		W	H					
6	Select card/head	R	L	0	1	1	0	R/W
		W	H					
7	Status	R	L	0	1	1	1	R only
	Command	W	H					W only
8	Alt status	R	L	1	1	1	0	R only
	Drive control	W	H					W only
9	Drive address	R	L	1	1	1	1	R only
	Reserved	W	H					W only

5.2 Connector Information

The products shown below are available as sockets for use when providing a PC card or CF slot. (The following products are not guaranteed or recommended by Hitachi.)

1. For PC card slot

Manufacturer	Product Code	
Matsushita Electric Works, Ltd.	AXP121121	(Header; with ejector; 1 slot)
Matsushita Electric Works, Ltd.	AXP122121	(Header; with ejector; 2 slot)
Matsushita Electric Works, Ltd.	AXP121122	(Header; with ejector; 1 slot)
Matsushita Electric Works, Ltd.	AXP122122	(Header; with ejector; 2 slot)
AMP	177961-1	(Header; with ejector; 1 slot)
AMP	177964-1	(Header; with ejector; 1 slot)

2. For CompactFlash™

Manufacturer	Product Code	
3M	N7E50-7516VY-20	(Header)
3M	D7E50-7516-02	(Ejector)
JAE	JC26-CS20LH	(Header; with ejector)
JAE	JC26-CS20L	(Header; without ejector)
JST	ICM-MA50H-SS52	(Header)
Hosiden Corporation	CCD3003-010020	(Header)
Hosiden Corporation	CCD3003-010010	(Header)
Hosiden Corporation	CCD3003-010100	(Ejector)

Note: CompactFlash™ can also be mounted in a PCMCIA slot (Type II or Type III) by inserting it in a special adapter. PC card adapters are available from any bulk electrical products supplier.

Appendix A CIS Information

CIS addresses are defined as shown below, starting at address 000H in the attribute region. These addresses are read-only.

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
000H	01H	CISTPL DEVICE								Device info tuple	Tuple code
002H	04H	TPL_LINK								Link length is 4 byte	Link to next tuple
004H	DFH	Device type				WPS	Device speed			Device type = DH: I/O device WPS = 0: No WP Device speed = 7: ext speed	Device type, WPS, speed
006H	4AH	EXT	Speed mantissa				Speed exponent			400 ns if no wait	Extended speed
008H	01H	1x					2k units			2 kbyte of address space	Device size
00AH	FFH	List end marker								End of device	END marker
00CH	1CH	CISTPL DEVICE OC								Other conditions device info tuple	Tuple code
00EH	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
010H	02H	EXT	Reserved				V_{CC}		MWAIT	3 V, wait is used	Other conditions info field
012H	D9H	Device type				WPS	Device speed			Device type = DH: I/O device WPS = 0: No WP Device speed = 1: 250 ns	Device type, WPS, speed
014H	01H	1x					2 k units			2 kbyte of address space	Device size
016H	FFH	List end marker								End of device	END marker
018H	18H	CISTPL JEDEC C								JEDEC ID common memory	Tuple code
01AH	02H	TPL_LINK								Link length is 2 bytes	Link to next tuple
01CH	DFH	PCMCIA's manufacturer's JEDEC ID code								Manufacturer's ID code	JEDEC ID of PC Card ATA
01EH	01H	PCMCIA JEDEC device code								2nd byte of JEDEC ID	
020H	20H	CISTPL MANFID								Manufacturer's ID code	Tuple code
022H	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
024H	07H	Low byte of PCMCIA manufacturer's code								HITACHI JEDEC manufacturer's ID	Low byte of manufacturer's ID code
026H	00H	High byte of PCMCIA manufacturer's code								Code of 0 because other byte is JEDEC 1 byte manufac ID	High byte of manufacturer's ID code
028H	00H	Low byte of product code								HITACHI code for PC CARD ATA	Low byte of product code
02AH	00H	High byte of product code									High byte of product code

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
02CH	15H	CISTPL_VER_1								Level 1 version/product info	Tuple code
02EH	15H	TPL_LINK								Link length is 15h bytes	Link to next tuple
030H	04H	TPPLV1_MAJOR								PCMCIA2.0/JEIDA4.1	Major version
032H	01H	TPPLV1_MINOR								PCMCIA2.0/JEIDA4.1	Minor version
034H	48H									‘ H ’	Info string 1
036H	49H									‘ I ’	
038H	54H									‘ T ’	
03AH	41H									‘ A ’	
03CH	43H									‘ C ’	
03EH	48H									‘ H ’	
040H	49H									‘ I ’	
042H	00H									Null terminator	
044H	46H									‘ F ’	Info string 2
046H	4CH									‘ L ’	
048H	41H									‘ A ’	
04AH	53H									‘ S ’	
04CH	48H									‘ H ’	
04EH	00H									Null terminator	
050H	32H									‘ 2 ’	Vender specific strings
052H	2EH									‘ . ’	
054H	30H									‘ 0 ’	
056H	00H									Null terminator	
058H	FFH	List end marker								End of device	END marker
05AH	21H	CISTPL MANFID								Function ID tuple	Tuple code
05CH	02H	TPL_LINK								Link length is 2 bytes	Link to next tuple
05EH	04H	TPLFID_FUNCTION = 04H								Disk function, may be silicon, may be removable	PC card function code
060H	01H	Reserved						R	P	R = 0: No BIOS ROM P = 1: Configure card at power on	System initialization byte

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
062H	22H	CISTPL FUNCE								Function extension tuple	Tuple code
064H	02H	TPL_LINK								Link length is 2 bytes	Link to next tuple
066H	01H	Disk function extension tuple type								Disk interface type	Extension tuple type for disk
068H	01H	Disk interface type								PC card ATA interface	Interface type
06AH	22H	CISTPL FUNCE								Function extension tuple	Tuple code
06CH	03H	TPL_LINK								Link length is 3 bytes	Link to next tuple
06EH	02H	Disk function extension tuple type								Single drive	Extension tuple type for disk
070H	0CH	Reserved			D	U	S	V		No V_{PP}, silicon, single drive V = 0: No V_{PP} required S = 1: Silicon U = 1: Unique serial # D = 1: Single drive on card	Basic ATA option parameters byte 1
072H	0FH	R	I	E	N	P3	P2	P1	P0	P0: Sleep mode supported P1: Standby mode supported P2: Idle mode suppported P3: Drive auto control N: Some config excludes 3X7 E: Index bit is emulated I: Twin IOIS16# data reg only R: Reserved	Basic ATA option parameters byte 2
074H	1AH	CISTPL CONF								Configuration tuple	Tuple code
076H	05H	TPL LINK								Link length is 5 bytes	Link to next tuple
078H	01H	RFS		RMS				RAS		RFS: Reserved RMS: TPCC_RMSK size - 1 = 0 RAS: TPCC_RADR size - 1 = 1 1 byte register mask 2 byte config base address	Size of fields byte TPCC_SZ
07AH	03H	TPCC_LAST								Entry with config index of 3 is fainal entry in table	Last entry of config registers
07CH	00H	TPCC RADR (LSB)								Configuration registers are located at 200 H in REG space	Location of config registers
07EH	02H	TPCC RADR (MSB)									
080H	0FH	Reserved				S	P	C	I	I: CCOR, C: CCSR P: PRR, S: SCR	Configuration registers present mask TPCC_RMSK

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
082H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
084H	08H	TPL_LINK								Link length is 8 bytes	Link to next tuple
086H	C0H	I	D	Configuration index						Memory mapped I/O configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
088H	C0H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVD1 and BVD2 not used IF type = 0: Memory interface	Interface description field TPCE_IF
08AH	A1H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 01: Memory space info single 2-byte length IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
08CH	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
08EH	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
090H	08H	Length in 256 bytes pages (LSB)								Length of memory space is 2 kB	Memory space description structures (TPCE MS)
092H	00H	Length in 256 bytes pages (MSB)									
094H	20H	X	R	P	RO	A	T			X = 0: No more misc fields R: Reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
096H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
098H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
09AH	00H	I	D	Configuration index						Memory mapped I/O configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
09CH	01H	M	MS		IR	IO	T	P		M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
09EH	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0A0H	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0A2H	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
0A4H	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0A6H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0A8H	0AH	TPL_LINK								Link length is 10 bytes	Link to next tuple
0AAH	C1H	I	D	Configuration INDEX						Contiguous I/O mapped ATA registers configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
0ACH	41H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
0AEH	99H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0B0H	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0B2H	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
0B4H	64H	R	S	E	IO AddrLine					S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLine: 4 lines decoded	I/O space description field TPCE_IO
0B6H	F0H	S	P	L	M	V	B	I	N	S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 1: Bit mask of IRQs present V = 0: No vender unique IRQ B = 0: No bus error IRQ I = 0: No IO check IRQ N = 0: No NMI	Interrupt request description structure TPCE_IR

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0B8H	FFH	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0	IRQ level to be routed 0 to 15 recommended	Mask extension byte 1 TPCE_IR
0BAH	FFH	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	Recommended routing to any “normal, maskable” IRQ.	Maskextension byte 2 TPCE_IR
0BCH	20H	X	R	P	RO	A	T			X = 0: Nomore misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0BEH	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0C0H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
0C2H	01H	I	D	Configuration index						Contiguous I/O mapped ATA registers configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
0C4H	01H	M	MS		IR	IO	T	P		M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0C6H	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0C8H	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0CAH	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
0CCH	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0CEH	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0D0H	0FH	TPL_LINK								Link length is 15 bytes	Link to next tuple
0D2H	C2H	I	D	Configuration INDEX						ATA primary I/O mapped configuration I = 1: Interface byte follows D = 1: Default entry follows Configuration index = 2	Configuration table index byte TPCE_INDX
0D4H	41H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
0D6H	99H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0D8H	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0DAH	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
0DCH	EAH	R	S	E	IO AddrLine					R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
0DEH	61H	LS		AS		N range				LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 byte N Range = 1: Address range - 1	I/O range format description

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0E0H	F0H									1st I/O base address (LSB)	1st I/O range address
0E2H	01H									1st I/O base address (MSB)	
0E4H	07H									1st I/O length - 1	1st I/O range length
0E6H	F6H									2nd I/O base address (LSB)	2nd I/O range address
0E8H	03H									2nd I/O base address (MSB)	
0EAH	01H									2nd I/O length - 1	2nd I/O range length
0ECH	EEH	S	P	L	M	IRQ level				S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level is IRQ14	Interrupt request description structure TPCE_IR
0EEH	20H	X	R	P	RO	A	T			X = 0: No more misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0F0H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0F2H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
0F4H	02H	I	D	Configuration index						ATA primary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 2	Configuration table index byte TPCE_INDX
0F6H	01H	M	MS		IR	IO	T	P		M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0F8H	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0FAH	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0FCH	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
0FEH	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max average current

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
100H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
102H	0FH	TPL_LINK								Link length is 15 bytes	Link to next tuple
104H	C3H	I	D	Configuration INDEX						ATA secondary I/O mapped configuration I = 1: Interface byte follows D = 1: default entry Configuration index = 3	Configuration table index byte TPCE_INDX
106H	41H	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
108H	99H	M	MS		IR	IO	T	P		M = 1: misc info present MS = 00: No memory space info IR = 1: Onterrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
10AH	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
10CH	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
10EH	EAH	R	S	E	IO AddrLine					R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
110H	61H	LS		AS		N range				LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 byte N Range = 1: Address range - 1	I/O range format description

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
112H	70H									1st I/O base address (LSB)	1st I/O range address
114H	01H									1st I/O base address (MSB)	
116H	07H									1st I/O length - 1	1st I/O range length
118H	76H									2nd I/O base address (LSB)	2nd I/O range address
11AH	03H									2nd I/O base address (MSB)	
11CH	01H									2nd I/O length - 1	2nd I/O range length
11EH	EEH	S	P	L	M	IRQ level				S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level isIRQ14	Interrupt request description structure TPCE_IR
120H	20H	X	R	P	RO	A	T			X = 0: Nomore misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
122H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
124H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
126H	03H	I	D	Configuration index						ATA secondary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 3	Configuration table index byte TPCE_INDX
128H	01H	M	MS		IR	IO	T	P		M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
12AH	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
12CH	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
12EH	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
130H	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max average current
132H	14H	CISTPL_NO_LINK								No link control tuple	Tuple code
134H	00H									Link is 0 bytes	Link to next tuple
136H	FFH	CISTPL_END								End of list tuple	Tuple code

Appendix B Descriptions of Task File Registers

Data Register: This is a 16-bit readable/writable register used in sector-unit data transfer between the host and the card. Word, byte, and odd-byte accesses defined in the PC card standard can all be used on this register, but part of the address is shared with the error register when reading and the feature register when writing.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D0 to D15															

Error Register: This is a read-only register used in the analysis of error contents during card access. This register is valid when the BSY bit is 0 (“Ready”) in the status register and alternate status register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBK	UNC	“0”	IDNF	“0”	ABRT	“0”	AMNF

Bit	Name	Function
7	BBK (Bad BlocK detected)	This bit is set if a bad block is detected.
6	UNC (Data ECC error)	This bit is set if an uncorrectable ECC error is detected.
4	IDNF (I D Not Found)	This bit is set if there is an error in the access target sector or if that sector is not present.
2	ABRT (ABoRTed command)	This bit is set if a command is aborted due to the card status (Not ready, Write fault, etc.), or if an unsupported command is executed.
0	AMNF (Address Mark Not Found)	This bit is set in case of the general error state.

Feature Register: This is a write-only register used when the host sets a specific function for the card.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Feature byte							

Sector Register: The number of sectors for read/write transfer between the host and the card is set in this register by the host. If a value of 00H is set in this register, the sector count is 256. In the case of multiple sector transfers, if the command ends abnormally the number of unprocessed sectors is stored in this register. The initial value of this register is 01H.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sector count byte							

Sector Number Register: The sector number at which sector transfer is to start is set in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sector number byte							

Cylinder Low Register: The lower 8 bits of the cylinder number at which sector transfer is to start are set in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cylinder low byte							

Cylinder High Register: The upper 8 bits of the cylinder number at which sector transfer is to start are set in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cylinder high byte							

Drive Head Register: The card drive number and the head number at which sector transfer is to start are set in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	LBA	1	DRV	Head number			

Bit	Name	Function
7	1	Set this bit to 1.
6	LBA	Used to switch between operation in cylinder/head/sector (CHS) mode and logical block address (LBA) mode. CHS mode is selected when LBA = 0, and CHS mode when LBA = 1. In LBA mode, the logical block addresses correspond to the following register bits. LBA07-LBA00: Sector Number Register D7–D0. LBA15-LBA08: Cylinder Low Register D7–D0. LBA23-LBA16: Cylinder High Register D7–D0. LBA27-LBA24: Drive/Head Register bits HS3–HS0.
5	1	Set this bit to 1.
4	DRV (DRiVe select)	This bit is used for selection in a master/slave configuration. When the DRV# bit in the socket and copy register and this bit match, the card can be accessed.
3 to 0	Head number	These bits specify the head number at which sector transfer is to start. Bit 3 is the MSB.

Status Register: This is a read-only register that notifies the host of the card status when a command is executed. If the card is configured in I/O card mode (INDEX = 1, 2, 3) and level interrupt mode, the $\overline{\text{IREQ}}$ signal pin is negated by reading this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Bit	Name	Function
7	BSY (BuSY)	This bit is set to 1 when internal card processing is being executed. When this bit is 1, the other bits in this register are invalid.
6	DRDY (Drive ReaDY)	This bit is set to 1 when internal card processing ends and access from the host can be accepted.
5	DWF (Drive Write Fault)	This bit is set to 1 if a write fault occurs in the card.
4	DSC (Drive Seek Complete)	This bit is set to 1 when a drive seek is completed.
3	DRQ (Data ReQuest)	This bit is set to 1 when preparations are completed for data transfer between the host and the card.
2	CORR (CORRected data)	This bit is set to 1 when a correctable error has occurred in internal card processing and the error has been corrected.
1	IDX (InDeX)	This bit is always cleared to 0.
0	ERR (ERRor)	This bit is set to 1 if an error occurs during processing of the input command. Supplementary error information is set in the error register. This bit is cleared by input of the next command.

Alternate Status Register: Physically, this register has the same bit assignments as the status register. The difference is that the $\overline{\text{IREQ}}$ pin is not negated when this register is read.

Command Register: This is a write-only register used for command execution. A command is executed by writing that command to this register after parameter setting is completed (see table below).

		Used Parameter						
Command	**Command Code**	**FR**	**SC**	**SN**	**CY**	**DR**	**HD**	**LBA**
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
SC: Sector Count register
SN: Sector Number register

CY: Cylinder register
DR: DRV bit of Drive Head register
HD: Head Number of Drive Head register
LBA: Logical Block Address Mode Supported
Y: Valid parameter for this command
N: Invalid parameter for this command

Device Control Register: This is a write-only register that performs internal reset signal control and ATA software reset issuance.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	×	×	×	1	SRST	nIEN	0

Bit	Name	Function
7 to 4	×	don't care
3	1	Set this bit to 1.
2	SRST (Software ReSeT)	When this bit is set to 1, an ATA software reset is executed. Unlike a hardware reset, this reset does not initialize the configuration registers. The reset state is not cleared until this bit is cleared to 0.
1	nIEN (Interrupt ENable)	This bit controls enabling of the $\overline{\text{IREQ}}$ signal. $\overline{\text{IREQ}}$ is enabled when this bit is cleared to 0, and disabled when it is set to 1.
0	0	Clear this bit to 0.

Drive Address Register: This is a read-only register used to provide compatibility with the AT disk interface. As bit 7 of this register may cause a collision, it is recommended that this register not be mapped in I/O space.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

Bit	Name	Function
7	×	Undefined
6	nWTG (WriTing Gate)	Undefined
5 to 2	nHS3–0 (Head Select 3–0)	These 4 bits are the NOT of the Head Number bits in the drive/head register.
1	nDS1 (Idrive Select 1)	Undefined
0	nDS0 (Idrive Select 0)	Undefined

Appendix C Glossary

No.	Item	Description
1	PCMCIA	Personal Computer Memory Card International Association: an organization for the standardization of PC card specifications.
	PCMCIA*.* / JEIDA *.*	Standard name and revision number. Standardization of SRAM and other memory cards was begun in 1985, initially by JEIDA. In 1989, PCMCIA was established with the participation of IBM, Apple, etc. Standardization efforts have progressed jointly since then. The current standard is PCMCIA2.1/JEIDA4.2, covering the use of fax/modem cards, etc., as well as memory cards.
2	JEIDA	Japan Electric Industrial Development Association. Promotes PC card standardization jointly with PCMCIA.
3	WindowsCE	An operating system for handheld PCs, developed by Microsoft. The interface uses a similar GUI to that of Windows95.
4	CompactFlash™	A new flash card standard proposed by SanDisk Inc. of the USA. Physically, 1/3 the area of a PC card, with a 50-pin two-piece connector, but electrically compliant with existing projects, including PC-ATA specifications and True-IDE specifications, offering excellent compatibility.
5	PC-ATA	PC Card AT Attachment. Standard for connecting a PC-ATA specification memory card to a PC card slot. Can be thought of as bringing the ATA standard for HDDs into the field of PC cards. A PC-ATA card is a PC card that conforms to the PCMCIA PC-ATA standard.
6	True-IDE	Standard for handling a flash card as an HDD. Standard for flash cards operated as HDDs immediately after start-up. Totally unrelated to PC-ATA specifications and the PC card standard.
7	Chip set	Generally refers to functional LSIs for implementing certain functions by being connected to the CPU, bus, etc. In this manual, “chip set” refers to products called PC card controllers.
8	Memory card	A type of PC card, such as an SRAM card or flash card, containing memory and used for storage, .
9	I/O card	A type of PC card, such as a SCSI card or fax/modem card, for connection to another device or computer.
10	IDE specifications	IDE: Integrated Device Electronics, Intelligent Device Electronics. HDD interface standard developed by US companies Western Digital and Compaq in 1986. Designed to allow direct connection to the PC-AT bus (currently generally called the ISA bus) initially used by IBM.
11	ISA bus (PC-AT bus)	Industrial Standard Architecture bus. Bus used in the days of the IBM-PC, initially called the PC-AT bus. Provides direct connection to an Intel X86 CPU. Became an industry standard after IBM stopped designing machines using this bus standard.

No.	Item	Description
12	IBM-PC	Earliest personal computer produced by IBM, from which all today's personal computers could be said to derive. The undercurrents of today's technologies, including Intel CPUs and Microsoft operating systems, began here.
13	ATA specifications	HDD standard created by ANSI, basically synonymous with IDE specifications. The original IDE specifications were established as ATA1, and currently a general enhanced IDE has been standardized as ATA3. Note that these specifications are different from the PC-ATA specifications referred to throughout this manual.
14	Enhanced IDE specifications	Currently the most widely used HDD standard. The former IDE standard, which provided only for connection of up to two HDDs and a capacity of up to 504 MB, has been enhanced to support 4 HDDs and almost 4 GB. Connection of CD-ROM is also supported. This requires an ATAPI (ATA Packet Interface) specification CD-ROM.
15	CFA	CompactFlash™ Association: an organization for the promotion of CompactFlash™. Currently (June 13, 1997) includes 72 vendors and user companies working to promote the use of this medium.
16	ANSI	American National Standards Institute
17	PC card	Business-card-sized IC card inserted in a PC card slot in a personal computer, etc. Fax/modem cards, LAN cards, etc., are available as well as flash memory cards. These have been standardized by PCMCIA/JEIDA.
18	Microsoft	Leader of the personal computer OS industry, headed by Bill Gates. World's largest software company, holding an overwhelming share of the PC operating system and application software markets.
19	Intel	World's largest semiconductor manufacturer. Controls 90% of the market for personal computer CPUs. Now attempting to make inroads into other PC-related fields.
20	Western Digital	HDD manufacturer
21	SanDisk	Dedicated flash card manufacturer, originator of the CF standard. Currently holds the largest share of the world flash card market.

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