
HB56A132 Series

1,048,576-word $\times$ 32-Bit High Density Dynamic RAM Module

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ADE-203-
Rev. 0.0
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Description

The HB56A132 is a 1 M $\times$ 32 dynamic RAM module, mounted 8 pieces of (4-Mbit) DRAM (HM514400CS/CLS) sealed in SOJ package. An outline of the HB56A132 is 72-pin single in-line package. Therefore, the HB56A132 makes high density mounting possible without surface mount technology. The HB56A132 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

Features

- 72-pin single in-line package
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 4.62W/4.20W/3.78W (max)
 - Standby mode: 84 mW (max)
4.2 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycle: 16 ms
128 ms (L-version)
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

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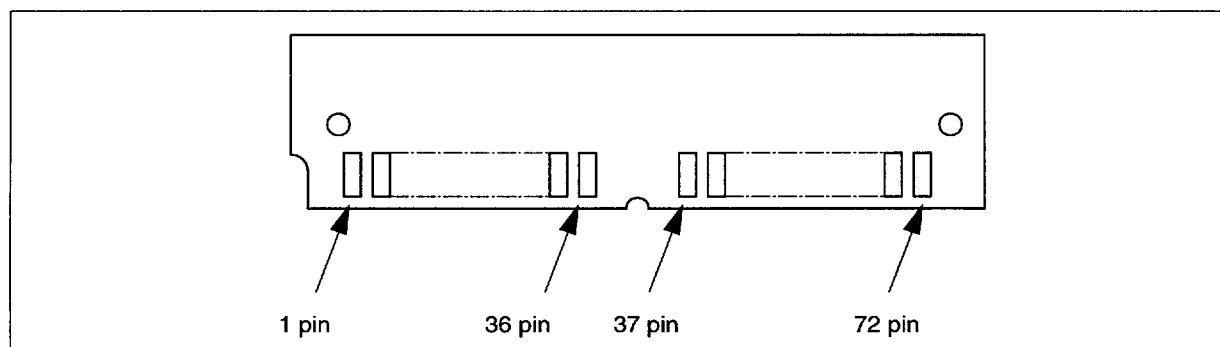
Ordering Information

Type No.	Access time	Package	Contact pad
HB56A132BW-6C	60 ns	72-pin SIP socket type	gold
HB56A132BW-7C	70 ns		
HB56A132BW-8C	80 ns		
HB56A132BW-6CL	60 ns		
HB56A132BW-7CL	70 ns		
HB56A132BW-8CL	80 ns		
HB56A132BU-6C	60 ns		
HB56A132BU-7C	70 ns		
HB56A132BU-8C	80 ns		
HB56A132BU-6CL	60 ns		
HB56A132BU-7CL	70 ns		
HB56A132BU-8CL	80 ns		
HB56A132SBW-6C	60 ns	72-pin SIP socket type	solder
HB56A132SBW-7C	70 ns		
HB56A132SBW-8C	80 ns		
HB56A132SBW-6CL	60 ns		
HB56A132SBW-7CL	70 ns		
HB56A132SBW-8CL	80 ns		

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Pin Arrangement


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	19	NC	37	NC	55	DC11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	CAS0	58	DQ28
5	DQ17	23	DQ21	41	CAS2	59	V _{CC}
6	DQ2	24	DQ6	42	CAS3	60	DQ29
7	DQ18	25	DQ22	43	CAS1	61	DQ13
8	DQ3	26	DQ7	44	RAS0	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	WE	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	RAS2	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

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Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
DQ0 – DQ31	Data-in/data-out
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column address strobe
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row address strobe
$\overline{\text{WE}}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

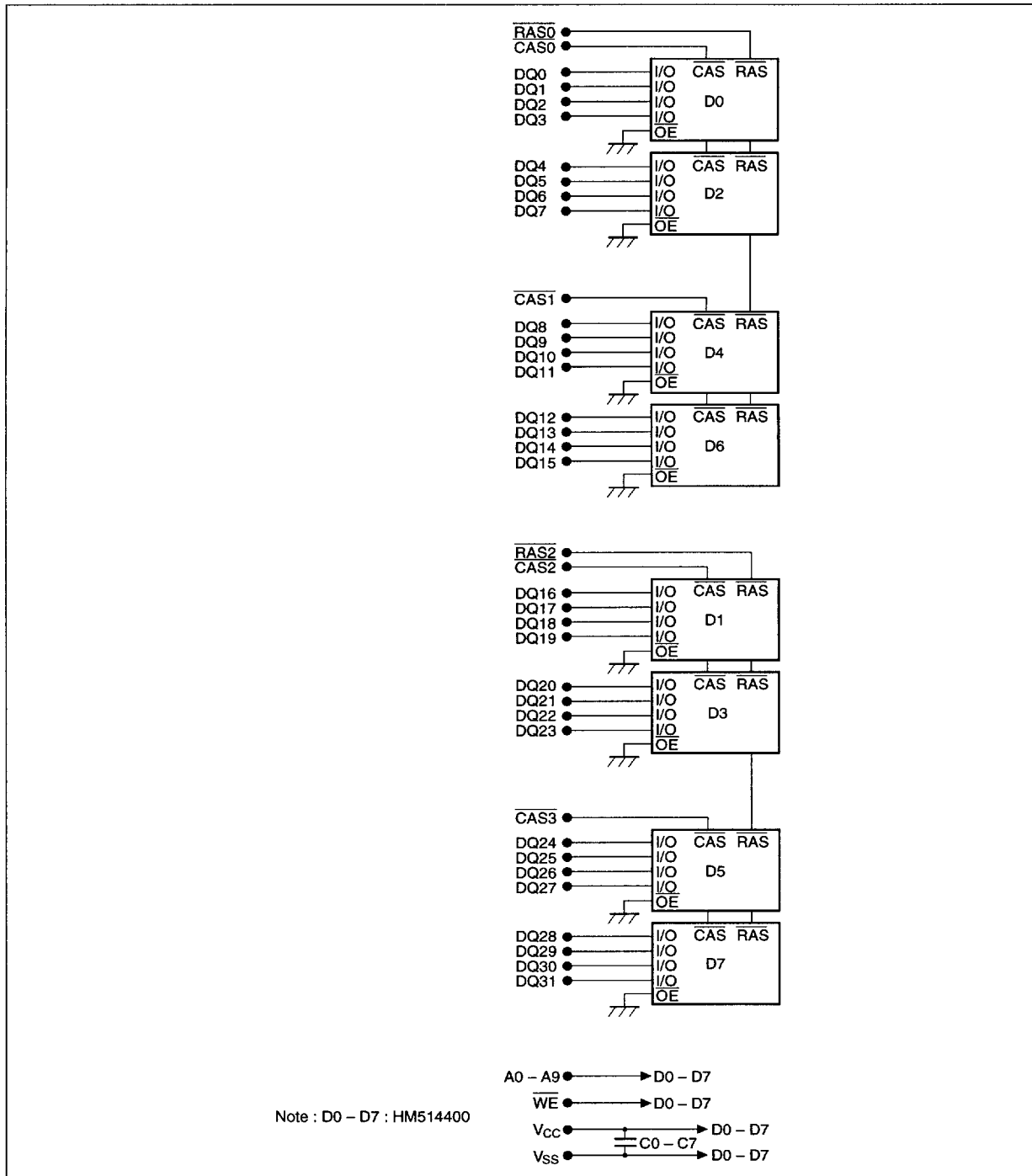
Presence Detect Pin Pinout

Pin No.	Pin name	HB56A132		
		60 ns	70 ns	80 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	8	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

		HB56A132								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I _{CC1}	—	880	—	800	—	720	ma	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	16	—	16	—	16	mA	TTL interface, RAS, CAS = V _{IH} , Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface, RAS, CAS ≥ V _{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	0.8	—	0.8	—	0.8	mA	CMOS interface, RAS, CAS = V _{IH} , WE, Address., Din = V _{IH} or V _{IL} , Dout = High-Z	4
RAS-only refresh current	I _{CC3}	—	880	—	800	—	720	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	40	—	40	—	40	mA	RAS = V _{IH} , CAS = V _{IL} , Dout = enable	1
CAS before RAS refresh current	I _{CC6}	—	880	—	800	—	720	mA	t _{RC} = min	
Page mode current	I _{CC7}	—	880	—	800	—	720	mA	t _{PC} = min	1, 3
Battery backup operation current (CBR refresh) (L-version)	I _{CC10}	—	1.6	—	1.6	—	1.6	mA	t _{RC} = 125 μs, t _{RAS} ≤ 1 μs, WE = V _{IH} , CAS = V _{IL} , Address, Din = V _{IH} or V _{IL} , Dout = High-Z	4
Input leakage current	I _{LI}	–10	10	–10	10	–10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I _{LO}	–10	10	–10	10	–10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = –5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$, $0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$

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Capacitance ($T_a=25^{\circ}\text{C}$, $V_{CC}=5\text{ V}\pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{11}	—	68	pF	1
Input capacitance ($\overline{WE}$)	C_{12}	—	76	pF	1
Input capacitance ($\overline{RAS}$)	C_{13}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C_{14}	—	29	pF	1
I/O capacitance (DQ0 - DQ31)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS}=V_{IH}$ to disable Dout.

AC Characteristics

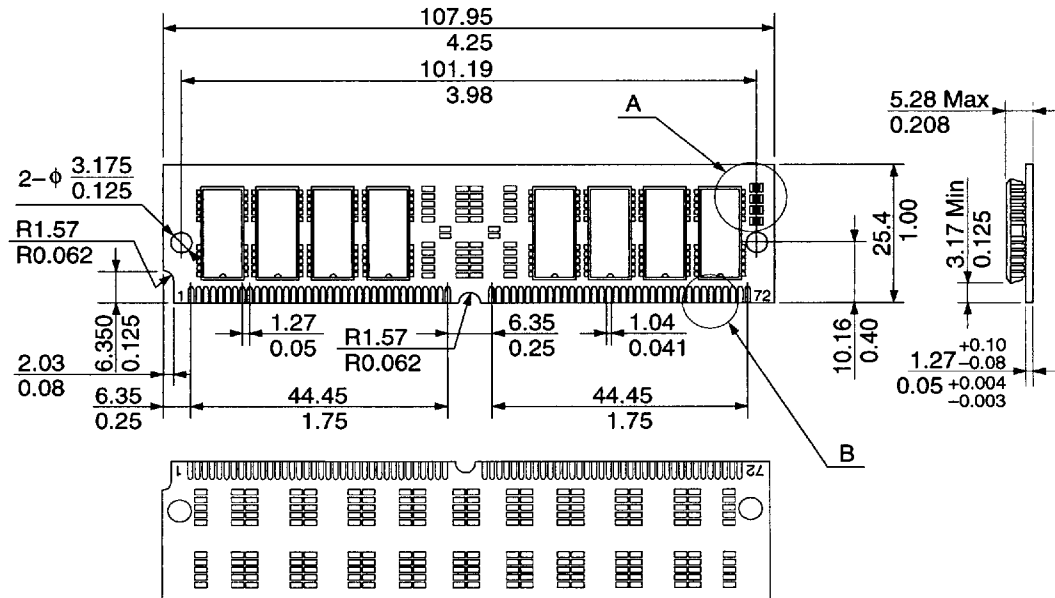
- Refer to the HM514400C Series data sheet.
- The HB56A132 writes data only in early write cycle ($t_{wCS} \geq t_{wCS}(\text{min})$).
Delayed write cycle is not available ($\overline{OE}$ pin is fixed to V_{SS}).

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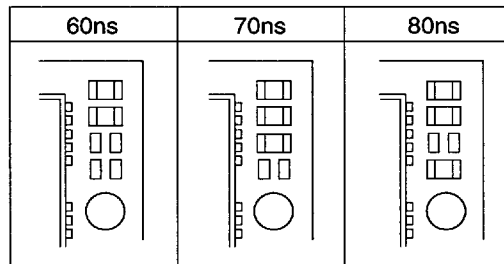
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Physical Outline

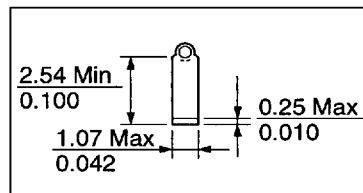
Unit: mm/inch



Detail A



Detail B



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