HB56A49 Series

4,194,304-Word x 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A49 is a 4M x 9 dynamic RAM module, mounted 9 pieces of 4 Mbit DRAM (HM514100AS, HM514100JP) sealed in an SOJ package. An outline of the HB56A49 is the 30-pin single in-line package. Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs, and also provides separate I/O parity bit for parity check. Decoupling capacitors are mounted beneath each SOJ.

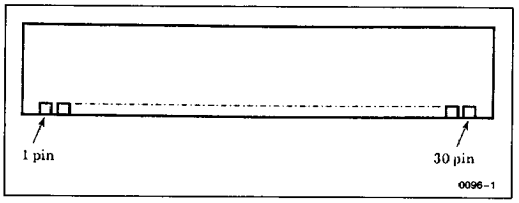
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 5445 mW/4059 mW/4455 mW/3960 mW (max)
  - Standby Mode ..... 99 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

■ PIN OUT



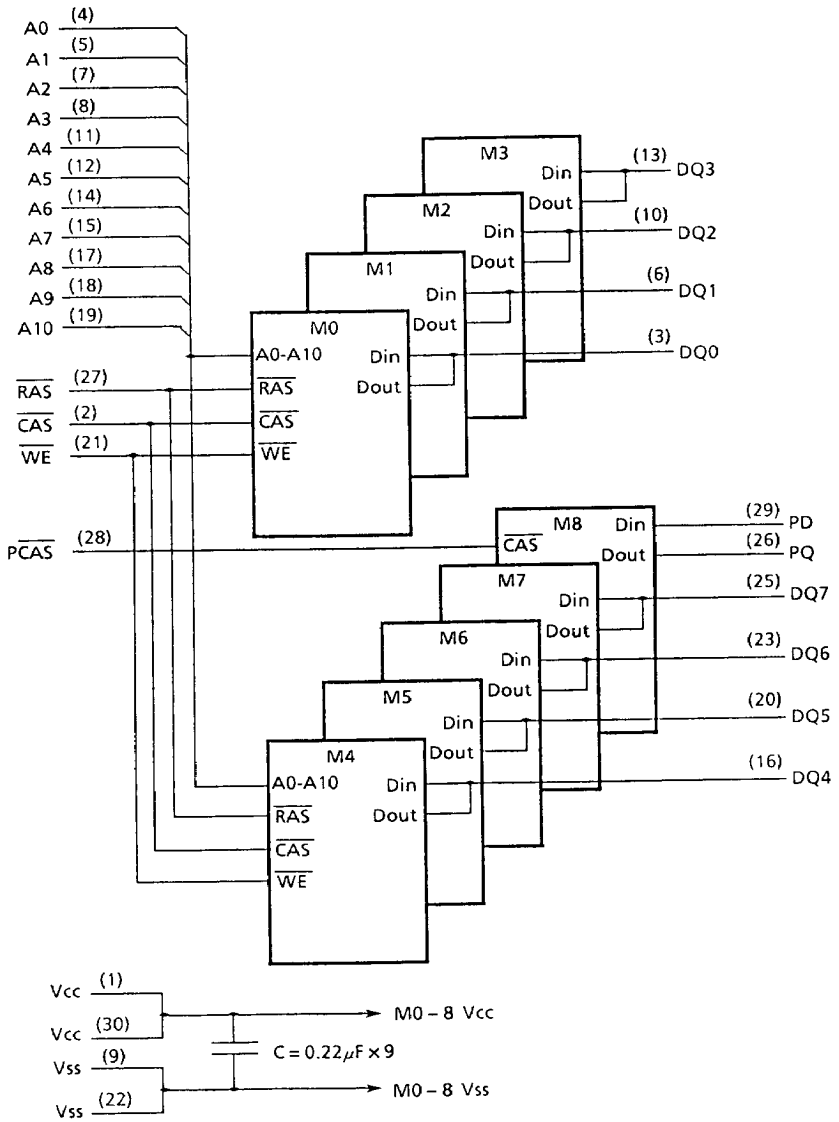
Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	A_{10}
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ ORDERING INFORMATION

Access Time	Package					
	30-pin [1] SIP Socket Type	30-pin [1] SIP Socket Type	30-pin SIP Lead Type	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Low Profile Lead Type
	0.945 Inch Height	0.805 Inch Height	0.989 Inch Height	0.810 Inch Height	0.591 Inch Height	0.500 Inch Height
60 ns	—	HB56A49BR/GBR-6A	—	HB56A49AR-6A	—	HB56A49ATR-6A
70 ns	—	HB56A49BR/GBR-7A	—	HB56A49AR-7A	—	HB56A49ATR-7A
80 ns	HB56A49B/GB-8	HB56A49BR/GBR-8A	HB56A49A-8	HB56A49AR-8A	HB56A49AT-8	HB56A49ATR-8A
100 ns	HB56A49B/GB-10	HB56A49BR/GBR-10A	HB56A49A-10	HB56A49AR-10A	HB56A49AT-10	HB56A49ATR-10A

Note: 1. Following the specification of the contact pad.
HB56A49B-XX, HB56A49BR-XX: solder
HB56A49GB-XX, HB56A49GBR-XX: gold

■ BLOCK DIAGRAM

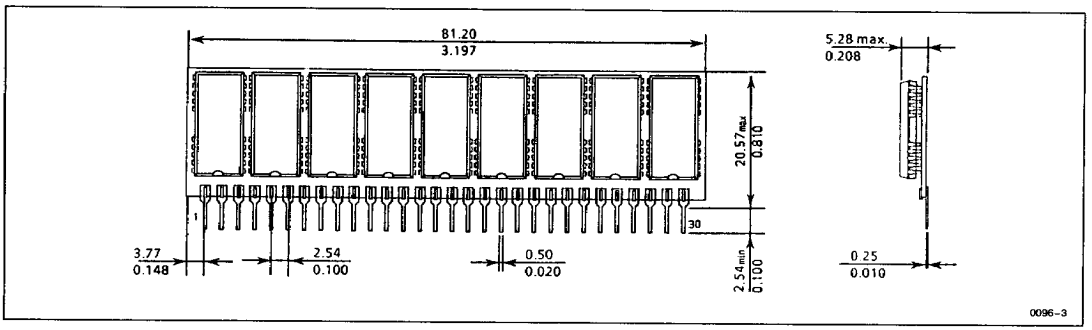


Note: M0–M8[HB56A49XX-XXA]: HM514100AS
M0–M8[HB56A49XX-8/10]: HM514100JP

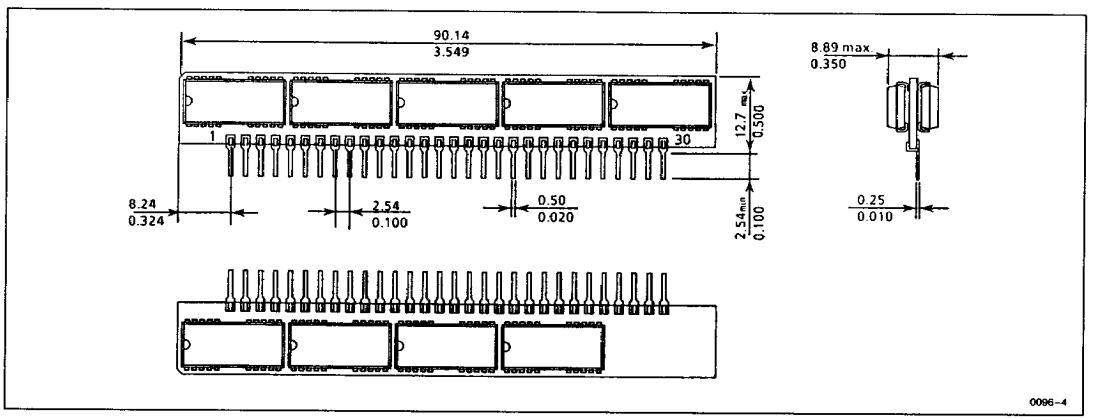
■ PHYSICAL OUTLINE

Unit: mm / inch

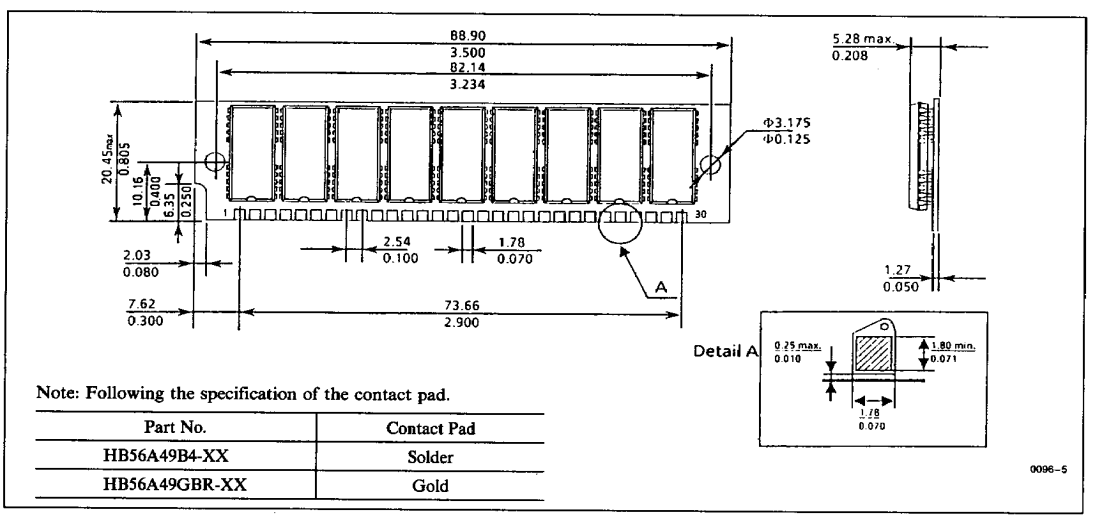
• HB56A49AR Series



• HB56A49ATR Series



• HB56A49BR/GBR Series

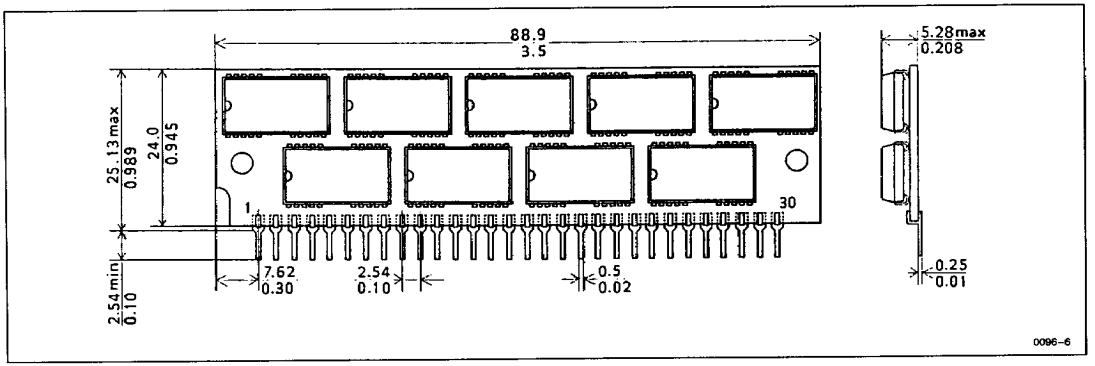


Note: Following the specification of the contact pad.

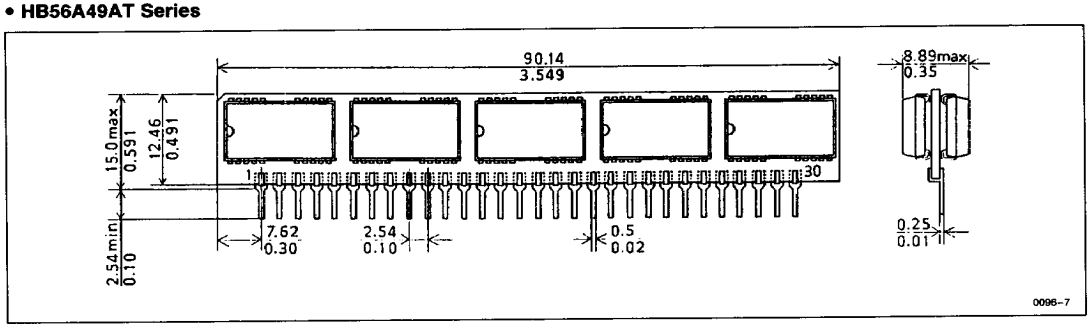
Part No.	Contact Pad
HB56A49B4-XX	Solder
HB56A49GBR-XX	Gold

Unit: mm / inch

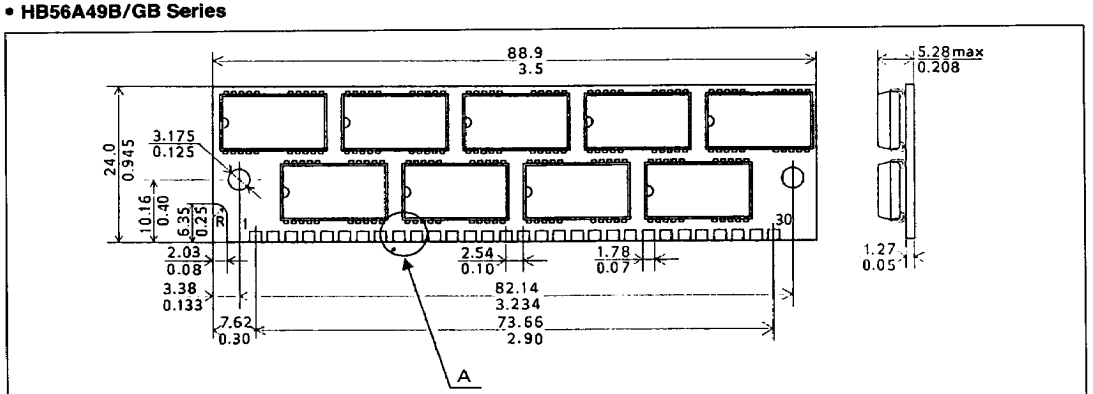
• **HB56A49A Series**



• **HB56A49AT Series**

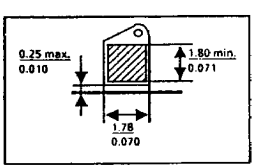


• **HB56A49B/GB Series**



Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A49B-XX	Solder
HB56A49GB-XX	Gold



Detail A

0096-9

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	9	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 0.5	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR								Unit	Test Condition	Note
		-6A		-7A		-8/-8A		-10/-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	990	—	900	—	810	—	720	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	18	—	18	—	18	—	18	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	9	—	9	—	9	—	9	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	990	—	900	—	810	—	720	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	45	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	990	—	900	—	810	—	720	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	990	—	900	—	810	—	720	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	HB56A49				Unit	Note
		BR/GBR/AR/ATR		A/AT/B/GB			
		Typ	Max	Typ	Max		
Input Capacitance (Address)	C_{I1}	—	60	—	70	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	—	88	pF	1
Input Capacitance ($\overline{PCAS}$)	C_{I3}	—	12	—	20	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	-	30	pF	1, 2
Input Capacitance (PD)	C_{I4}	—	10	—	20	pF	1
Output Capacitance (PQ)	C_O	—	12	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 15]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Ramdon Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	50	20	60	25	75	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	35	15	40	20	55	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	17

Read Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	—	25	—	25	ns	3, 4, 14
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	

Read Cycle (continued)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	15	0	20	0	20	0	25	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	—	50	—	50	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	50	—	50	—	ns	

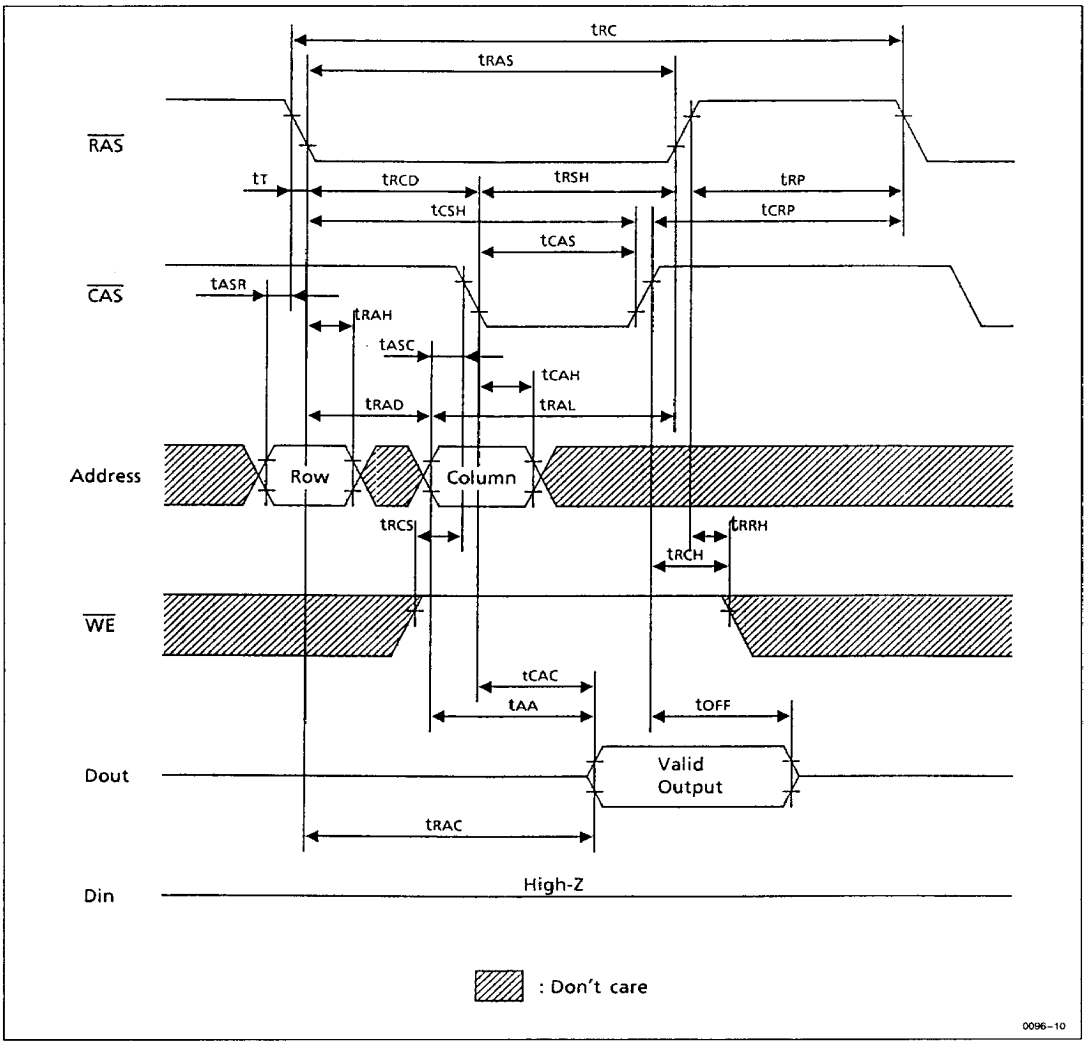
Test Mode Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	20	—	20	—	ns	

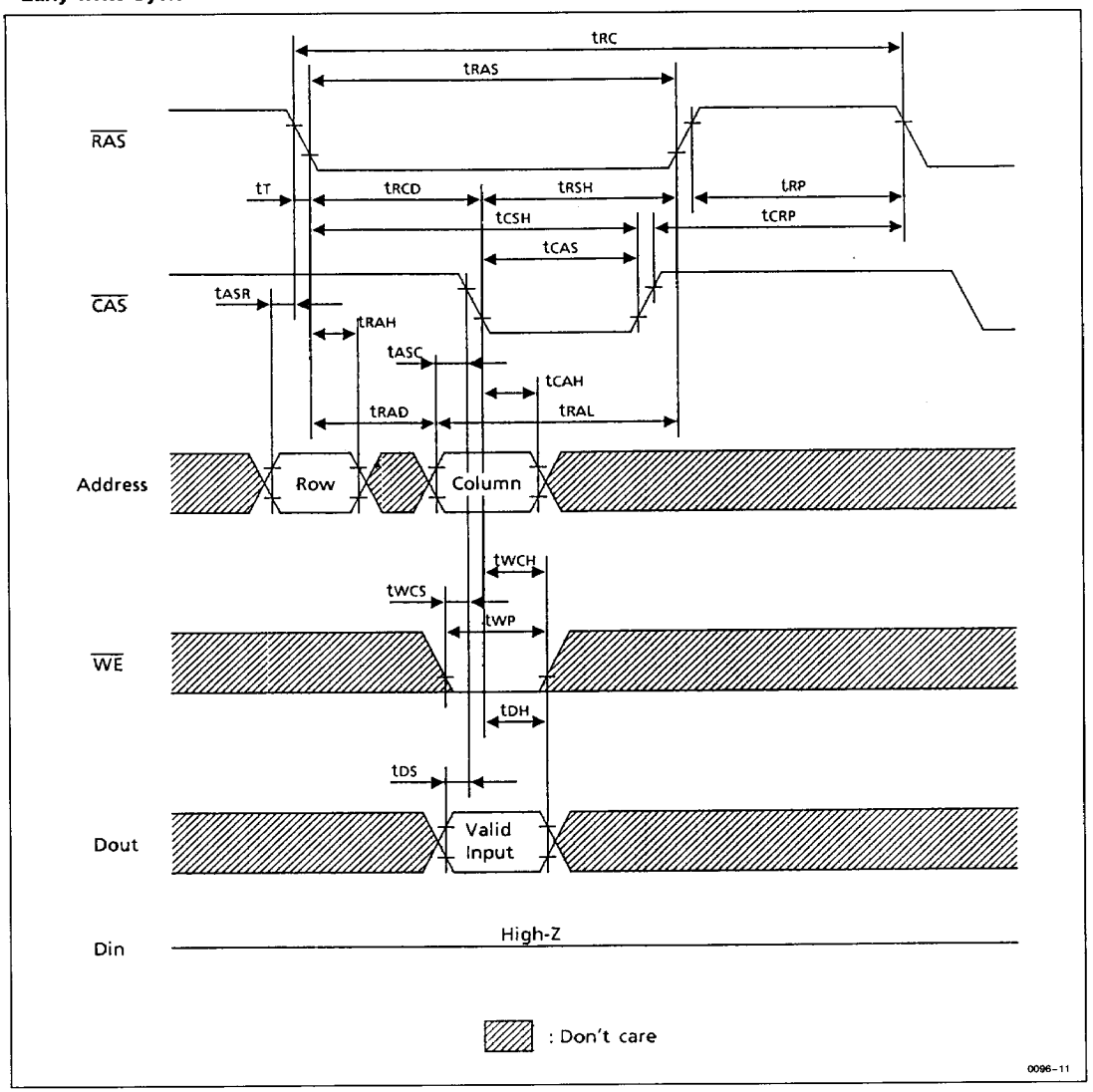
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as RAS only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits . . . RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORM

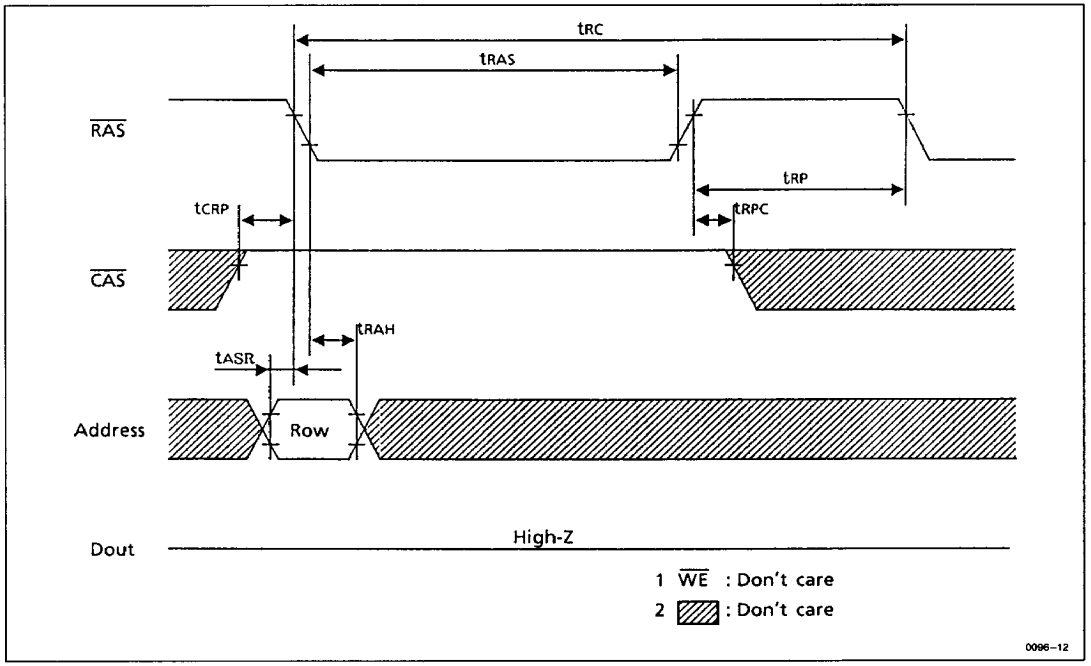
• Read Cycle



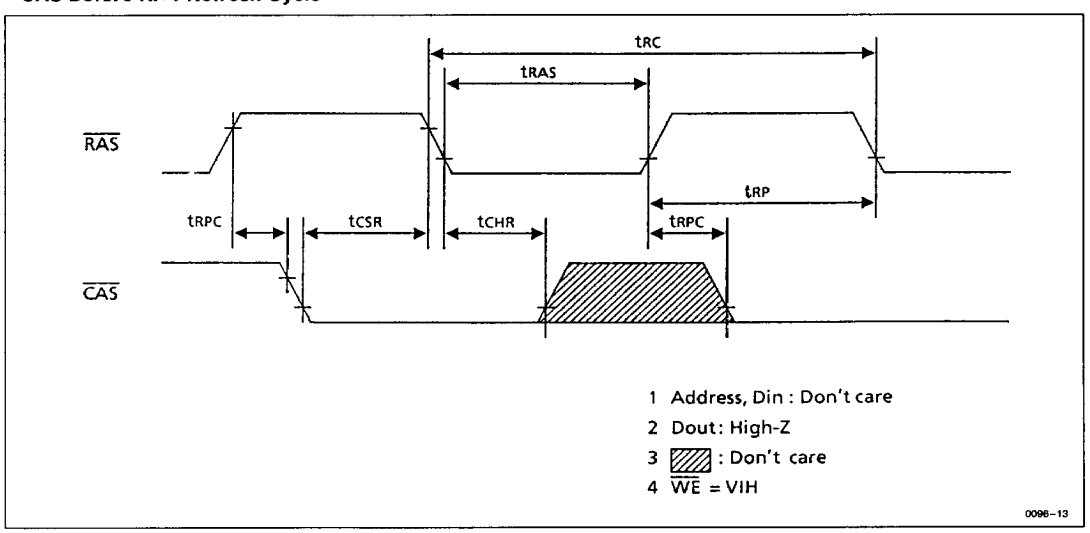
• **Early Write Cycle**



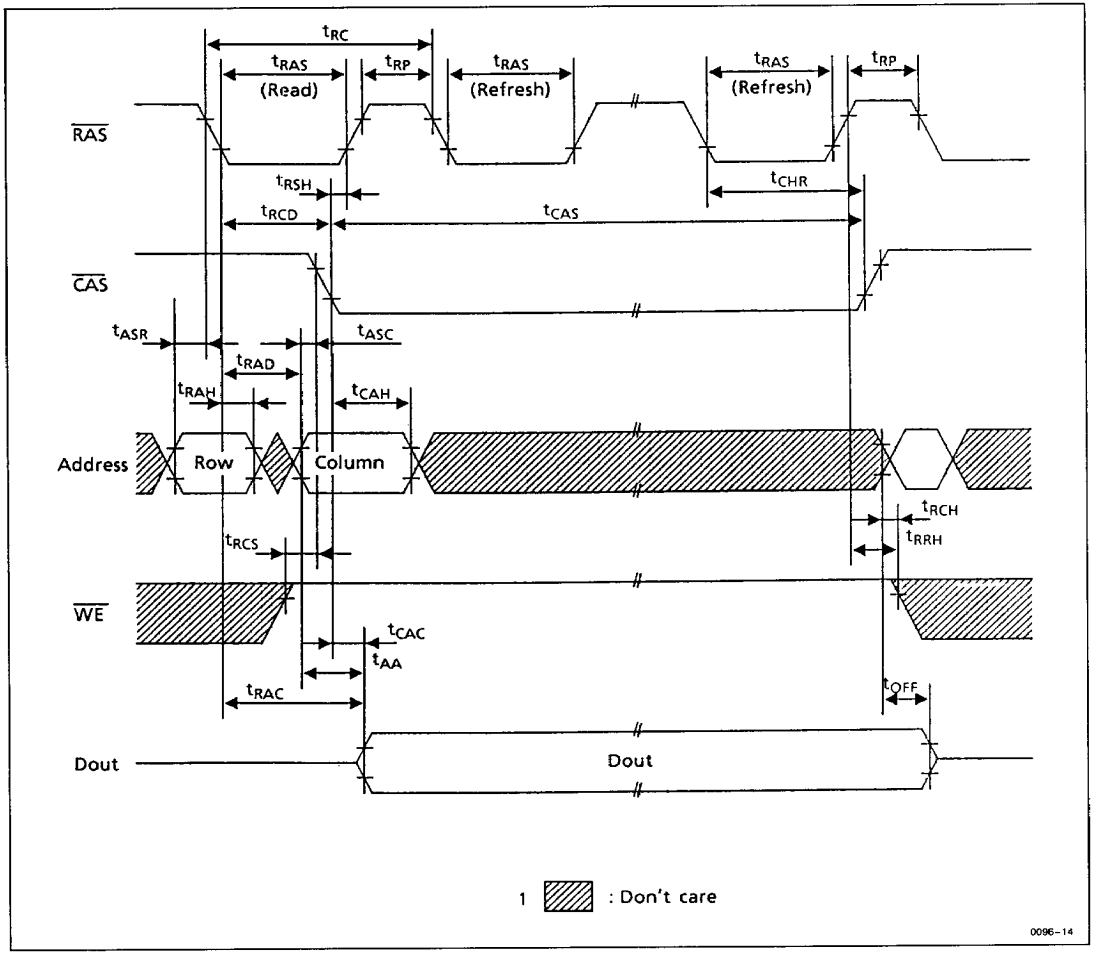
• $\overline{RAS}$ Only Refresh Cycle



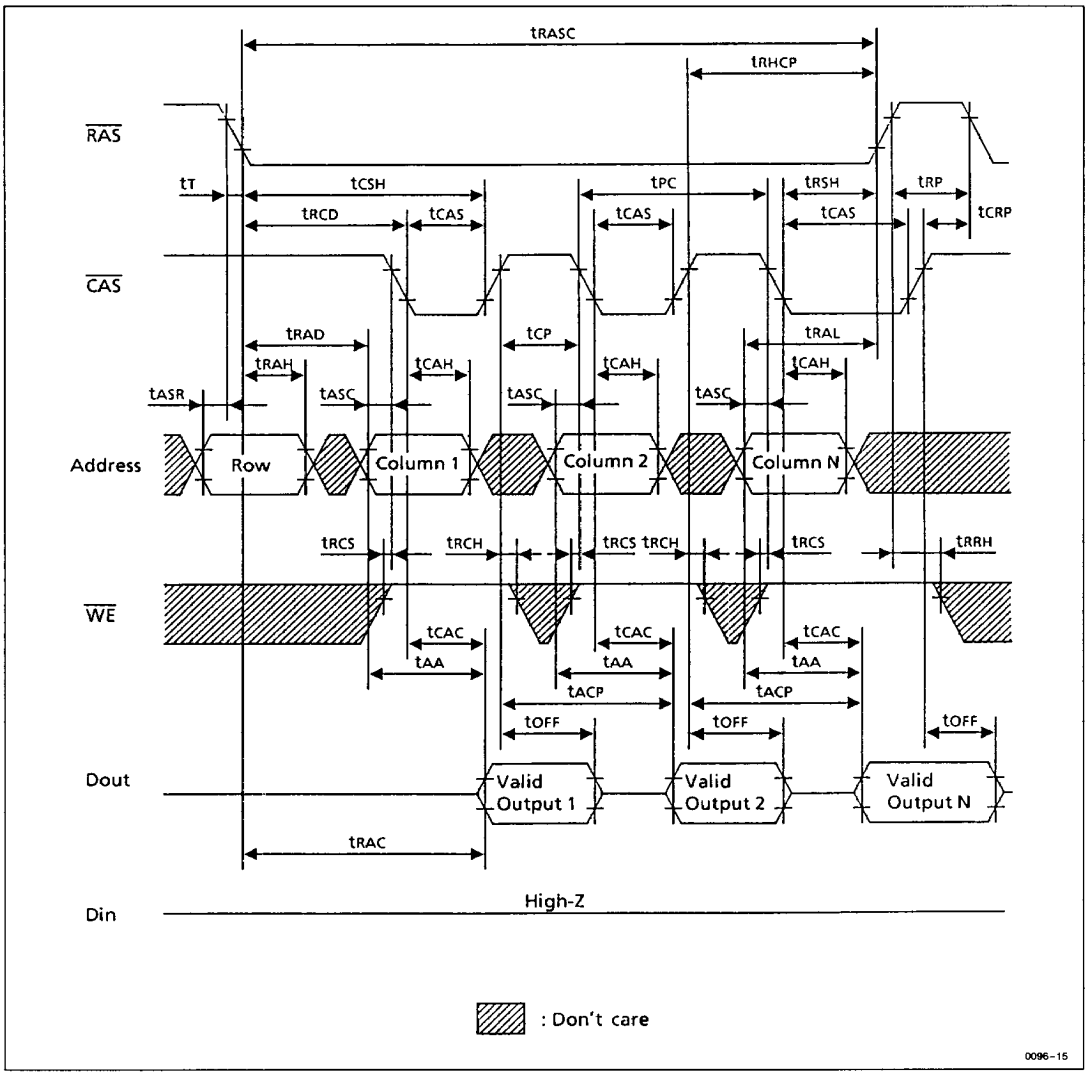
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



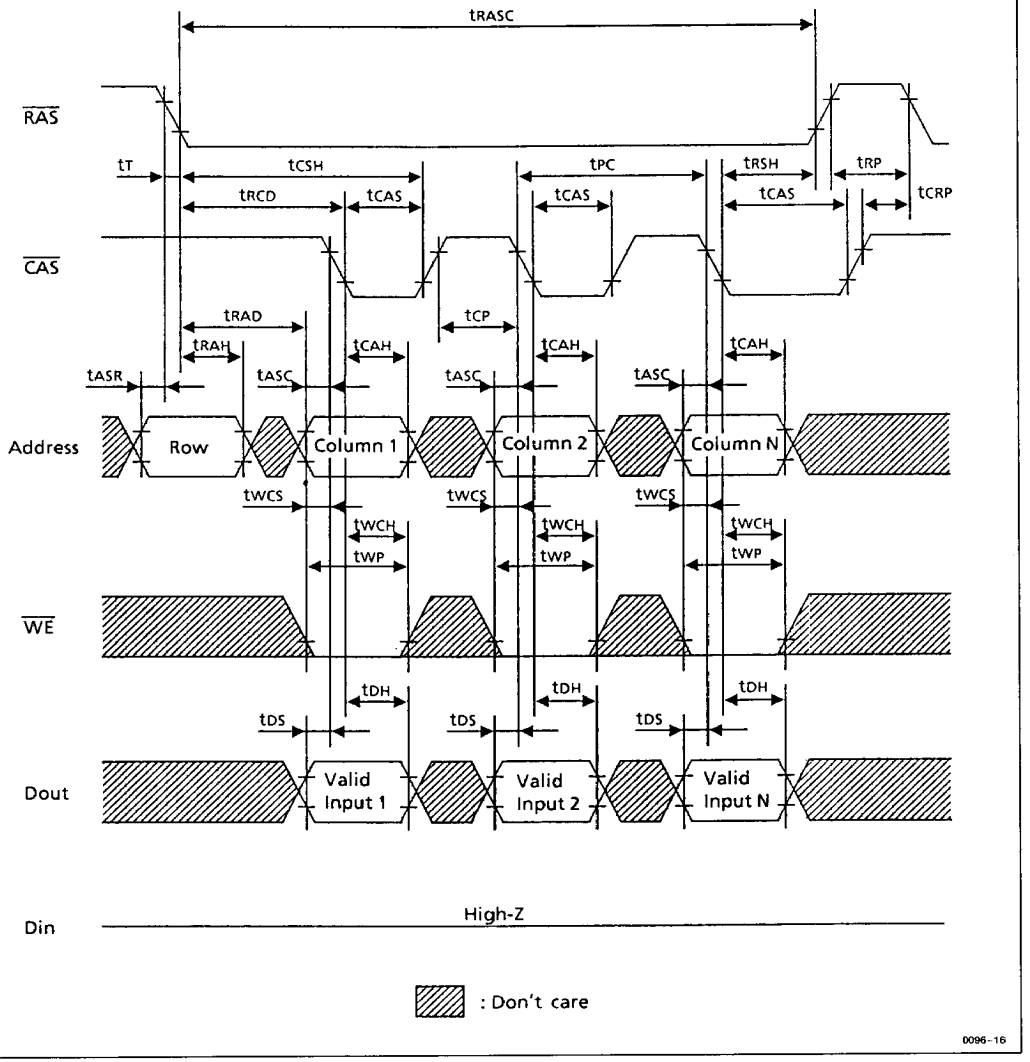
• **Hidden Refresh Cycle**



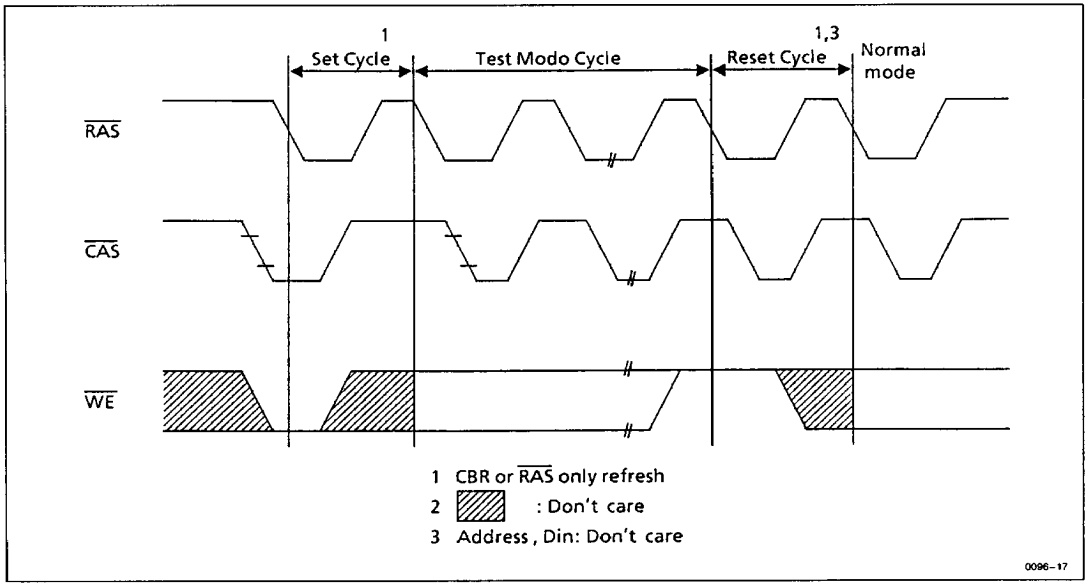
• **Fast Page Mode Read Cycle**



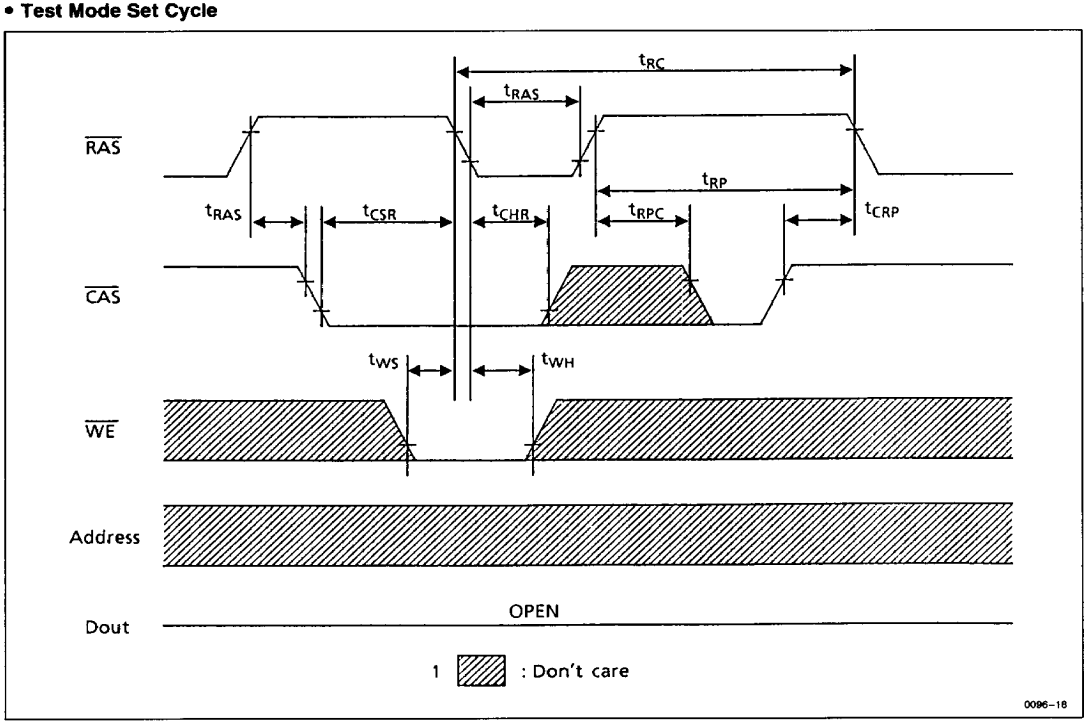
• **Fast Page Mode Early Write Cycle**



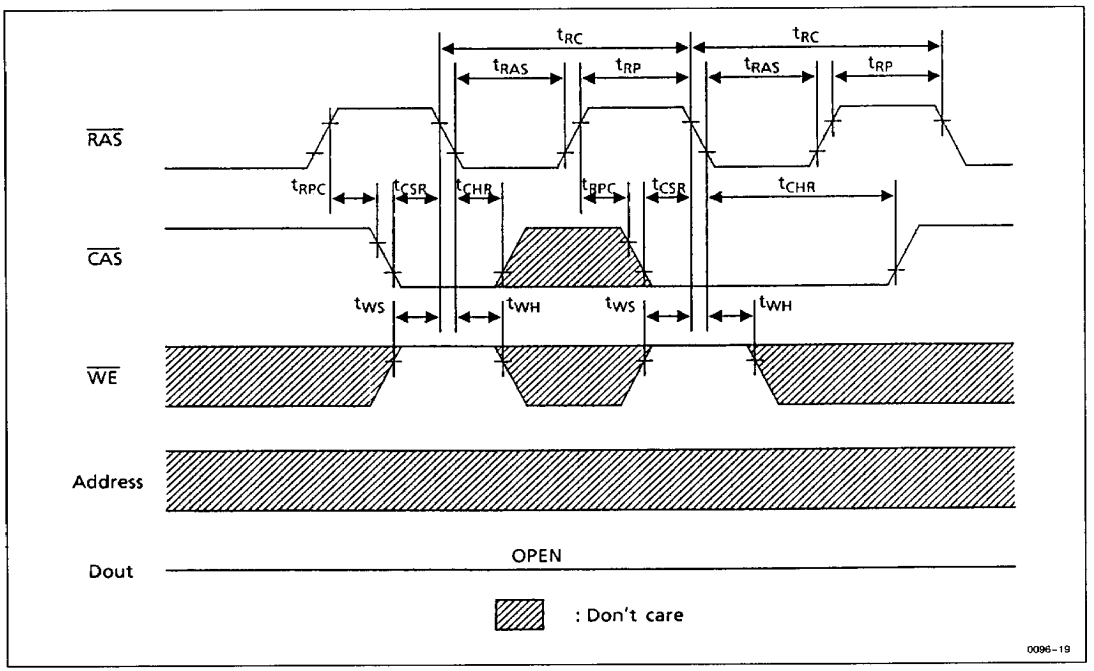
• **TEST MODE CYCLE**



• **Test Mode Set Cycle**



• **Test Mode Reset Cycle**
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{RAS}$ Only Refresh Cycle