

HB56C18 Series

1,048,576-Word x 8-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56C18 is a 1M x 8 static column mode dynamic RAM module, mounted eight 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C18 is 30-pin single in-line package having Lead types (HB56C18A, HB56C18AT), socket type (HB56C18B). Therefore, the HB56C18 makes high density mounting possible without surface mount technology. The HB56C18 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

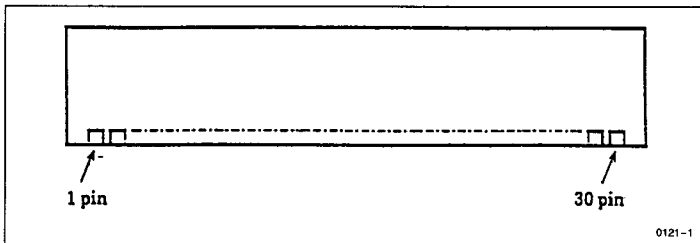
FEATURES

- 30-pin Single In-line Package
 - Lead Pitch2.54mm
- Single 5V ($\pm 10\%$) Supply
- High Speed
 - Access Time80 ns/100 ns/120 ns (max)
- Low Power Dissipation
 - Active Mode3080 mW/2640 mW/2200 mW (max)
 - Standby Mode88 mW (max)
- Static Column Mode Capability
- 512 Refresh Cycle(8 ms)
- 2 Variations of Refresh
 - RAS Only Refresh
 - CAS Before RAS Refresh
- TTL Compatible

ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Socket Type
80 ns	HB56C18A-8A	HB56C18AT-8A	HB56C18B-8A
100 ns	HB56C18A-10A	HB56C18AT-10A	HB56C18B-10A
120 ns	HB56C18A-12A	HB56C18AT-12A	HB56C18B-12A

PIN OUT



PIN DESCRIPTION

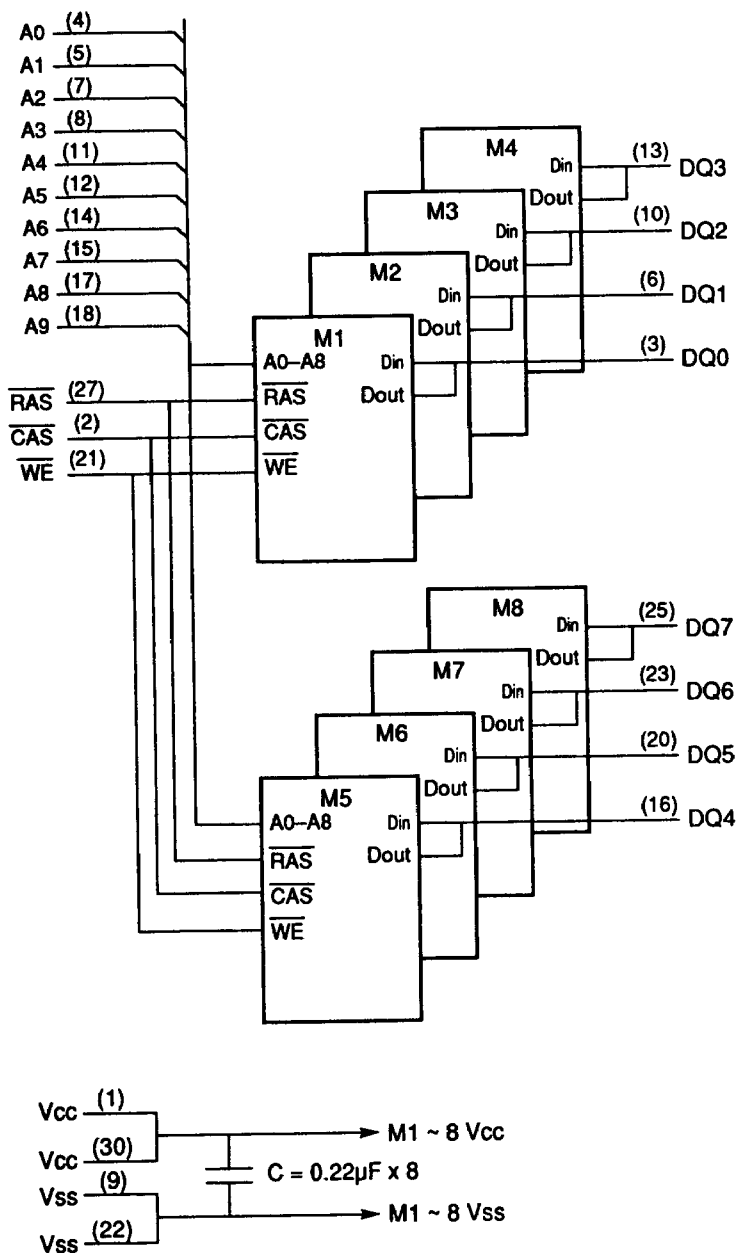
Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	16	DQ ₄
2	$\overline{\text{CAS}}$	17	A ₈
3	DQ ₀	18	A ₉
4	A ₀	19	NC
5	A ₁	20	DQ ₅
6	DQ ₁	21	$\overline{\text{WE}}$
7	A ₂	22	V _{SS}
8	A ₃	23	DQ ₆
9	V _{SS}	24	NC
10	DQ ₂	25	DQ ₇
11	A ₄	26	NC
12	A ₅	27	$\overline{\text{RAS}}$
13	DQ ₃	28	NC
14	A ₆	29	NC
15	A ₇	30	V _{CC}

PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₉	Address Input
A ₀ -A ₈	Refresh Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CS}}$	Chip Select
$\overline{\text{WE}}$	Read/Write Enable
DQ ₀ -DQ ₇	Data-in/Data-out
V _{CC}	Power Supply (+ 5V)
V _{SS}	Ground
NC	Non-Connection



■ BLOCK DIAGRAM



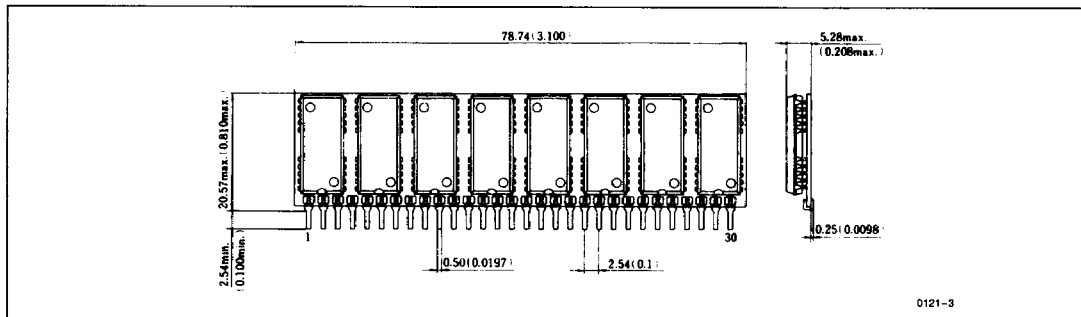
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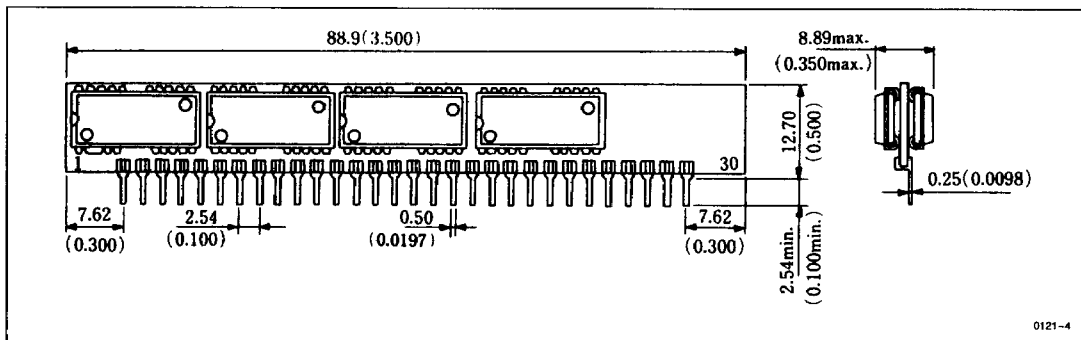
■ PHYSICAL OUTLINE

Unit: $\frac{\text{mm}}{\text{(inch)}}$

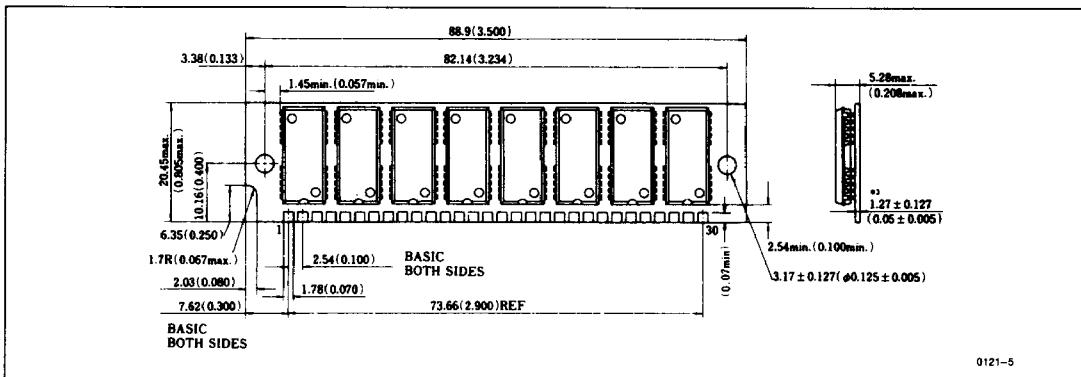
• HB56C18A Series



• HB56C18AT Series



• HB56C18B Series



Note: 1. The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS} .

• DC Electrical Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	HB56C18A/AT/B						Unit	Test Conditions	Note
		-8A		-10A		-12A				
		Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	560	—	480	—	400	mA	t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	16	—	16	—	16	mA	TTL Interface R _{AS} , C _{AS} = V _{IH} , D _{out} = High-Z	
		—	8	—	8	—	8	mA	CMOS Interface R _{AS} , C _{AS} ≥ V _{CC} - 0.2V, D _{out} = High-Z	
R _{AS} Only Refresh Current	I _{CC3}	—	480	—	400	—	360	mA	t _{RC} = Min	2
Standby Current	I _{CC5}	—	40	—	40	—	40	mA	R _{AS} = V _{IH} , C _S = V _{IL} , D _{out} = Enable	1
C _{AS} Before R _{AS} Refresh Current	I _{CC6}	—	480	—	400	—	320	mA	t _{RC} = Min	
Static Column Mode Current	I _{CC9}	—	480	—	400	—	320	mA	Static Column Mode t _{PC} = Min	1, 3
Input Leakage Current	I _{LI}	- 10	10	- 10	10	- 10	10	μA	0V ≤ v _{in} ≤ 7V	
Output Leakage Current	I _{LO}	- 10	10	- 10	10	- 10	10	μA	0V ≤ V _{out} ≤ 7V, D _{out} = Disable	
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	I _{out} = - 5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	I _{out} = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed less than three times while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CS} = V_{IH}$.



• Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	55	pF	1
Input Capacitance (Clock)	C_{I2}	—	70	pF	1, 2
Input/Output Capacitance (DQ_0 – DQ_7)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CS} = V_{IH}$ to disable D_{out} .

• AC Characteristics

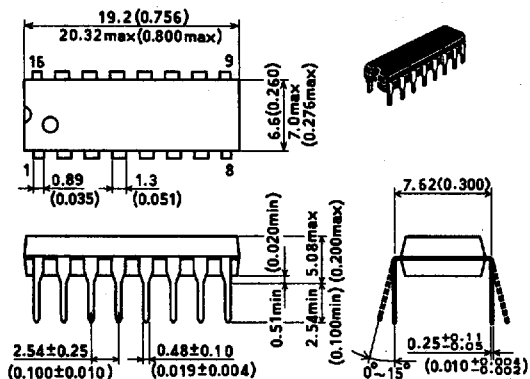
Please show at HM511002H series about AC Characteristics. But don't use by Delayed Write Cycle, because the HB56C18 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}(\text{min})$).

T-90-20

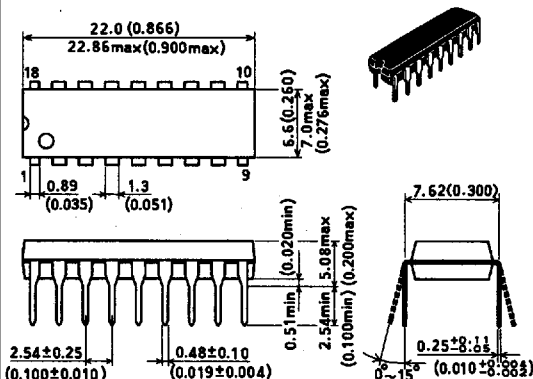
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

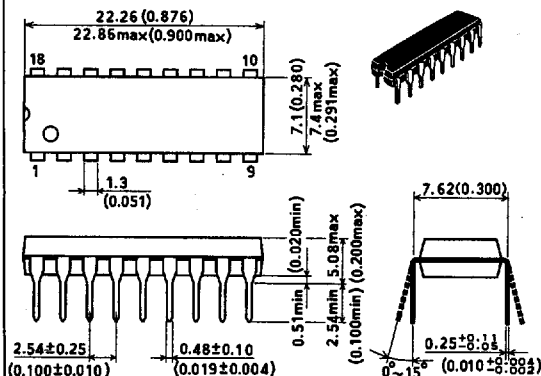
• DP-16B



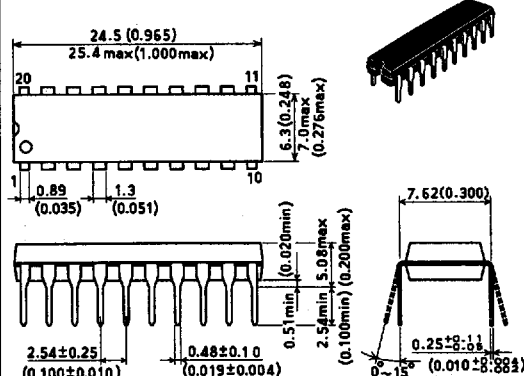
• DP-18B



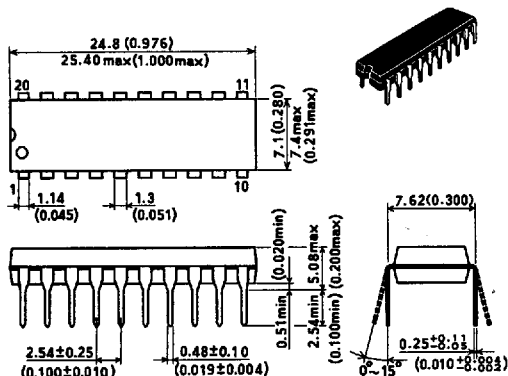
• DP-18C



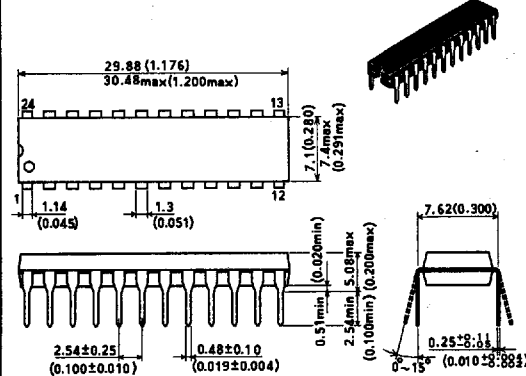
• DP-20N



• DP-20NA



• DP-20NC

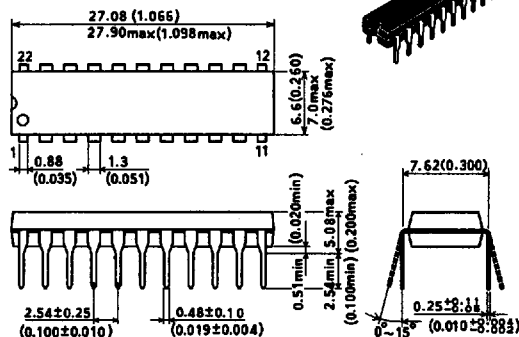


• Dual-In-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

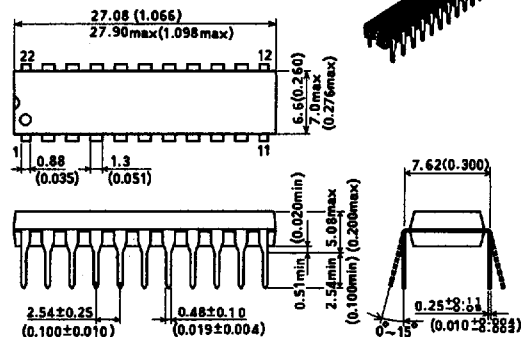
Unit: mm (inch) Scale 3/2

• DP-22N

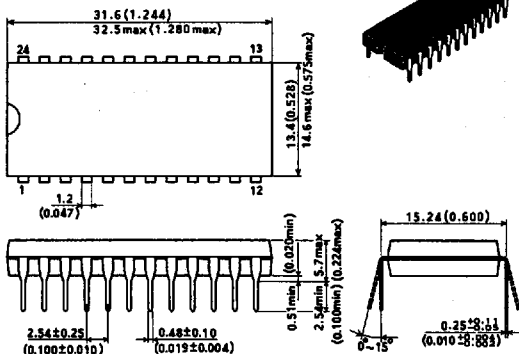


• DP-22NB

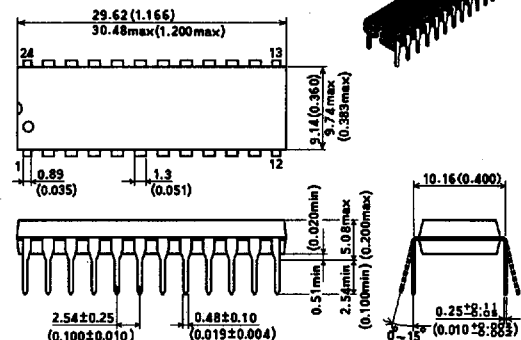
T-90-20



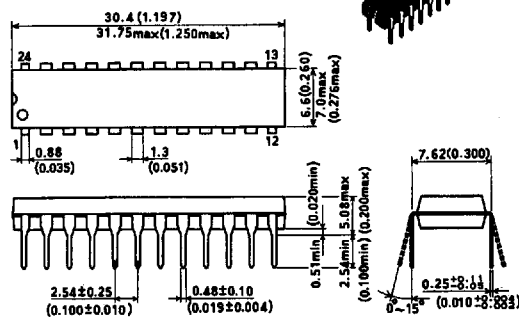
• DP-24



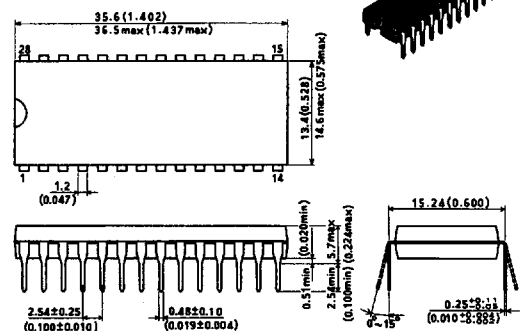
• DP-24A



• DP-24N



• DP-28

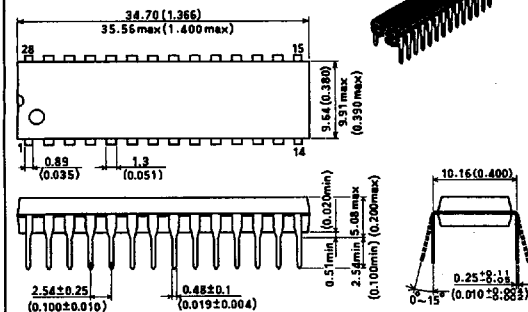


• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

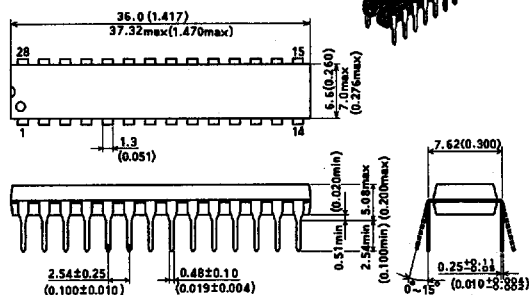
Unit: mm (inch) Scale 3/2

• DP-28C

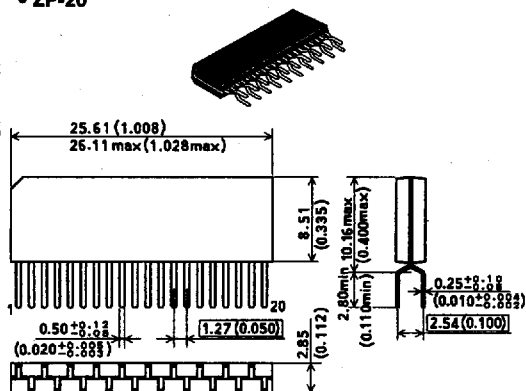


• DP-28N

T-90-20

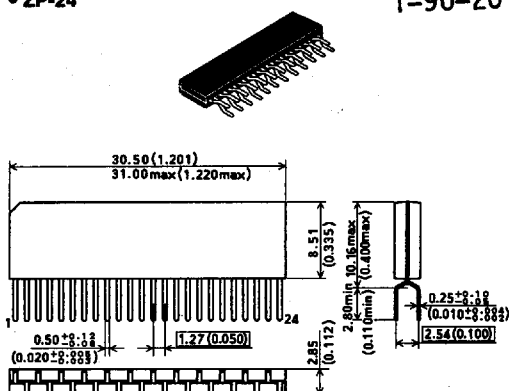


• ZP-20

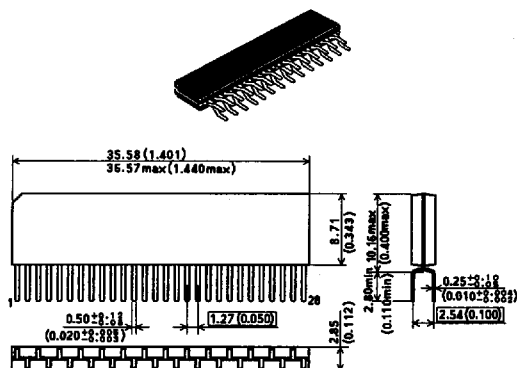


• ZP-24

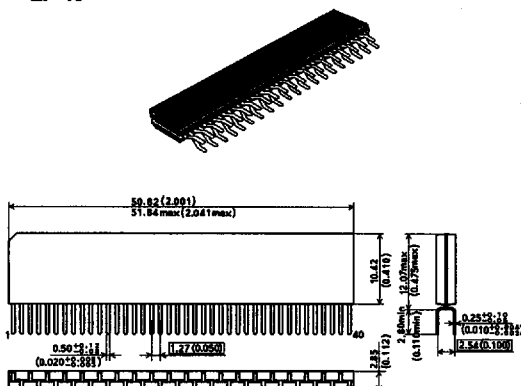
T-90-20



• ZP-28



• ZP-40



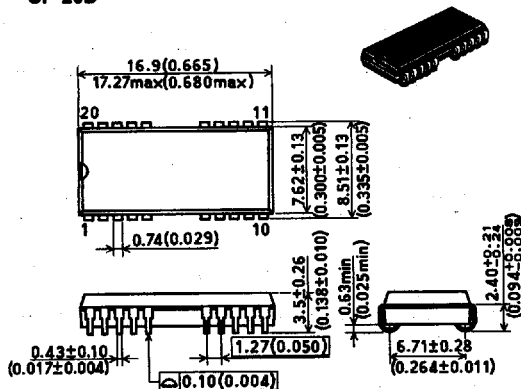
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

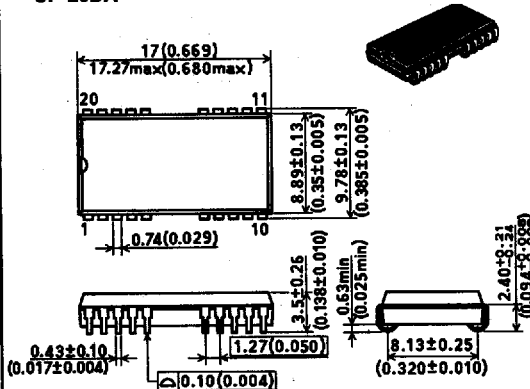
Unit: mm (inch) Scale 3/2

T-90-20

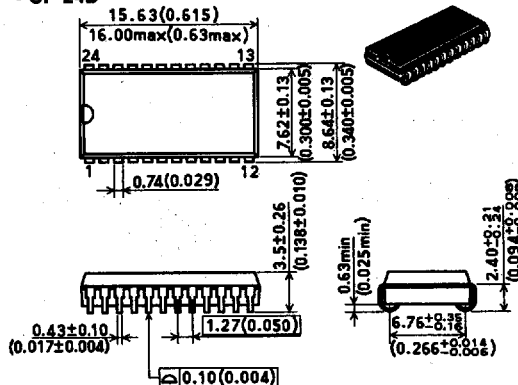
• CP-20D



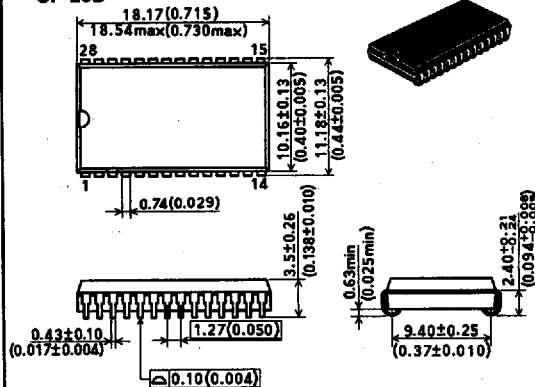
• CP-20DA



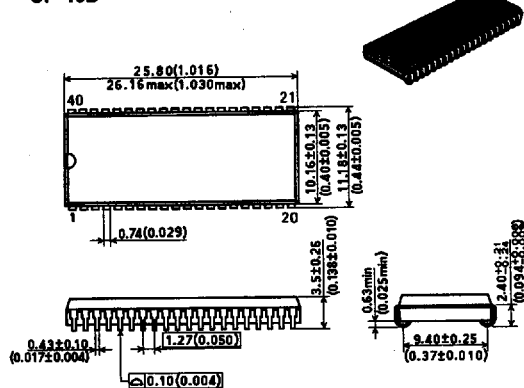
• CP-24D



• CP-28D



• CP-40D

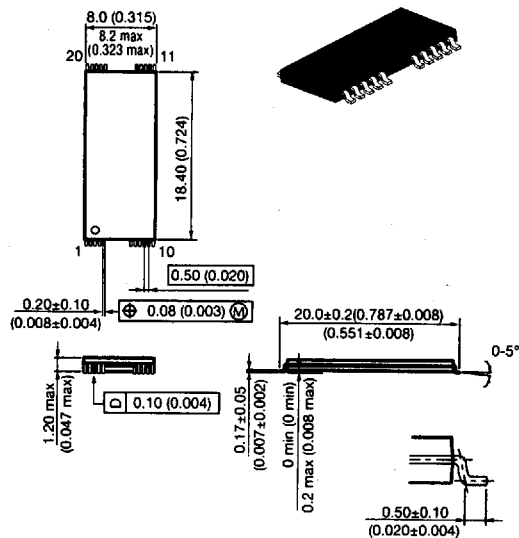


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

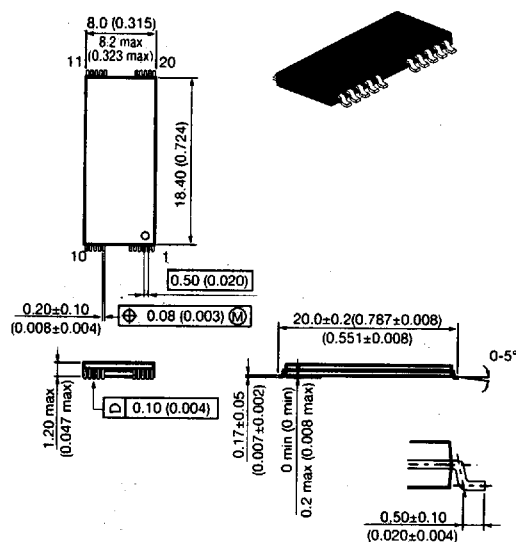
Unit: mm (inch) Scale 3/2

• TFP-20DA

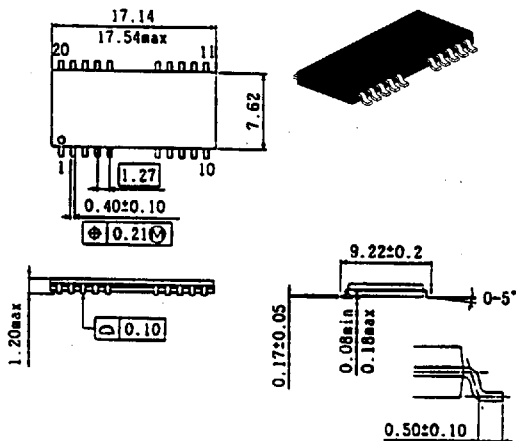


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

