HB56D236B/SB Series

T-46-23-18

2,097,152-Word x 36-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56D236B/SB/BS/SBS is a 2M x 36 dynamic RAM module, mounted 16 pieces of 4 Mbit DRAM (HM514400JP/AJ) sealed in SOJ package and 8 pieces of 1 Mbit DRAM (HM511000JP) sealed in SOJ package (HB56D236B/SB or 8 pieces of 1 Mbit DRAM (HM511000ATS) sealed in TSOP package (HB56D236SB/SBS). An outline of the HB56D236B/SB/BS/SBS is 72-pin single in-line package. Therefore, the HB56D236B/SB/BS/SBS makes high density mounting possible without surface mount technology. The HB56D236B/SB/BS/SBS provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ or beside each TSOP but only on the one side of its module board.

FEATURES

- 72-pin Single In-line Package
  - Lead Pitch .....1.27 mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .6.825W/6.195W/5.565W/4.935W (max)
  - Standby Mode .....252 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle .....(16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

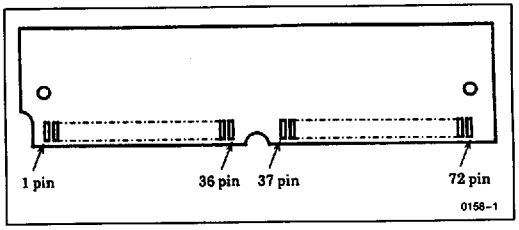
ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56D236B/BS-6A	60 ns	72-pin SIP Socket Type	Gold
HB56D236B/BS-7A	70 ns		
HB56D236B/BS-8A	80 ns		
HB56D236B/BS-10A	100 ns		
HB56D236B-8	80 ns		
HB56D236B-10	100 ns		
HB56D236SB/SBS-6A	60 ns	72-pin SIP Socket Type	Solder
HB56D236SB/SBS-7A	70 ns		
HB56D236SB/SBS-8A	80 ns		
HB56D236SB/SBS-10A	100 ns		
HB56D236SB-8	80 ns		
HB56D236SB-10	100 ns		

PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D236B/SB/BS/SBS					
		-6A	-7A	-8A	-10A	-8	-10
67	PD1	NC	NC	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC	NC	NC
69	PD3	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}
70	PD4	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}

PIN OUT

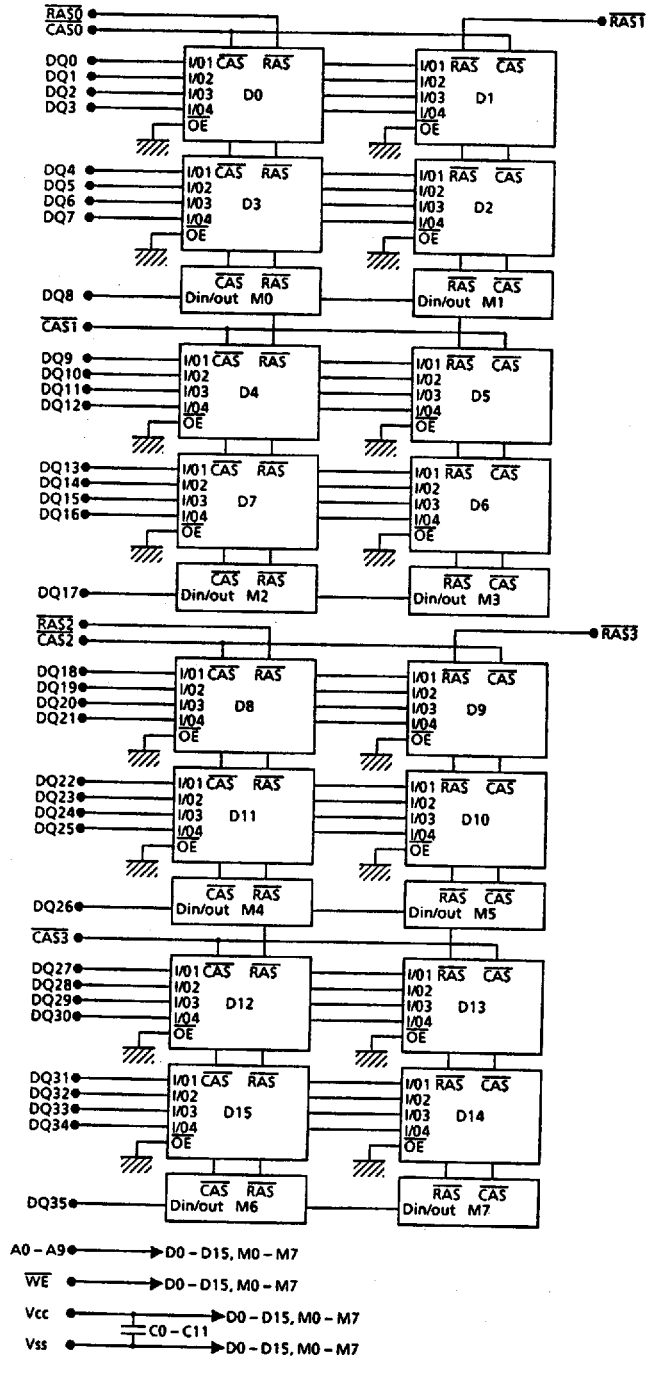


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS1}$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	$\overline{RAS1}$	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD1
14	A_2	32	A_9	50	DQ_{27}	68	PD2
15	A_3	33	$\overline{RAS3}$	51	DQ_{10}	69	PD3
16	A_4	34	$\overline{RAS2}$	52	DQ_{28}	70	PD4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	No Connection

BLOCK DIAGRAM



*D0–D15: HM514400JP/AJ
M0–M7: HM511000JP/ATS

PHYSICAL OUTLINE

HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm / inch

• HB56D236B/SB

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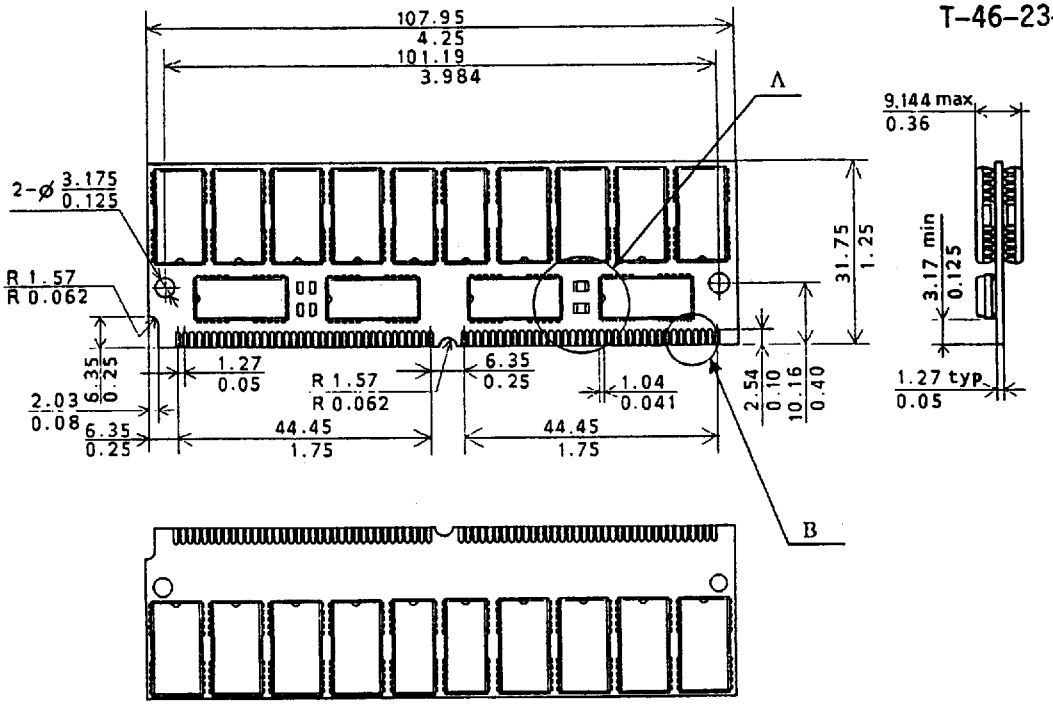
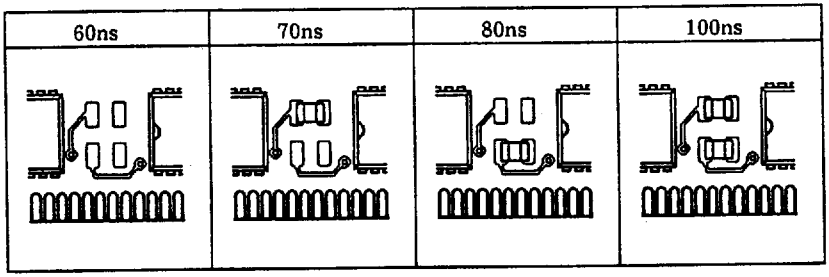
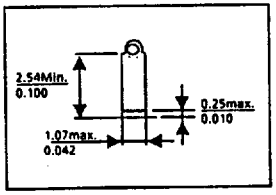


D158-3

Detail A



Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D236B-XX	Gold
HB56D236SB-XX	Solder

D158-4

■ **PHYSICAL OUTLINE** (continued) HITACHI/ LOGIC/ARRAYS/MEM Unit: mm / inch

• **HB56D236BS/SBS**

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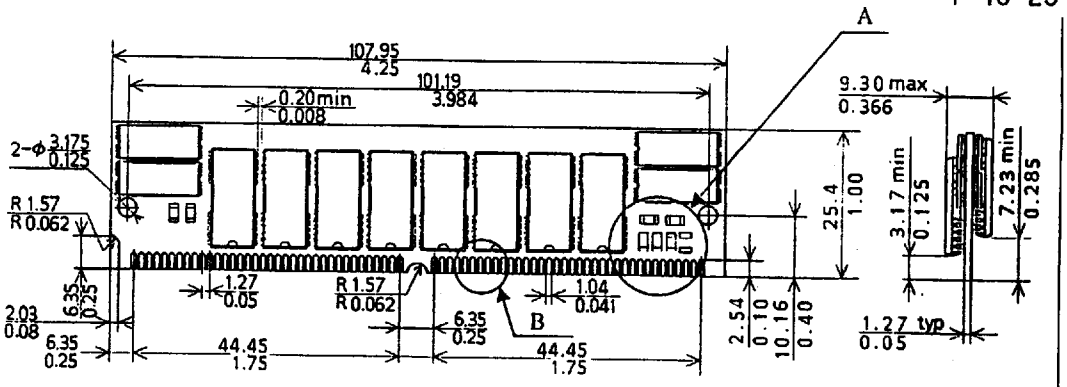

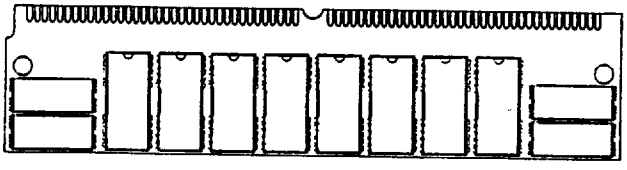

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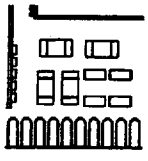
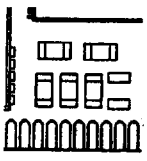
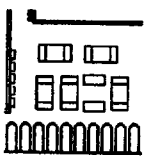
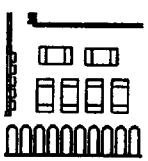
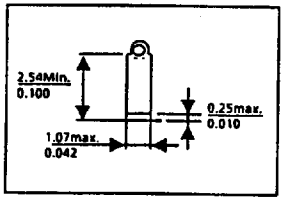
Detail A

60ns	70ns	80ns	100ns
			

Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D236BS-XX	Gold
HB56D236SBS-XX	Solder

0158-6

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1300	—	1180	—	1060	—	940	—	1060	—	940	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	48	—	48	—	48	—	48	—	48	—	48	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	24	—	24	—	24	—	24	—	24	—	24	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1300	—	1180	—	1020	—	900	—	1020	—	900	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	120	—	120	—	120	—	120	—	120	—	120	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1260	—	1140	—	1020	—	900	—	1020	—	900	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	1260	—	1140	—	980	—	900	—	980	—	900	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output Capacitance ($DQ_{0-7, 9-16, 18-25, 27-34}$)	$C_{I/O1}$	—	29	pF	1, 2
Output Capacitance ($DQ_{8, 17, 26, 35}$)	$C_{I/O2}$	—	39	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	160	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	25	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	12	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	22	55	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	17	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	20	—	25	ns	6

Write Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	20	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DD}	15	—	15	—	20	—	20	—	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

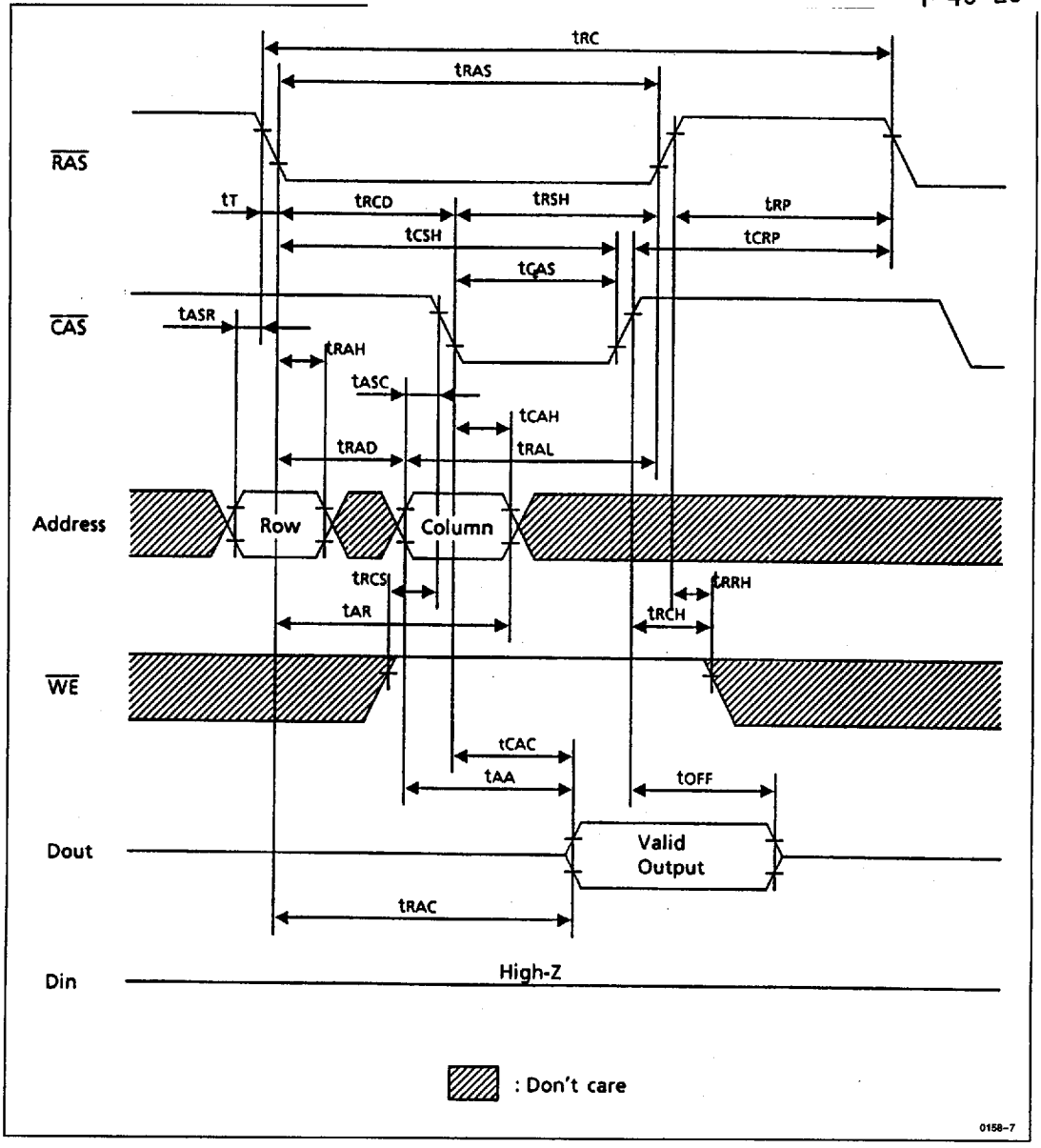
Fast Page Mode Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	50	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	50	—	50	—	ns	

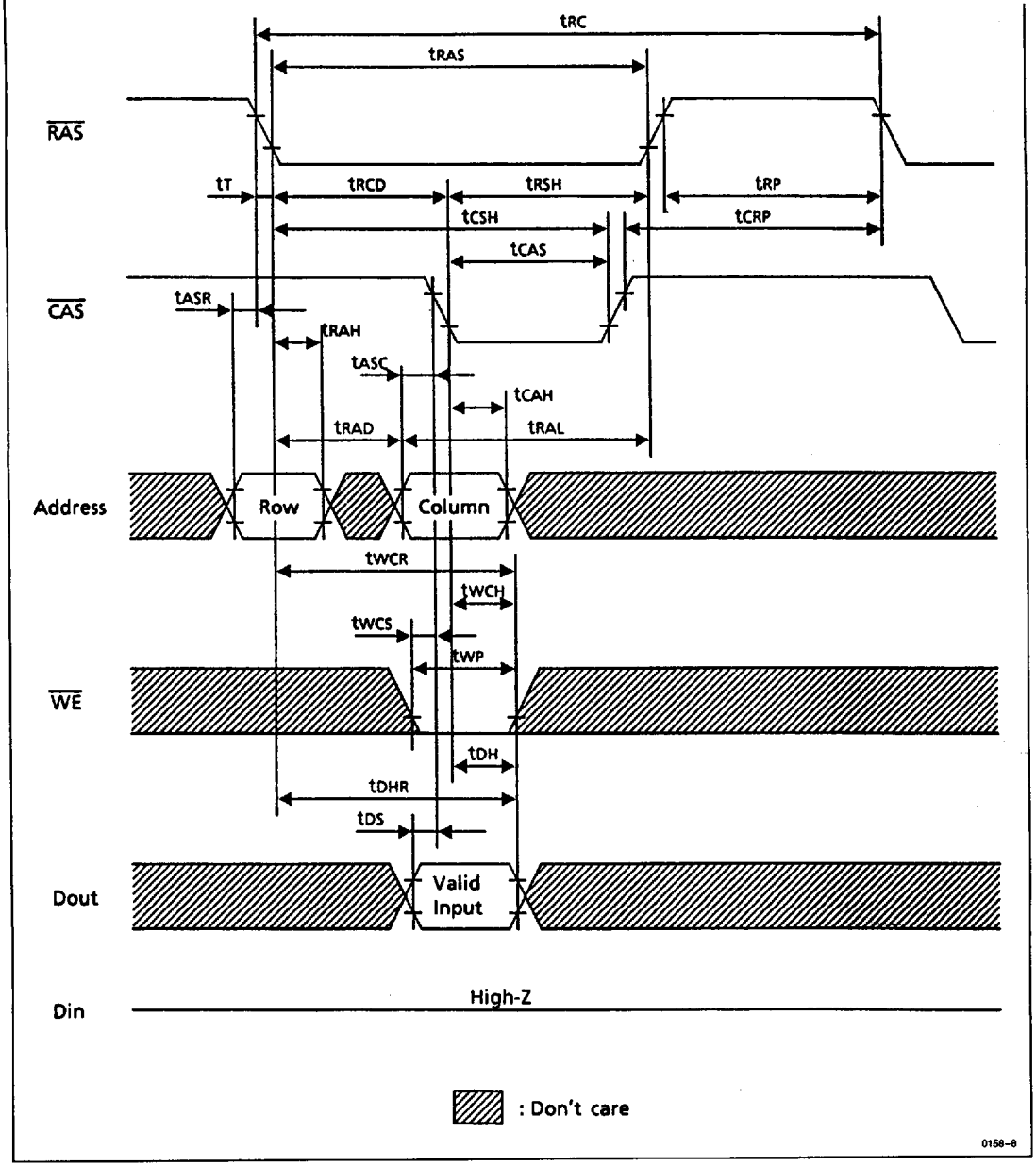
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refrersh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

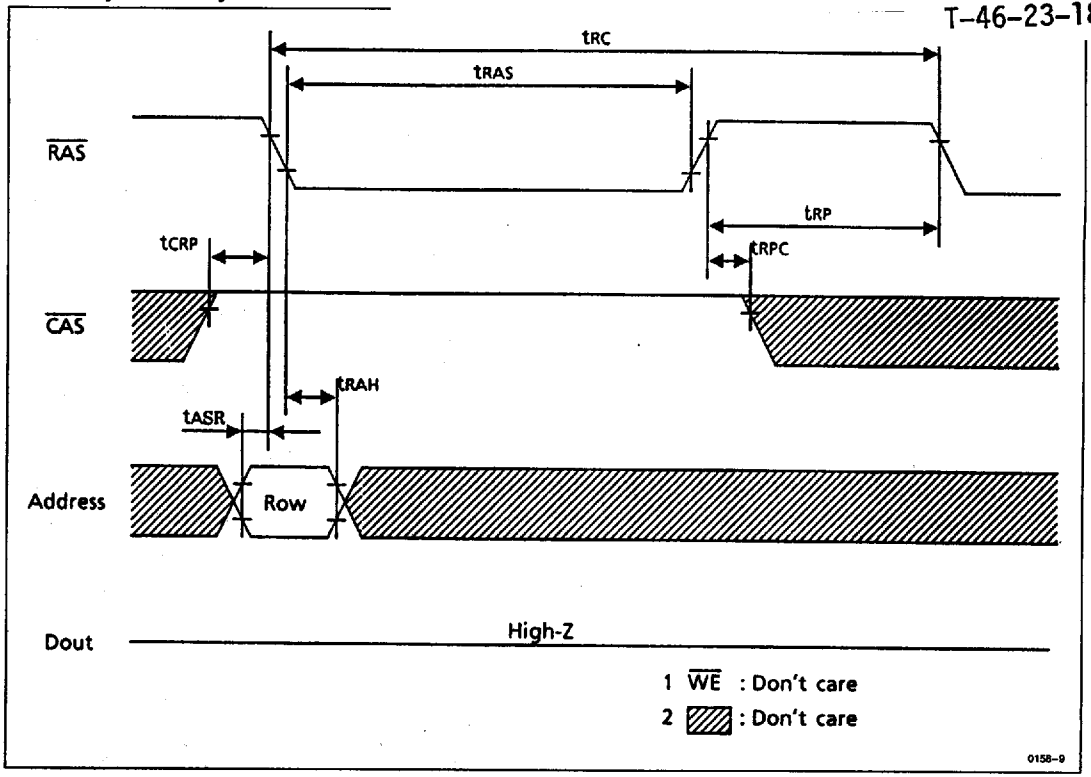
• Read Cycle



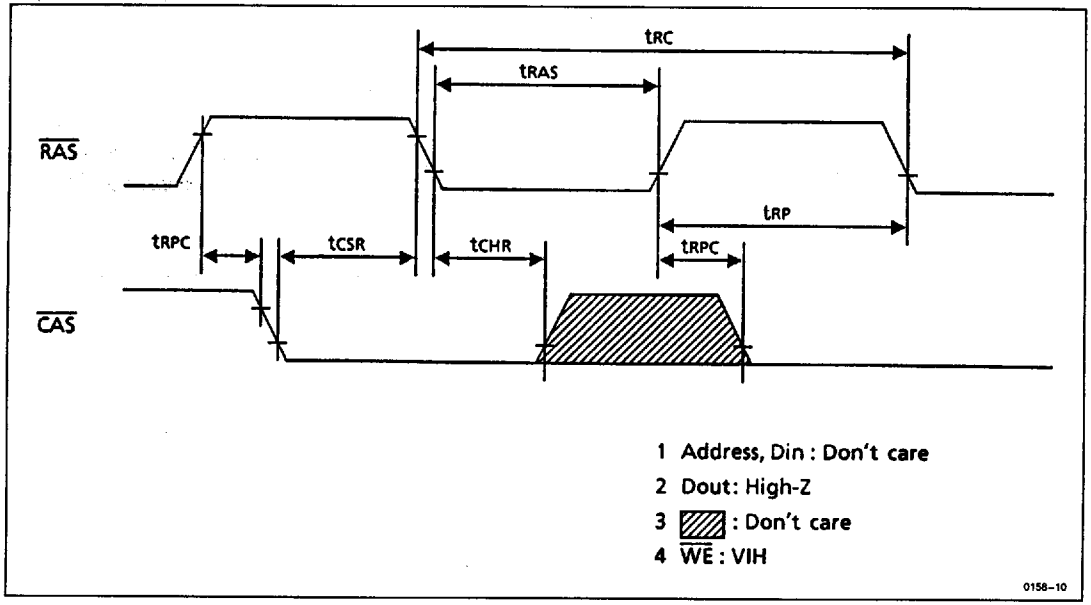
• Early Write Cycle



• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Fast Page Mode Read Cycle

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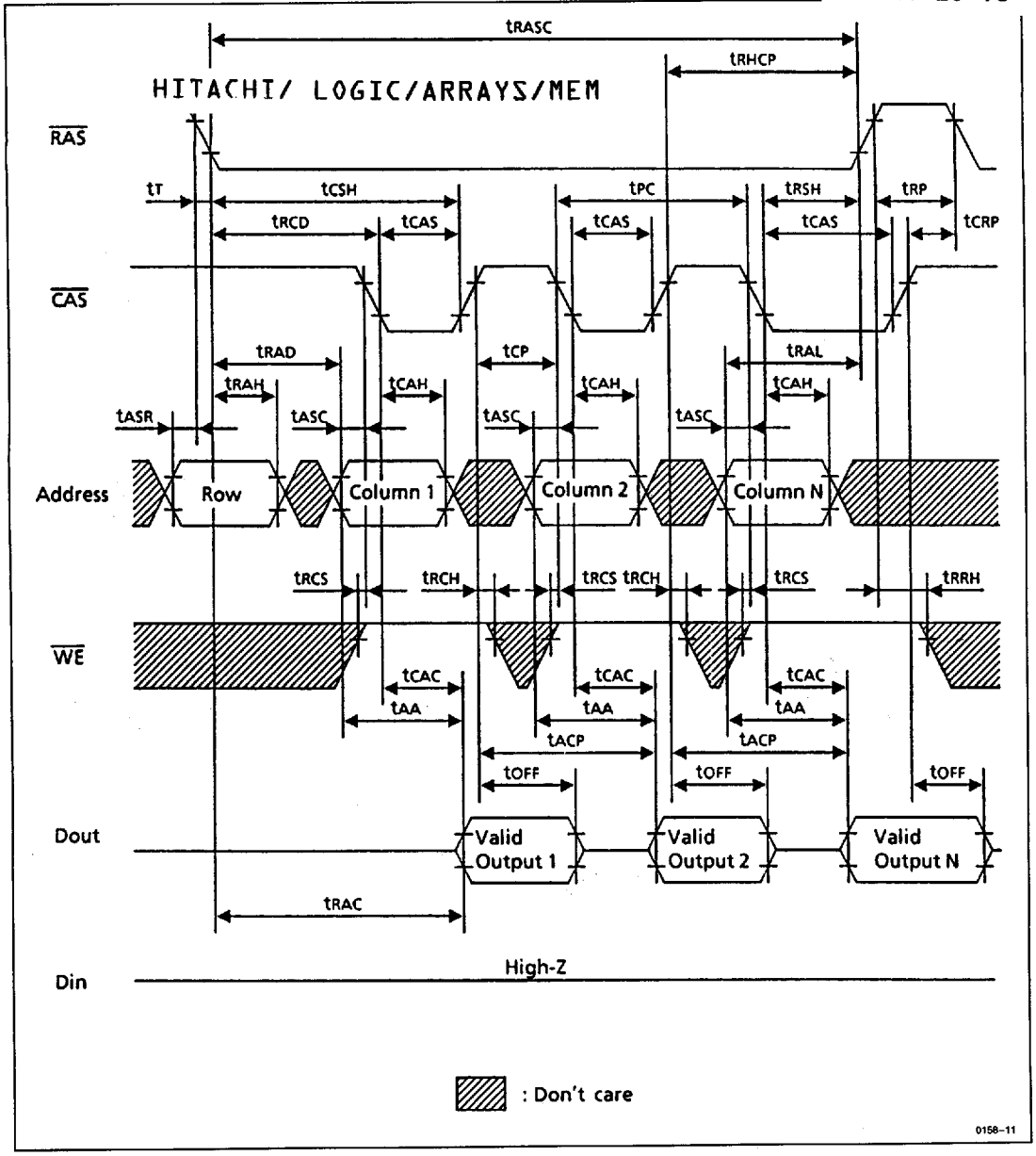
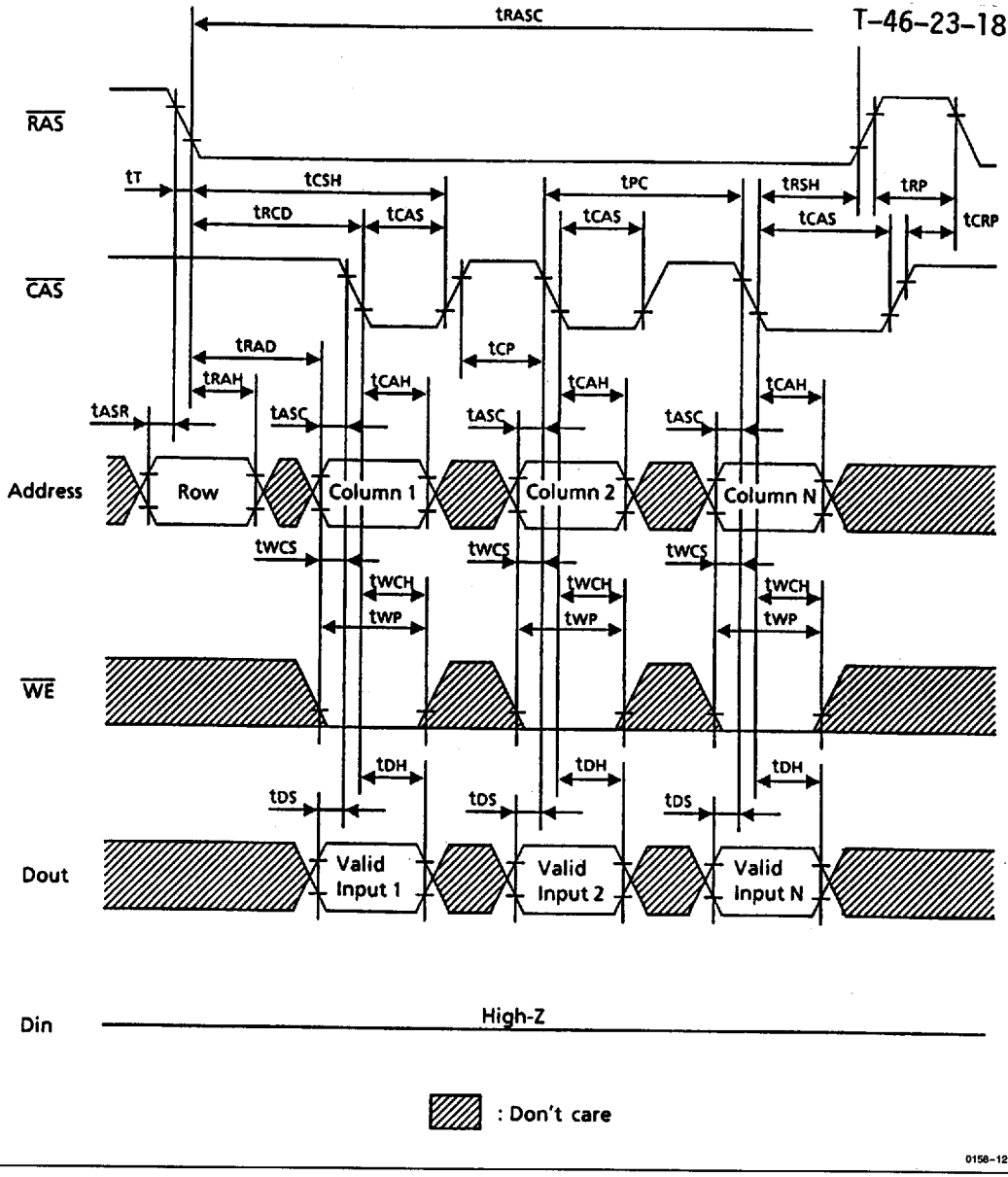


T-46-23-18


tRASC
RAS
tT
tCSH
tPC
tRSH
tRP
tRCD
tCAS
tCAS
tCAS
tCRP
CAS
tRAD
tCP
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Address
Row
Column 1
Column 2
Column N
tWCS
tWCS
tWCS
tWCH
tWCH
tWCH
tWP
tWP
tWP
WE
tDH
tDH
tDH
tDS
tDS
tDS
Dout
Valid Input 1
Valid Input 2
Valid Input N
Din
High-Z
: Don't care
0158-12

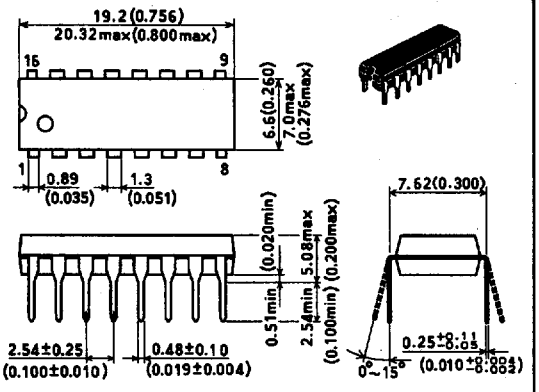
PACKAGE INFORMATION

T-90-20

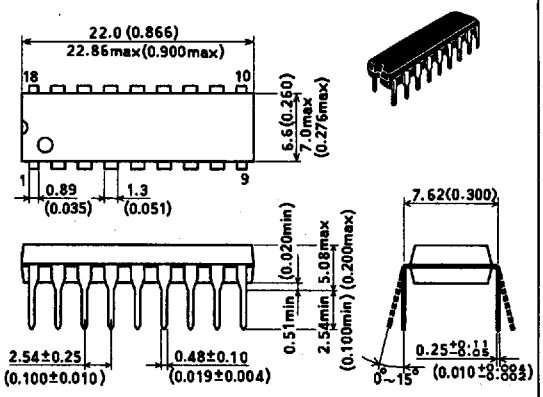
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

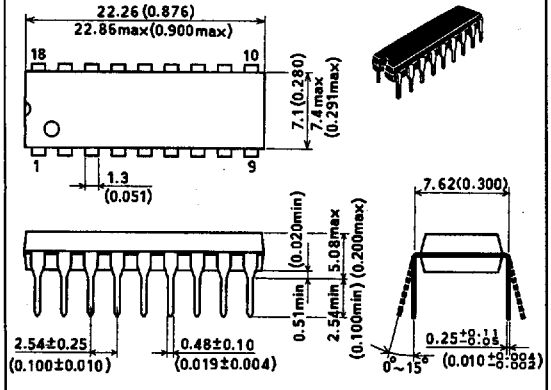
• DP-16B



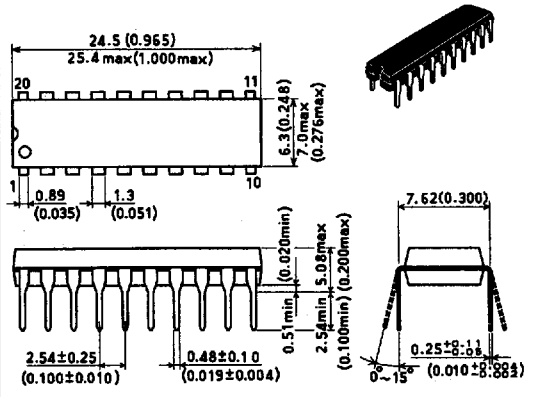
• DP-18B



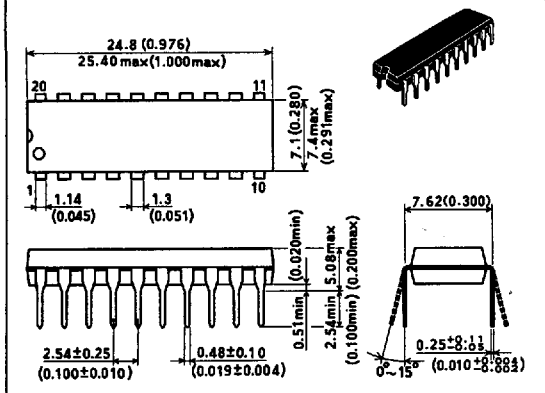
• DP-18C



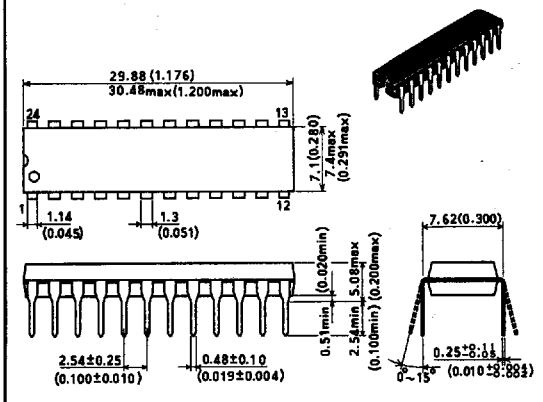
• DP-20N



• DP-20NA



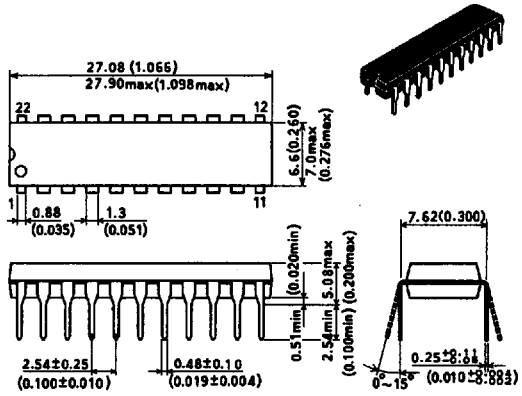
• DP-20NC



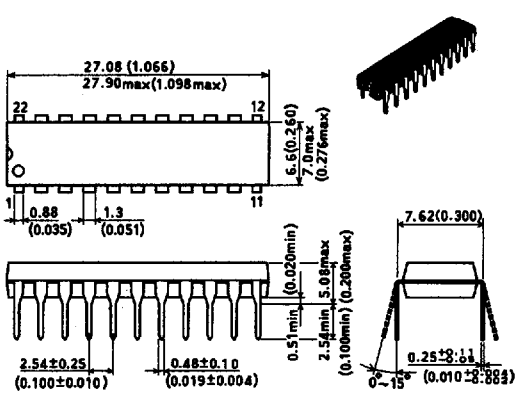
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

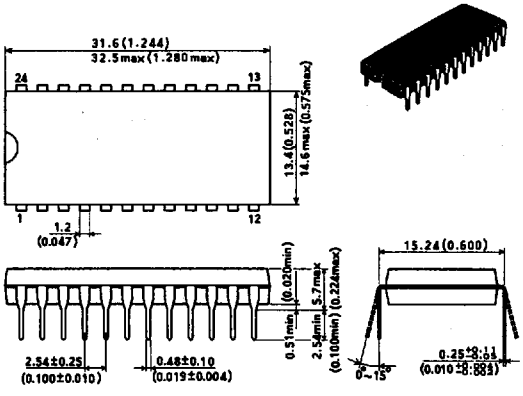
• DP-22N



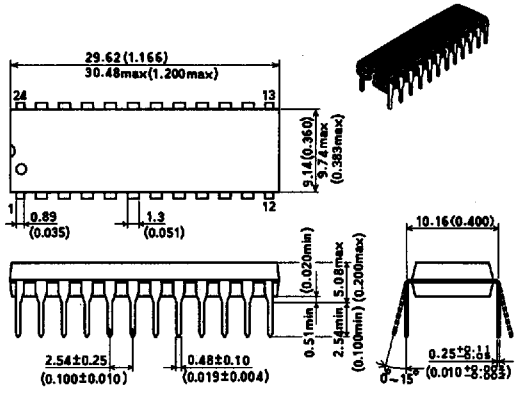
• DP-22NB



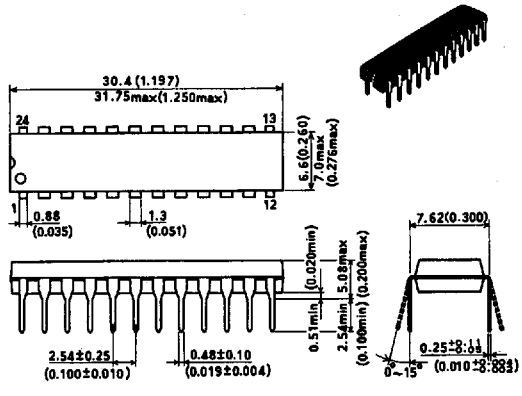
• DP-24



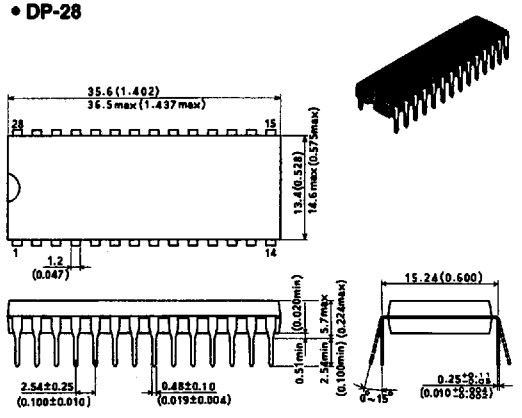
• DP-24A



• DP-24N



• DP-28



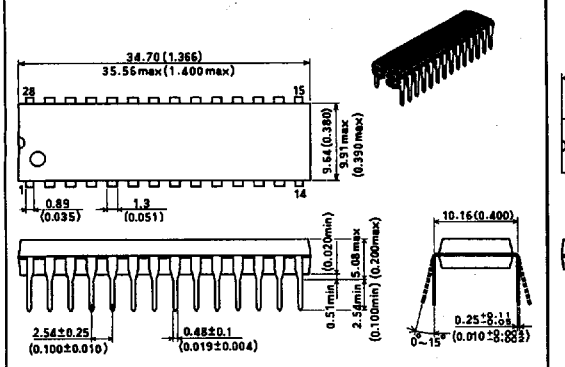
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

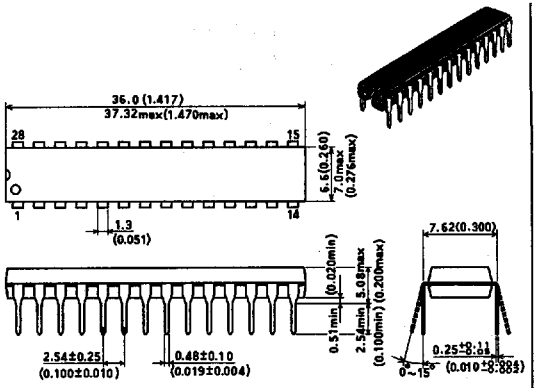
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

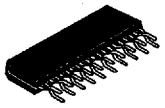


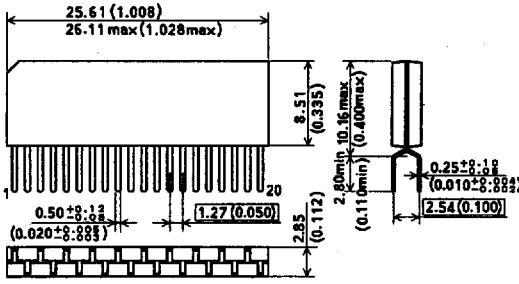
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

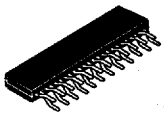
T-90-20

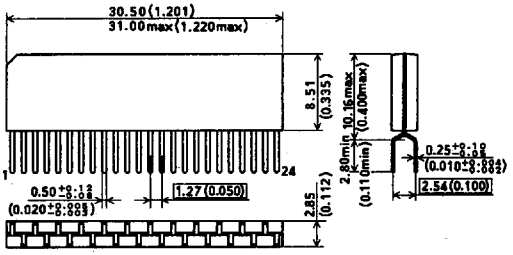
• ZP-20



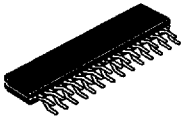


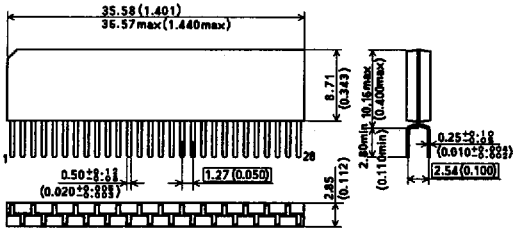
• ZP-24



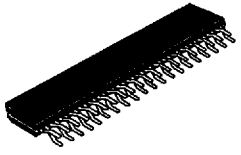


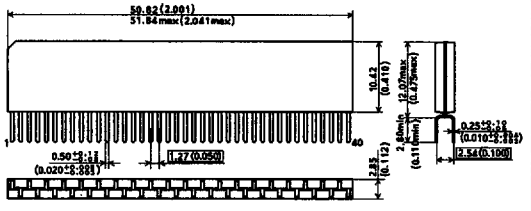
• ZP-28





• ZP-40





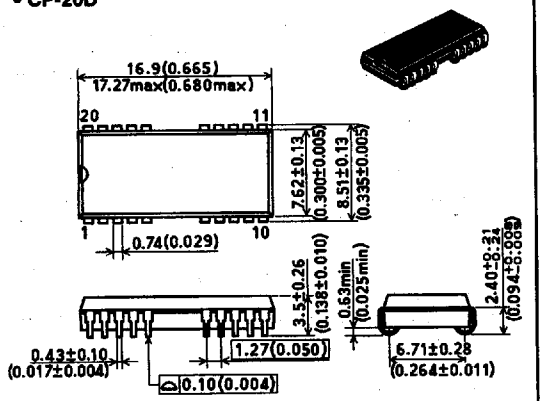
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

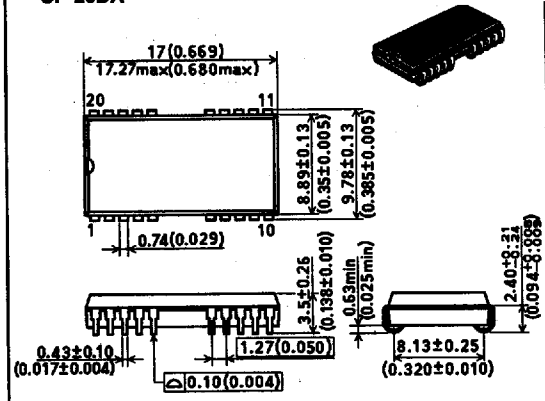
Unit: mm (inch) Scale 3/2

T-90-20

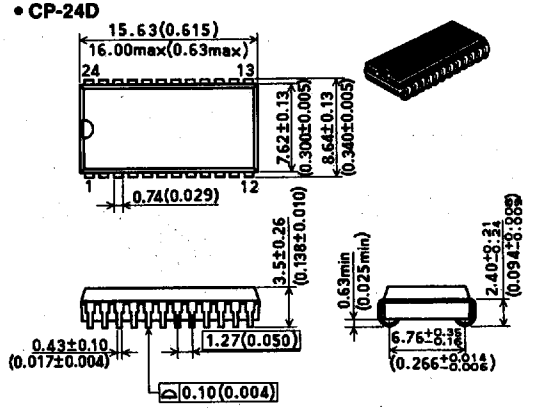
• CP-20D



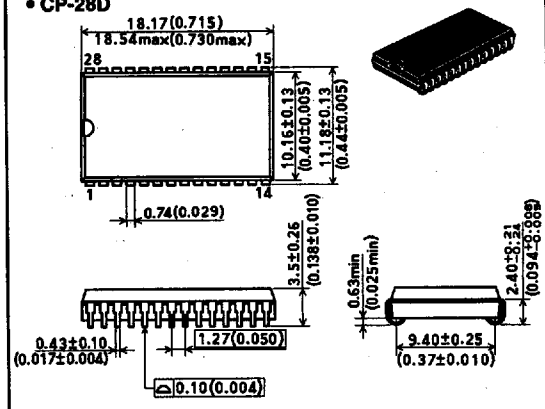
• CP-20DA



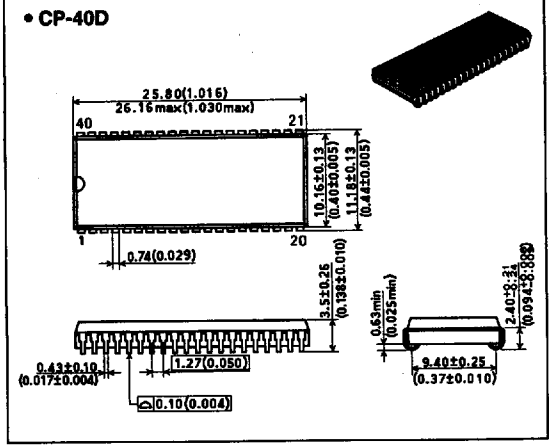
• CP-24D



• CP-28D



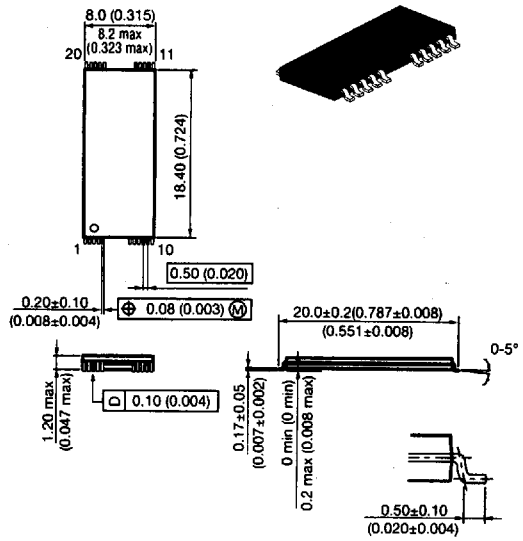
• CP-40D



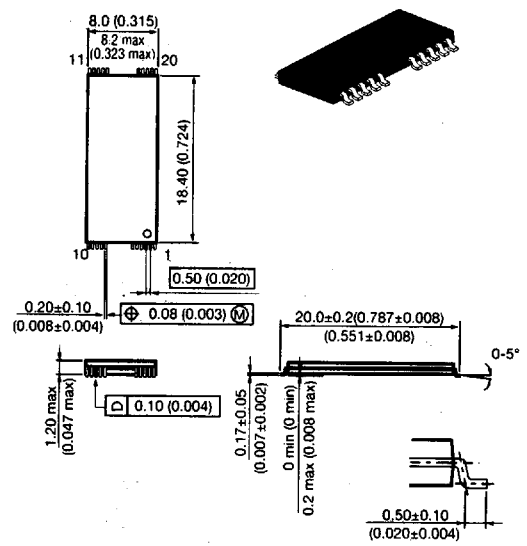
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

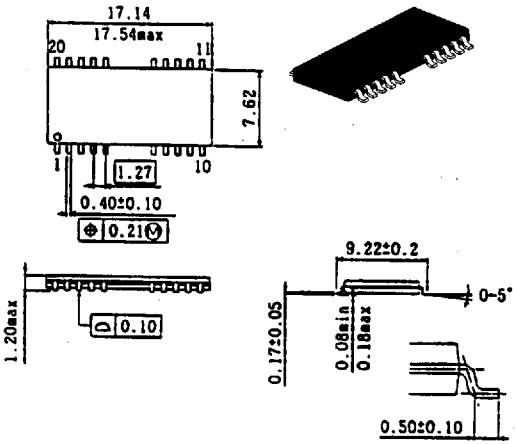
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR