HB56D25632 Series

T-46-23-17

262,144-Word x 32-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56D25632B is a 256k x 32 dynamic RAM module, mounted 8 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package. An outline of the HB56D25632B is 72-pin single in-line package. Therefore, the HB56D25632B makes high density mounting possible without surface mount technology. The HB56D25632B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

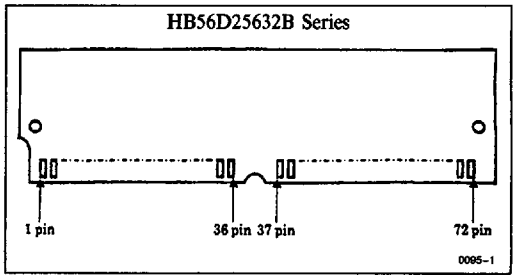
FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode .....3.78W/3.36W/2.772W/2.31W/1.974W (max)
  - Standby Mode.....84 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle/8 ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25632B-6A	60 ns	72-pin SIP Socket Type
HB56D25632B-7A	70 ns	
HB56D25632B-8A	80 ns	
HB56D25632B-10A	100 ns	
HB56D25632B-12A	120 ns	

PIN OUT

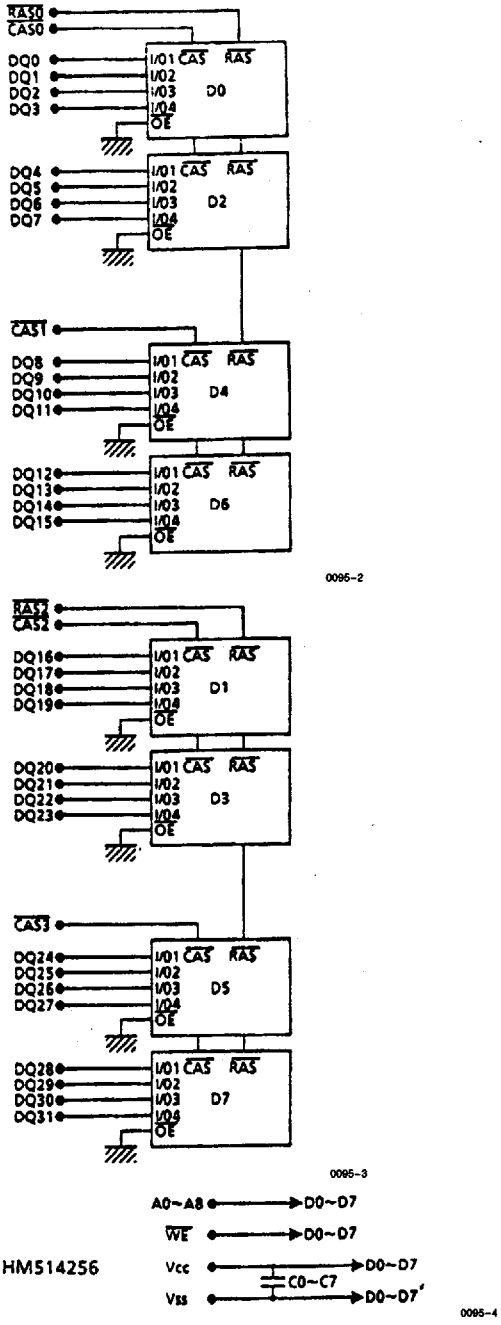


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	V_{SS}
14	A2	32	NC	50	DQ24	68	NC
15	A3	33	NC	51	DQ9	69	T.B.D.
16	A4	34	$\overline{RAS2}$	52	DQ25	70	T.B.D.
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$– $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$– $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

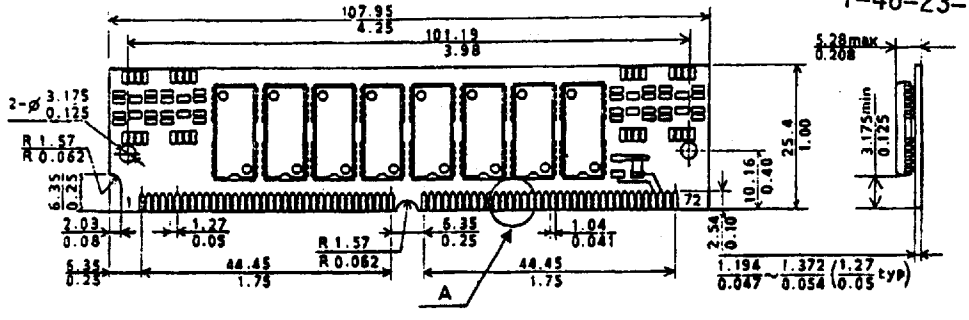


* D0~D7 : HM514256

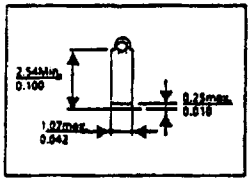
■ PHYSICAL OUTLINE

Unit: mm / inch

T-46-23-17



Detail A



Note: The plating of the contact finger is gold.

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■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note 1. All voltage referenced to V_{SS}.

T-46-23-17

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	720	—	640	—	528	—	440	—	376	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	720	—	640	—	528	—	440	—	376	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	720	—	640	—	528	—	440	—	376	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	720	—	640	—	440	—	440	—	376	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	68	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
Output Capacitance (DQ0–DQ31)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	125	—	140	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	55	—	60	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	

T-46-23-17

Read, Write and Refresh Cycle (Common Parameters) (continued)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ns	15

Read Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

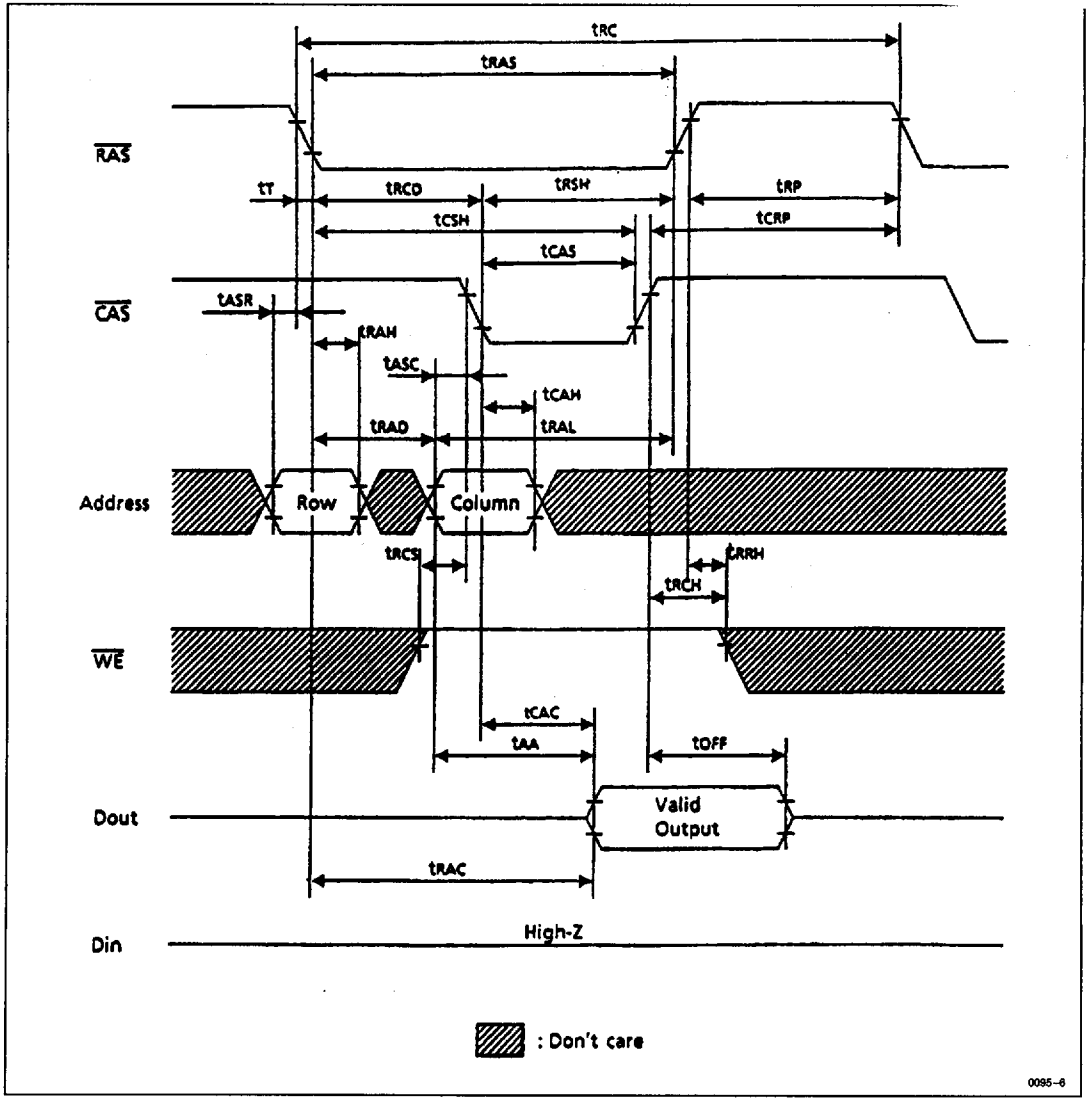
Fast Page Mode Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

■ TIMING WAVEFORM

• Read Cycle



■ Early Write Cycle

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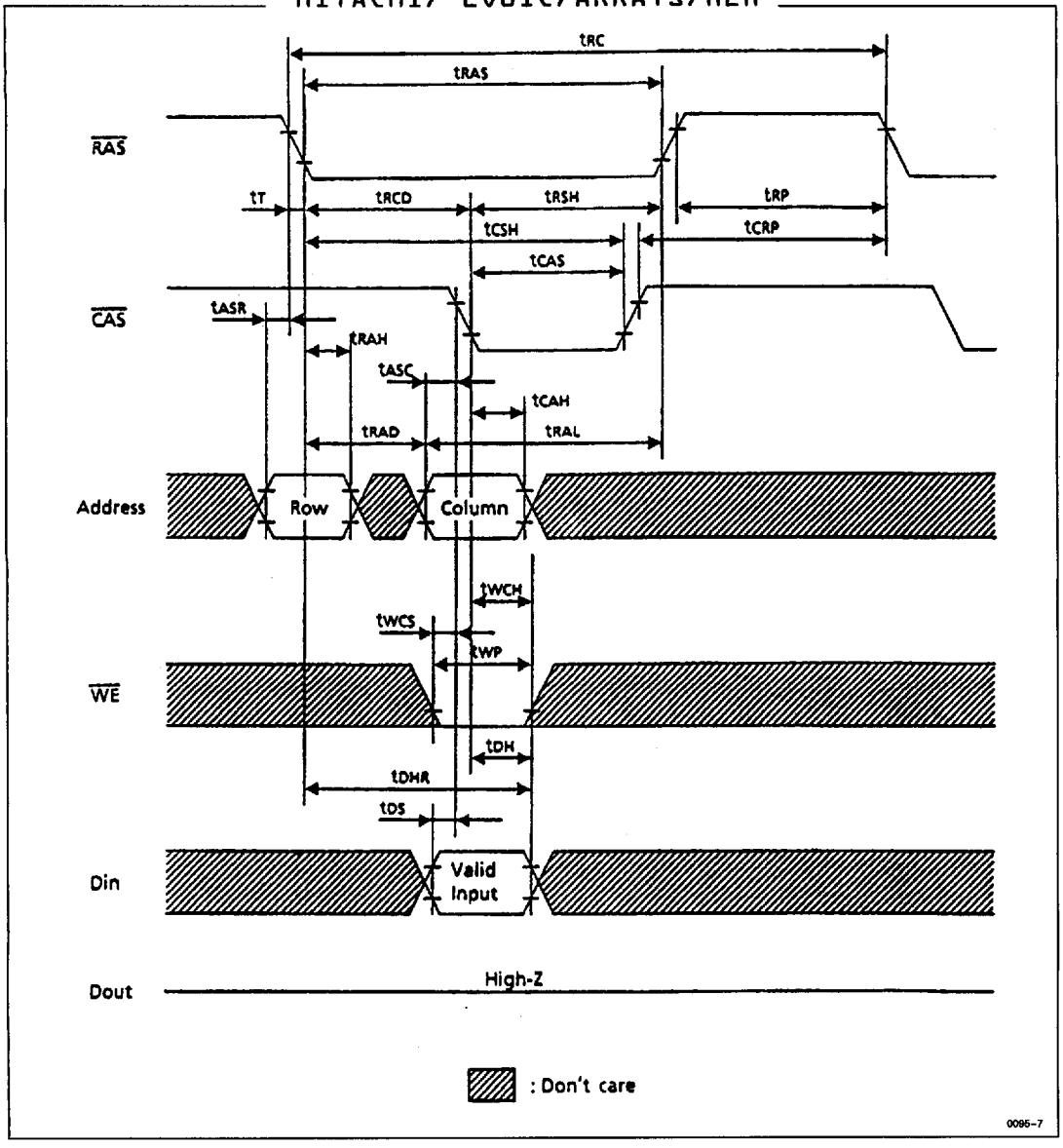
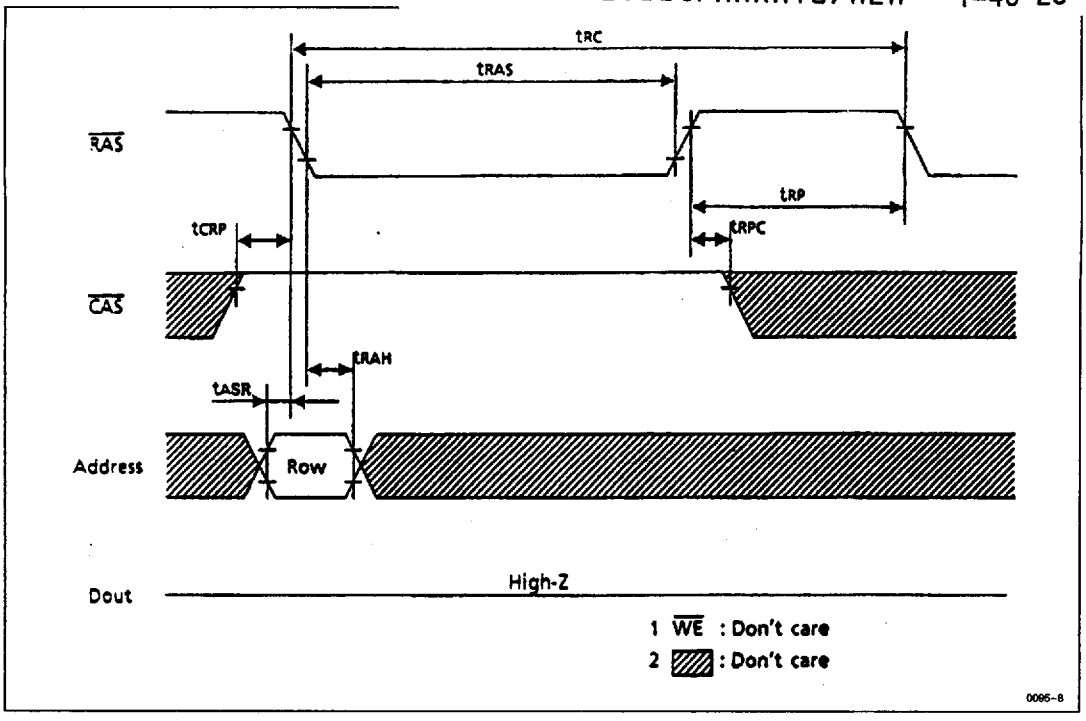
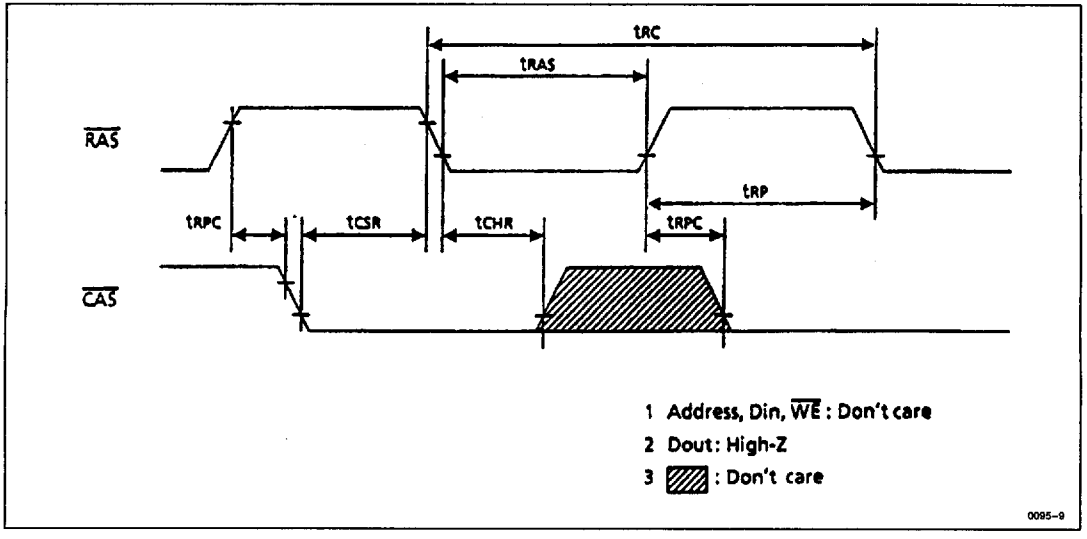


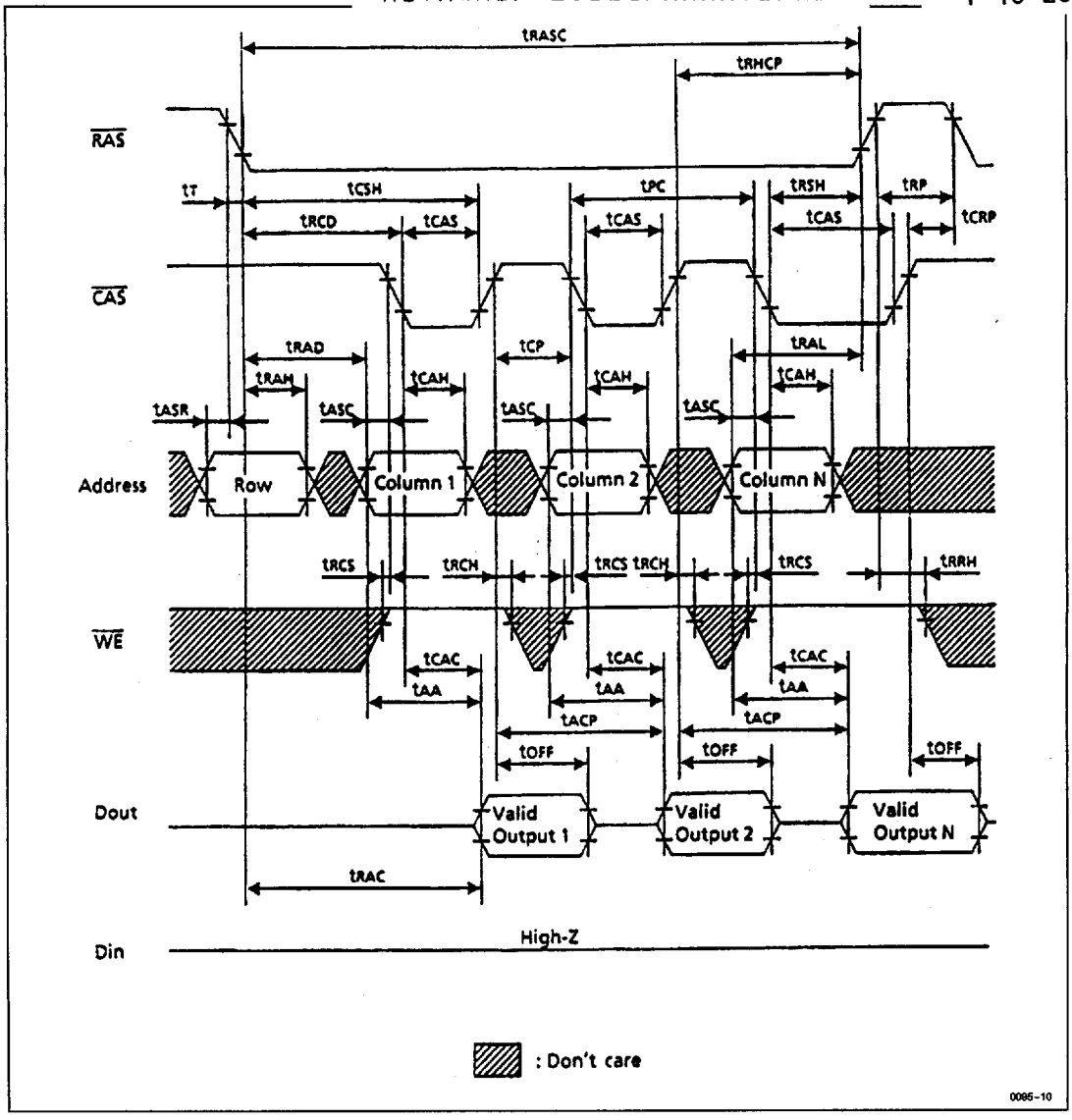
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

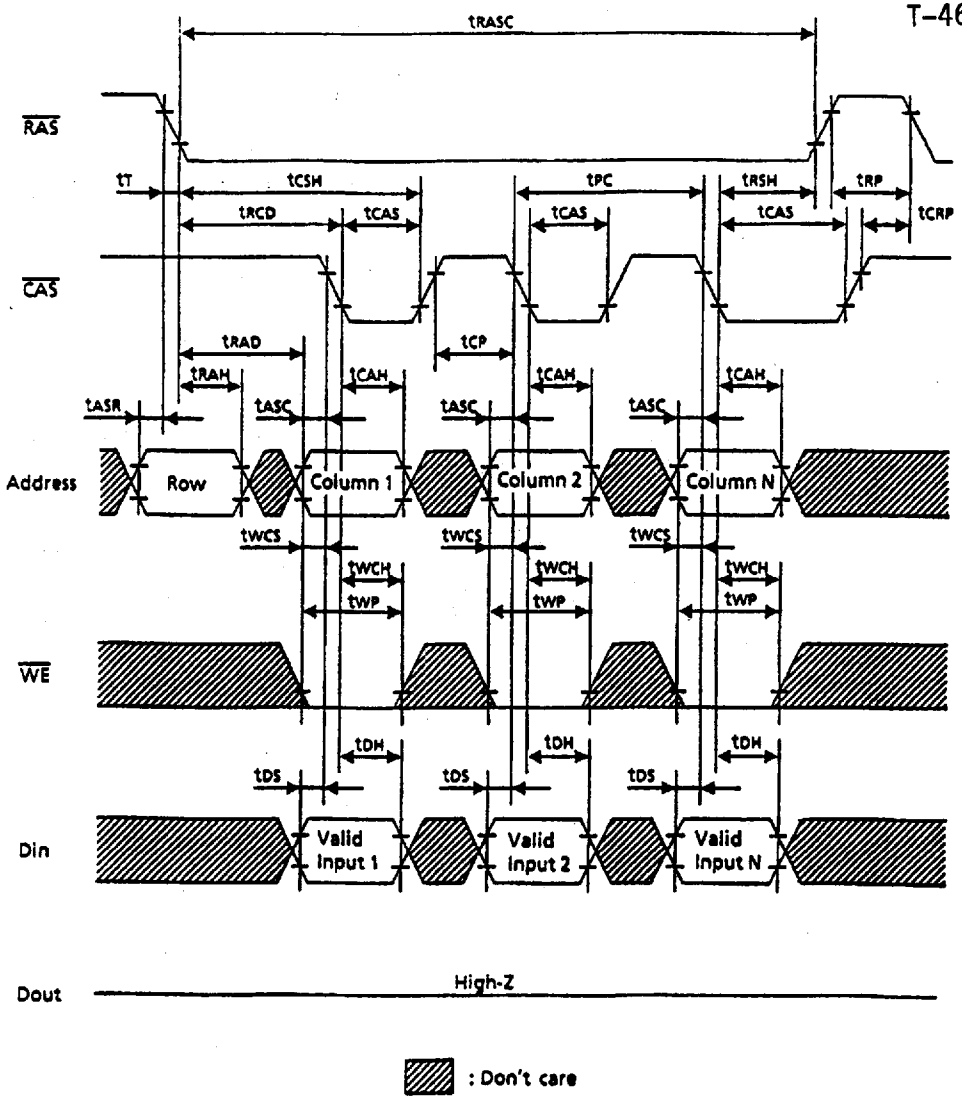


• Fast Page Mode Read Cycle



• Fast Page Mode Early Write Cycle

T-46-23-17



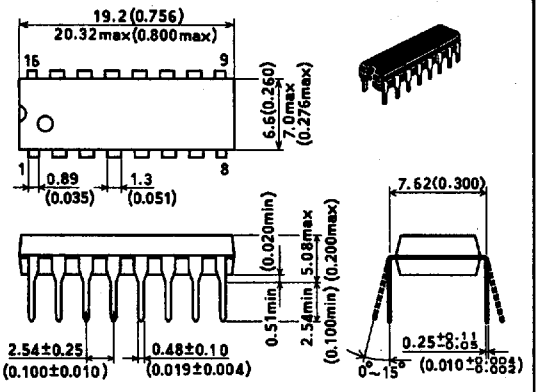
PACKAGE INFORMATION

T-90-20

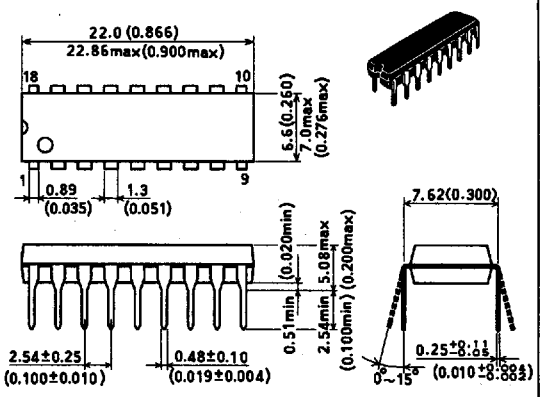
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

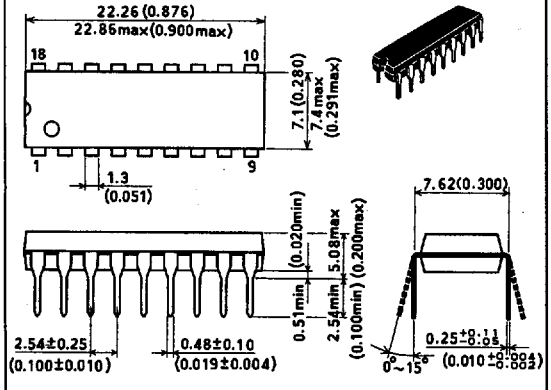
• DP-16B



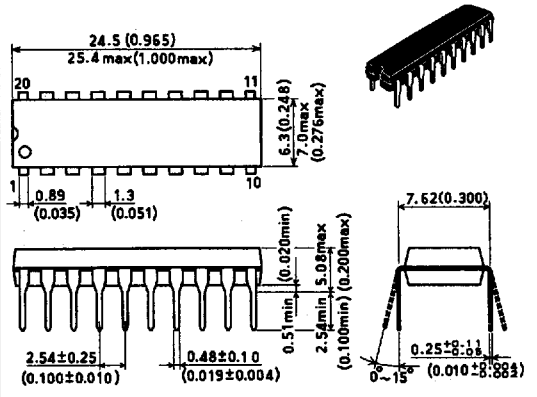
• DP-18B



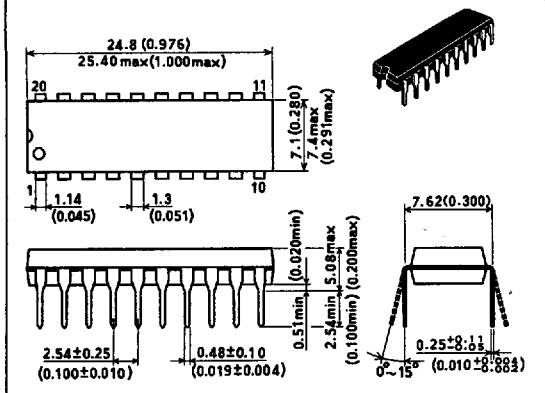
• DP-18C



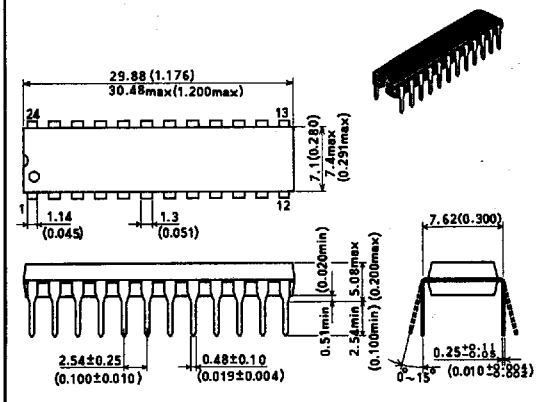
• DP-20N



• DP-20NA



• DP-20NC

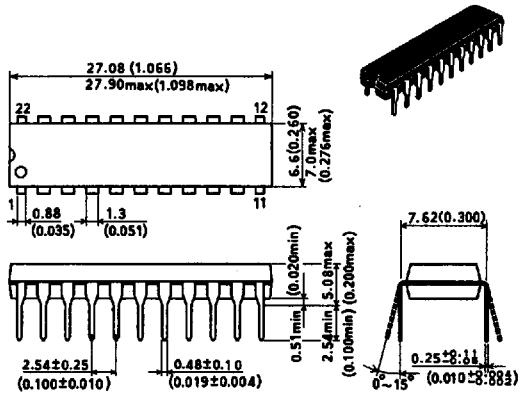


• Dual-in-line Plastic

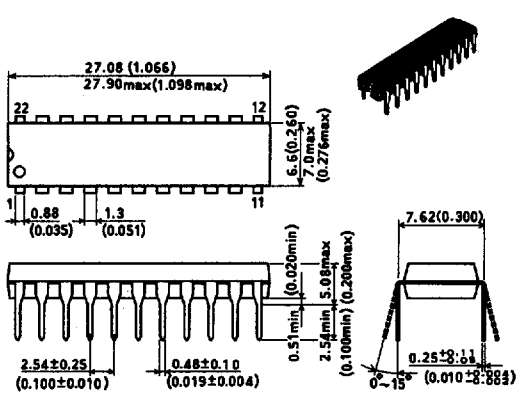
Unit: mm (inch) Scale 3/2

T-90-20

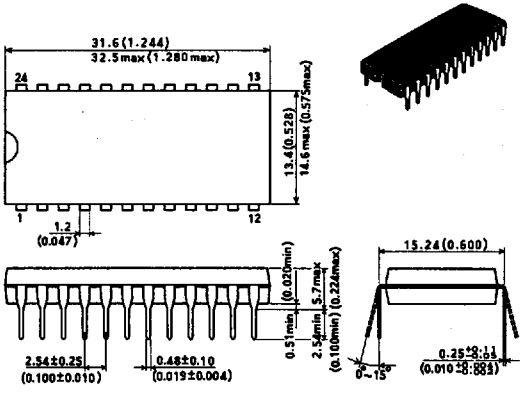
• DP-22N



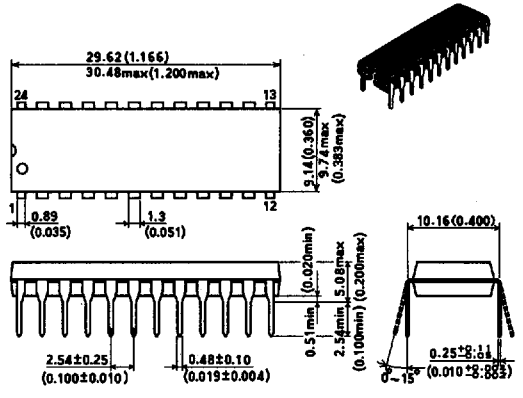
• DP-22NB



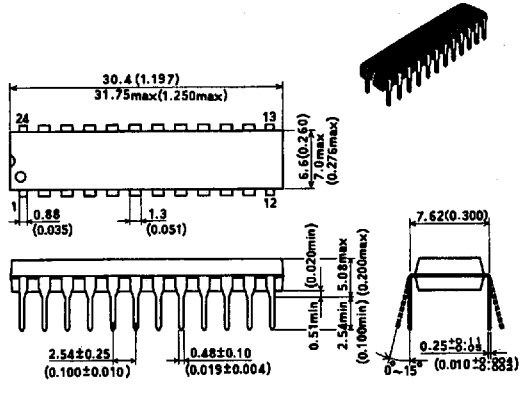
• DP-24



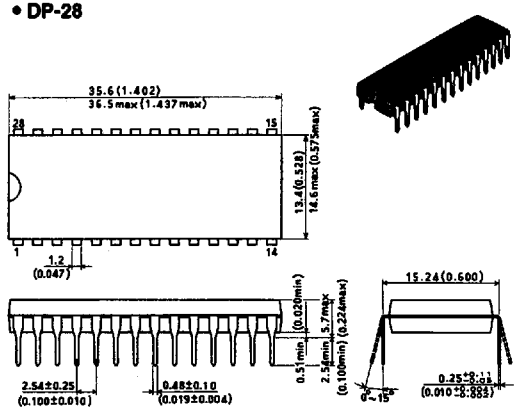
• DP-24A



• DP-24N



• DP-28



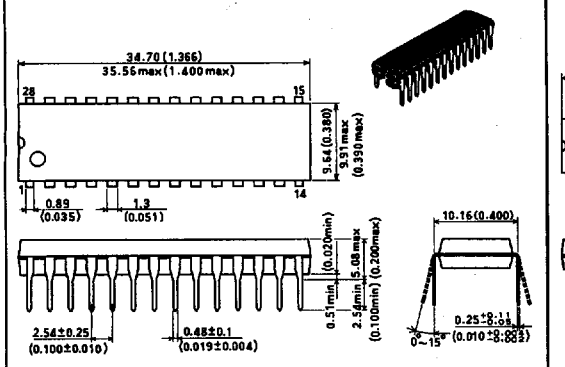
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

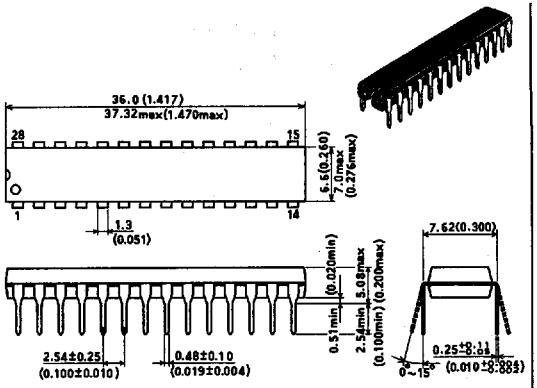
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

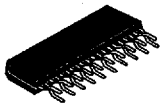


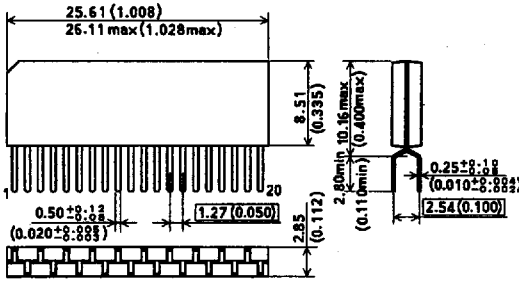
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

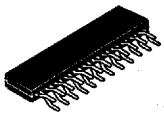
T-90-20

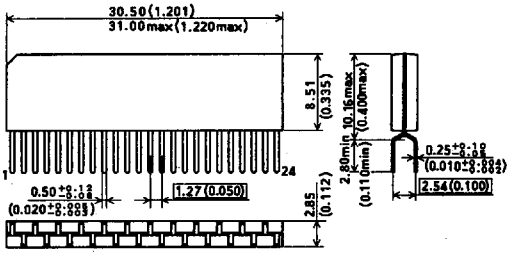
• ZP-20



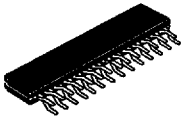


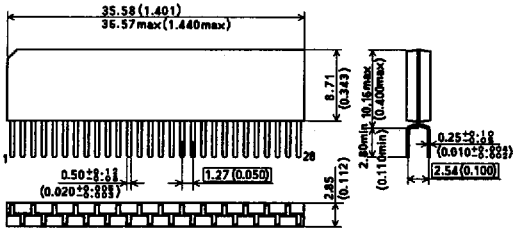
• ZP-24



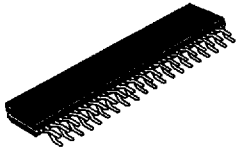


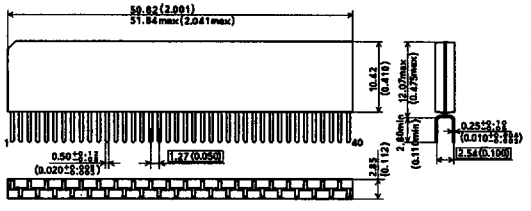
• ZP-28





• ZP-40

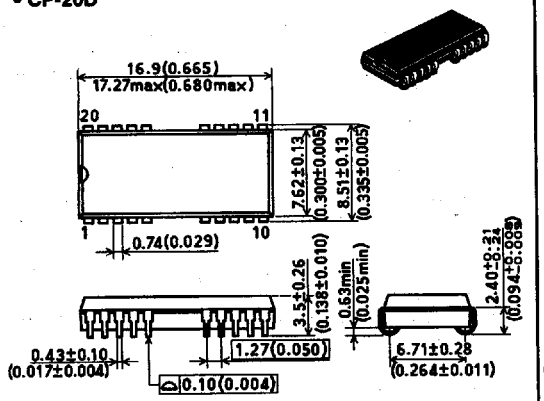




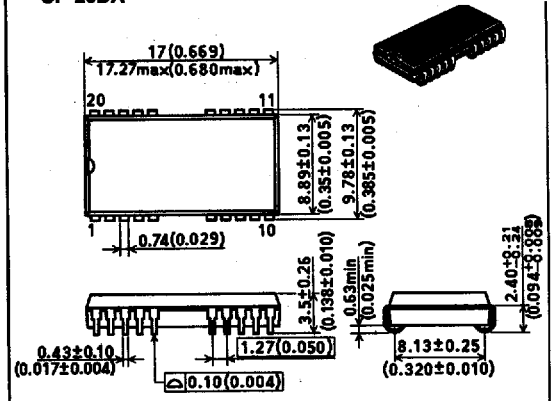
• Flat Package (J-bend Leads) HITACHI/ LOGIC/ARRAYS/MEM Unit: mm (inch) Scale 3/2

T-90-20

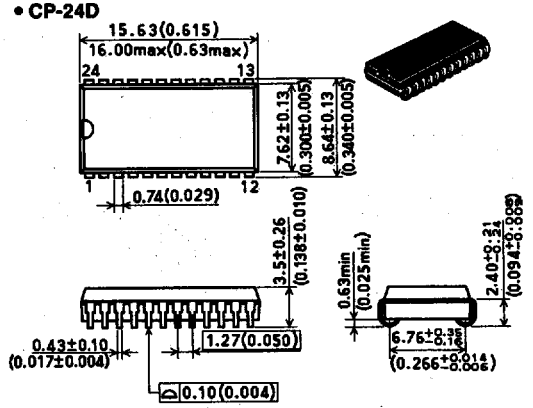
• CP-20D



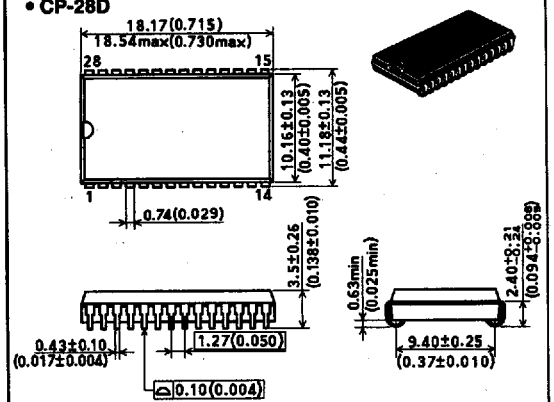
• CP-20DA



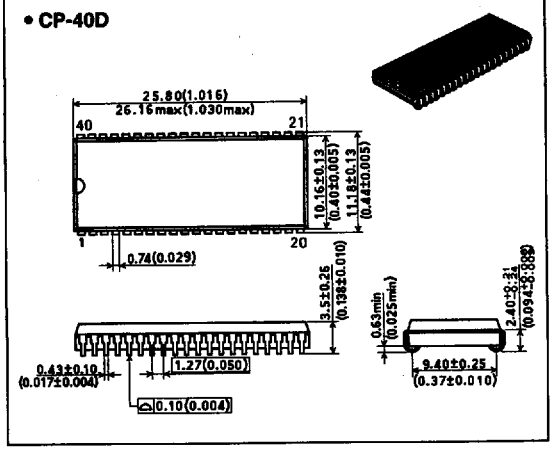
• CP-24D



• CP-28D



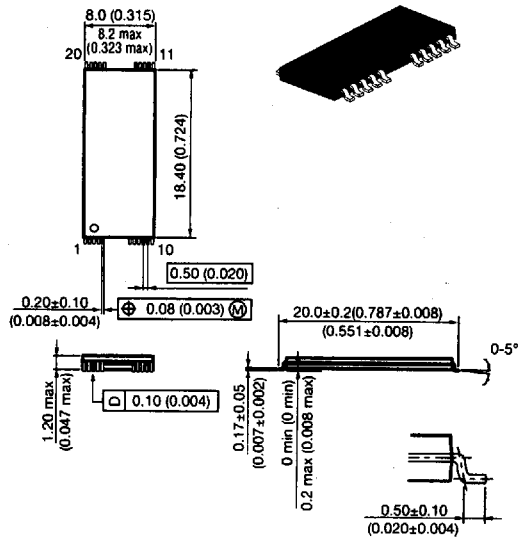
• CP-40D



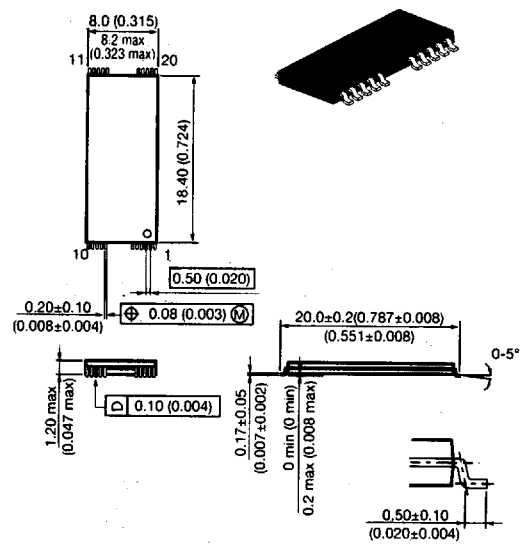
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

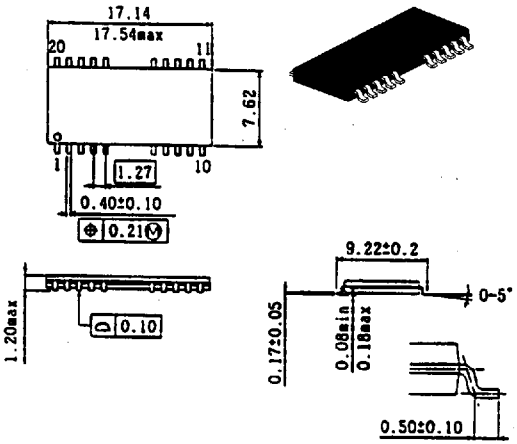
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR