HB56G19 Series

1,048,576-Word x 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56G19 is a 1M x 9 dynamic RAM module, mounted two 4 Mbit DRAM (HM514400AS) sealed in SOJ package and 1 Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56G19 is 30-pin single in-line package having lead types (HB56G19A), socket type (HB56G19B/GB). Therefore, the HB56G19 makes high density mounting possible without surface mount technology. The HB56G19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

■ FEATURES

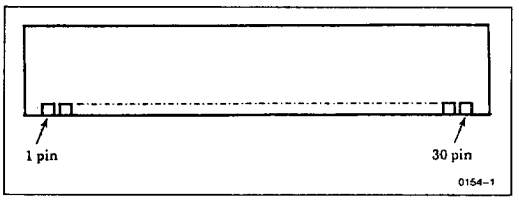
- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 1705 mW/1540 mW/1375 mW/1210 mW (max)
  - Standby Mode ..... 33 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56G19A-6A	60 ns	30-pin SIP Low Profile Lead Type
HB56G19A-7A	70 ns	
HB56G19A-8A	80 ns	
HB56G19A-10A	100 ns	
HB56G19B/GB-6A	60 ns	30-pin SIP Socket Type
HB56G19B/GB-7A	70 ns	
HB56G19B/GB-8A	80 ns	
HB56G19B/GB-10A	100 ns	

Note: Following the specification of the contact pads.
HB56G19B-XX :solder
HB56G19GB-XX :gold

■ PIN OUT

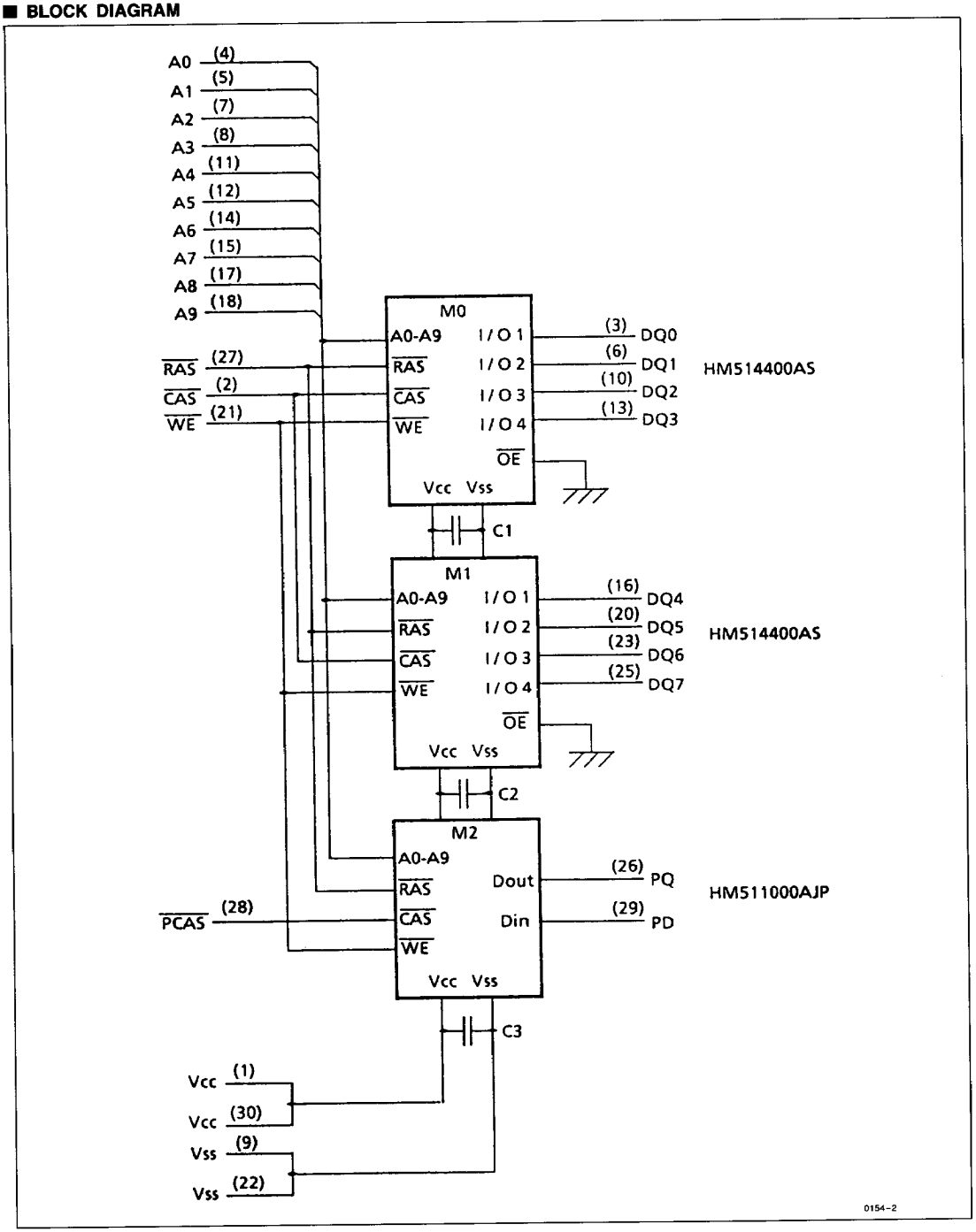


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

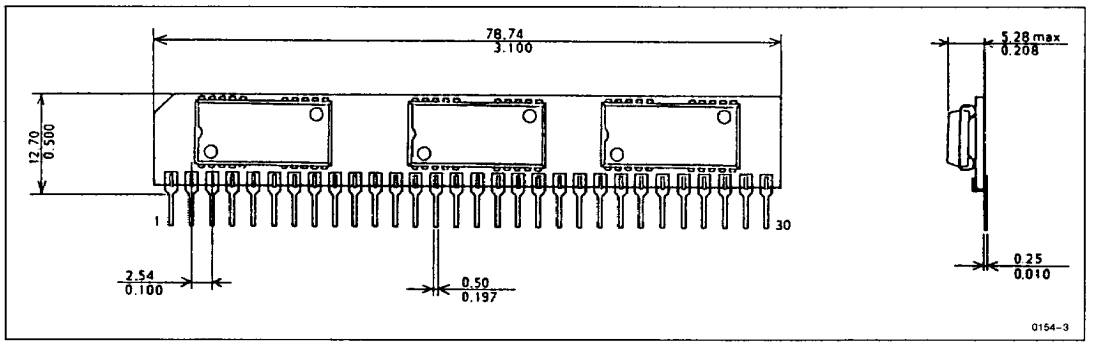
■ BLOCK DIAGRAM



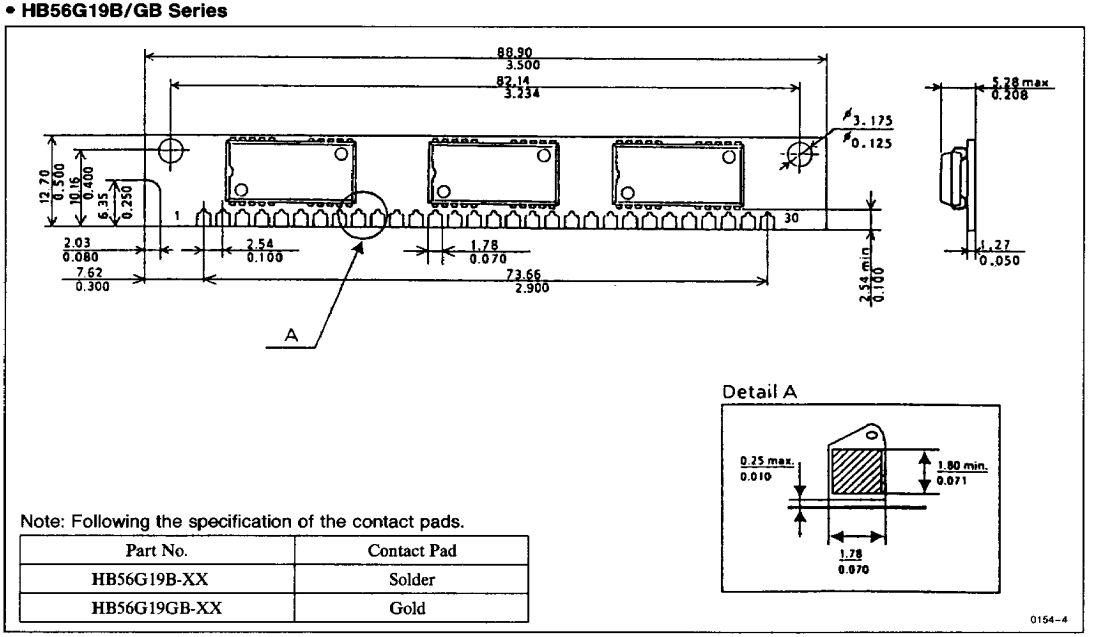
■ PHYSICAL OUTLINE

Unit: mm / inch

• **HB56G19A Series**



• **HB56G19B/GB Series**



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56G19B-XX	Solder
HB56G19GB-XX	Gold

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56G19A/B/GB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	310	—	280	—	250	—	220	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	6	—	6	—	6	—	6	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	3	—	3	—	3	—	3	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	310	—	280	—	240	—	210	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	15	—	15	—	15	—	15	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	300	—	270	—	240	—	210	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	300	—	270	—	230	—	210	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	30	pF	1
Input Capacitance (Clock)	C_{I2}	—	36	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12]

Read, Write, and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	20	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

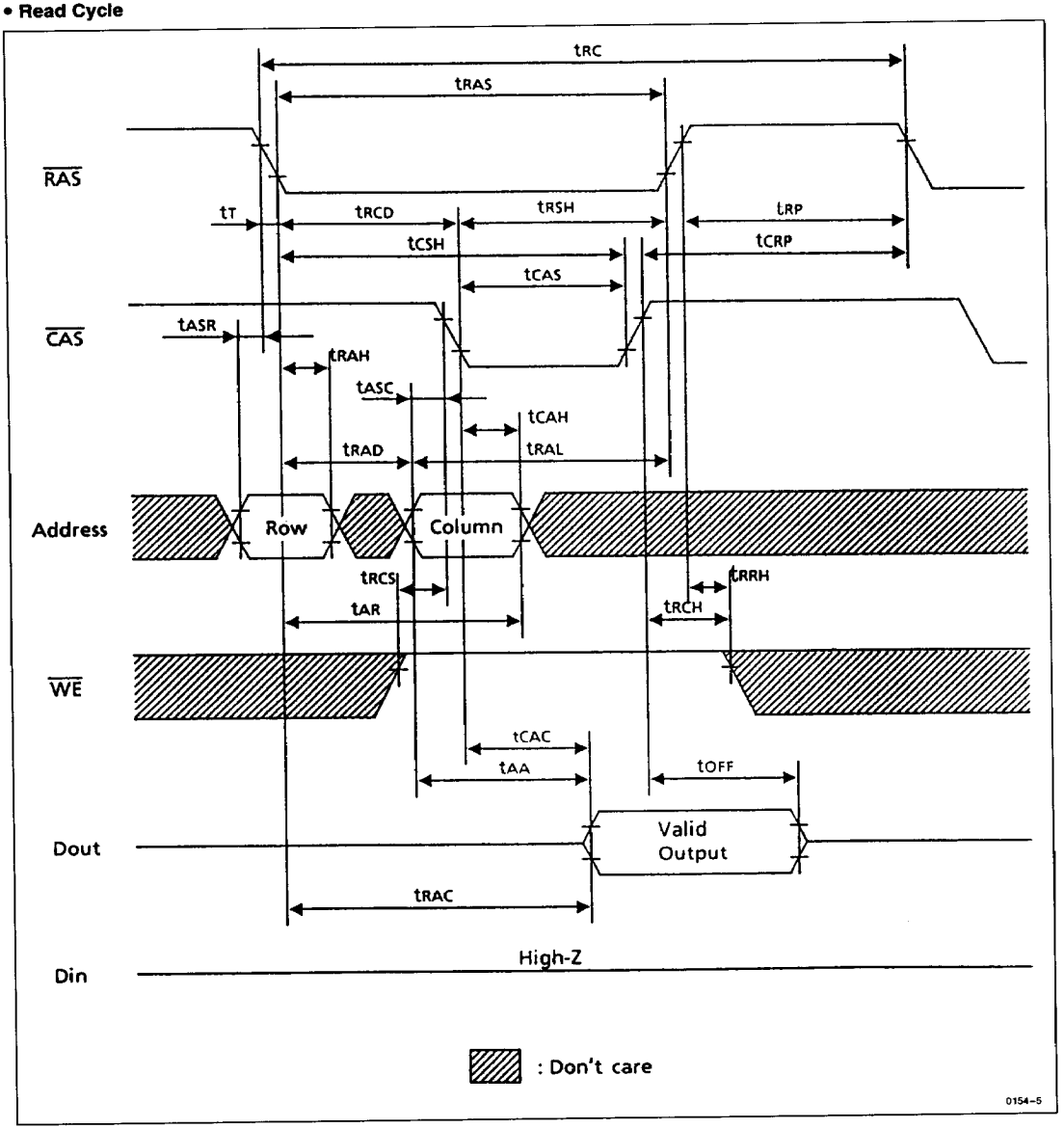
Fast Page Mode Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	60	100000	70	100000	80	100000	100	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	ns	

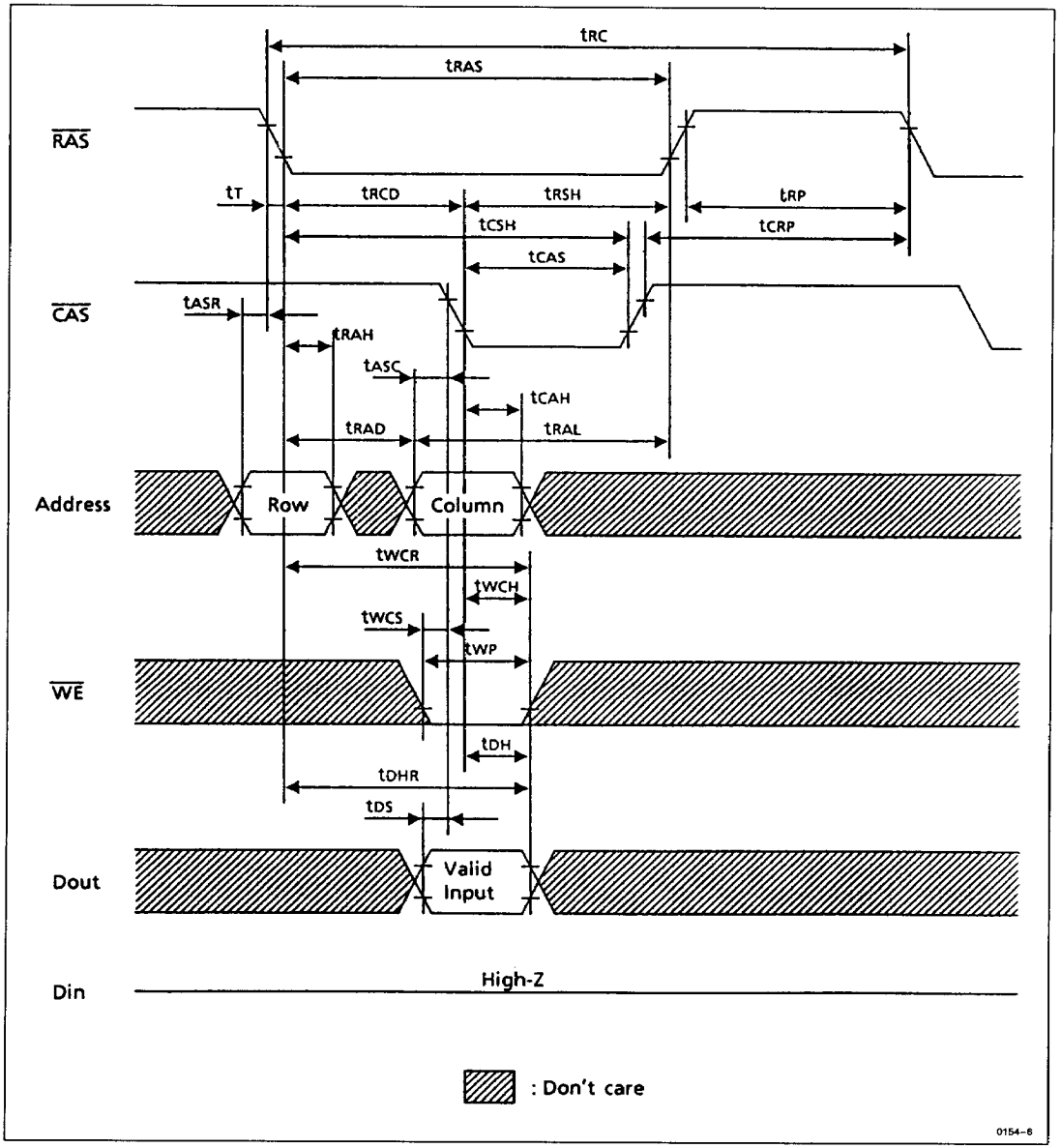
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

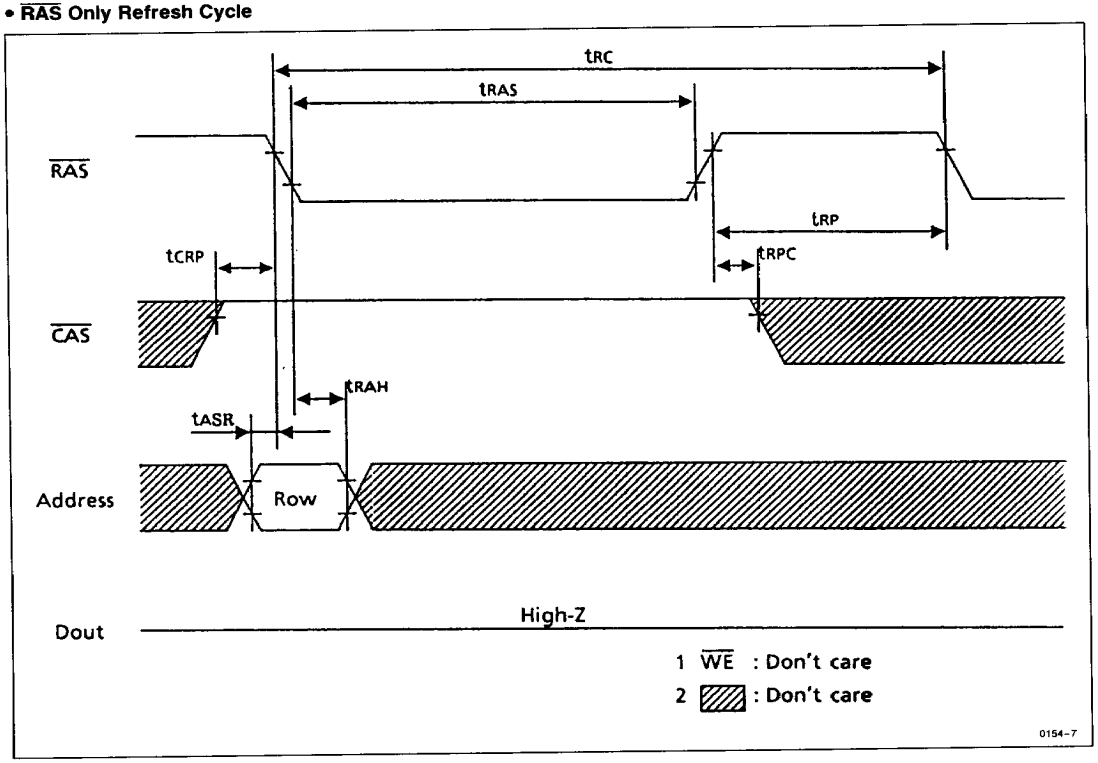
• Read Cycle



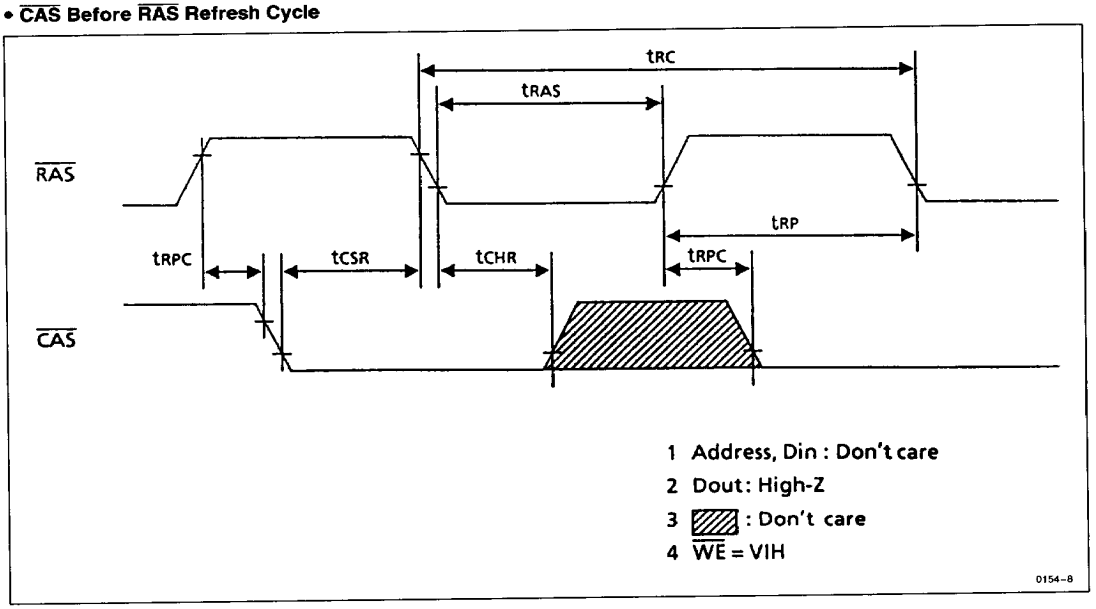
• **Early Write Cycle**



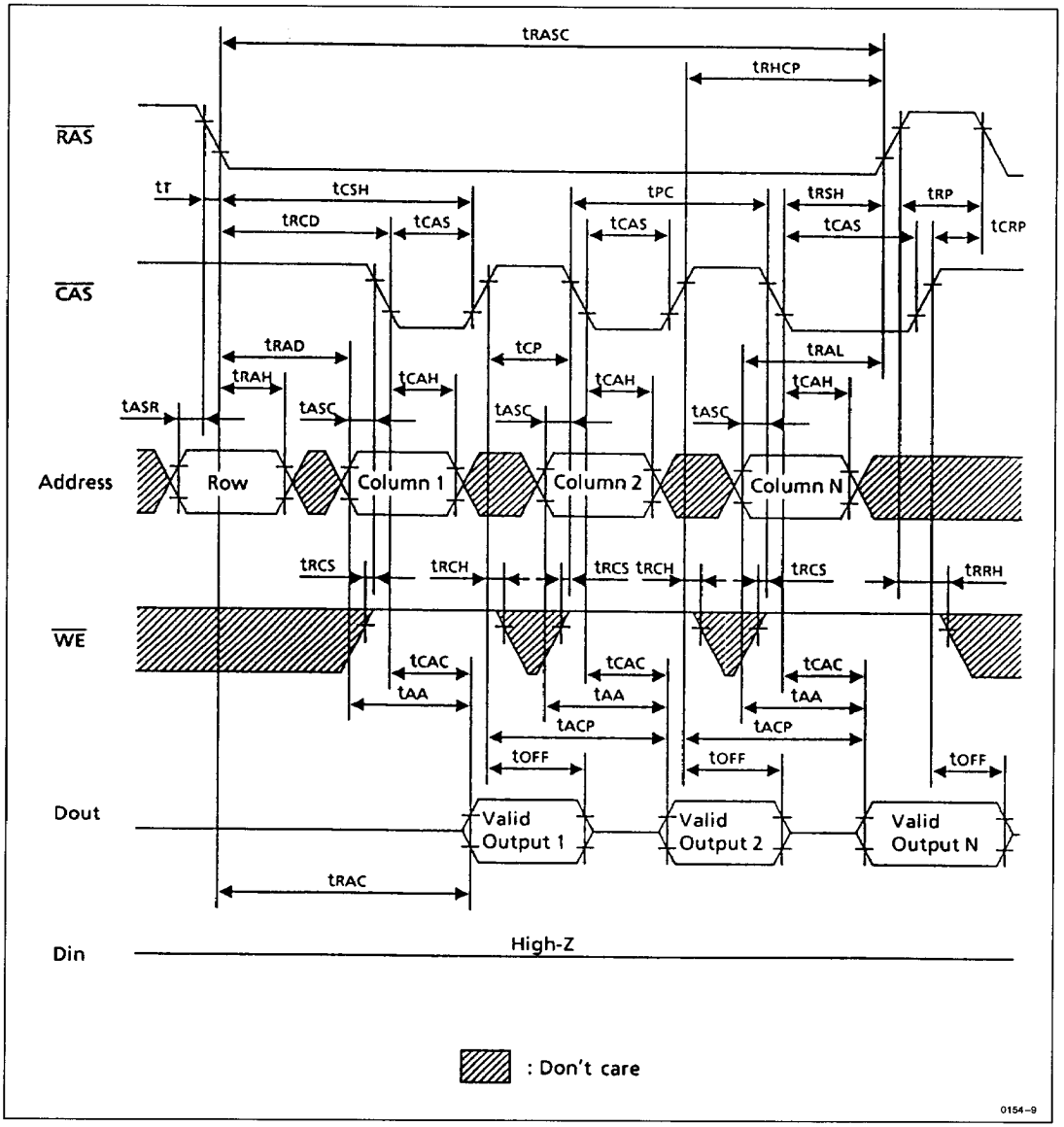
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**