HC2010 / HC2012

NSP FAMILY

HUGHES

SEMICONDUCTOR PRODUCTS CENTER

NONVOLATILE SERIALLY PROGRAMMABLE SOLID STATE TRIM POTENTIOMETERS

DESCRIPTION

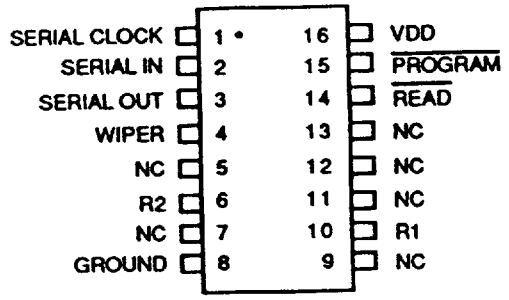
The Hughes HC2010 / HC2012 are 100% electronic potentiometers. They are implemented using an eight stage R - 2R ladder circuit. The wiper terminal setting is stored in nonvolatile latches. The output resolution is 0.4% of the voltage applied between pins R1 and R2 .

Nonvolatile data latches retain the last programmed state when power is removed. The correct state is automatically restored when power is reapplied. A standard serial interface, common to all the NSP devices, is used to access the nonvolatile memory.

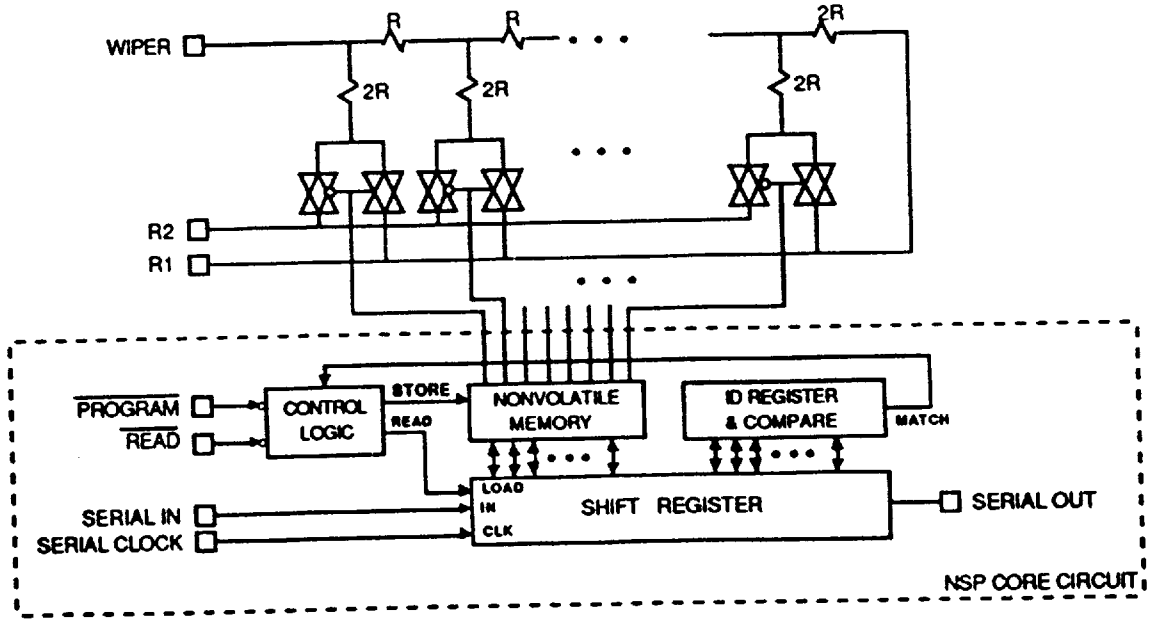
FEATURES

- CMOS
- Wide Supply Range (3 to 10 volts)
- Standard "NSP" Serial Interface
- R - 2R Ladder Configuration
- 0.4 % Resolution
- HC2010 (R≈1K) / HC2012 (R≈100K)
- Nonvolatile Data Latches

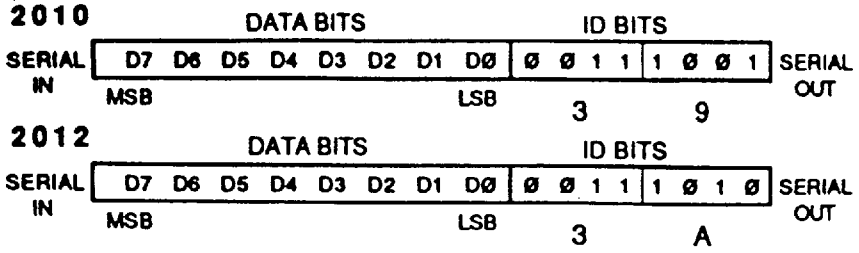
PIN CONFIGURATION



BLOCK DIAGRAM



SERIAL INTERFACE BIT ALLOCATION



DETAIL DESCRIPTION

The potentiometer function is provided by an eight stage R-2R ladder circuit. This circuit allows the voltage at the wiper pin (Vwiper) to be linearly varied between the voltages applied to pins R1 and R2. The eight nonvolatile data bits provide 256 equal steps at the wiper pin. The voltage applied to pins R1 and R2 must be between the device power supplies (Vdd and ground), but are not otherwise restricted in polarity.

The eight data bits form a binary number with DØ being the least significant bit. When all the data bits equal one (DATA=255), Vwiper=Vr1. As the value of DATA decreases, Vwiper moves from the voltage at Pin R1 towards the voltage at pin R2. When DATA reaches its minimum value of Ø , Vwiper is one step (Vr1-Vr2)/(256) from the voltage at Pin R2.

The HC2010 and HC2012 devices differ in their impedance values. The typical value of R for the HC2010 is 1KΩ and for the HC2012 is 100KΩ. The HC2010 is designed to have a lower temperature coefficient.

Resolution = 0.4% of Vdelta

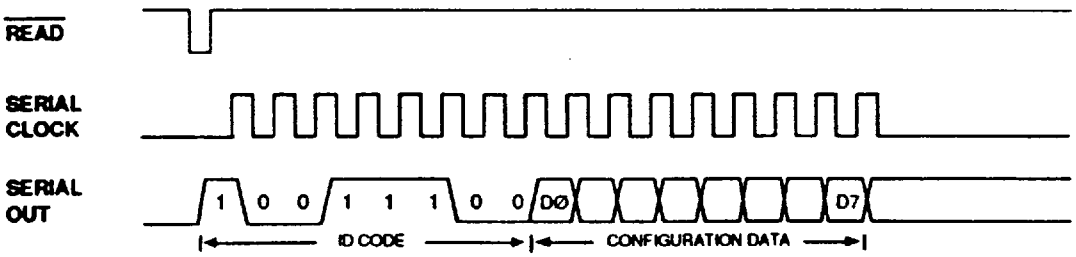
Range = 99.6 % of Vdelta

$$Vwiper = Vr2 + \frac{(DATA + 1) \cdot Vdelta}{256}$$

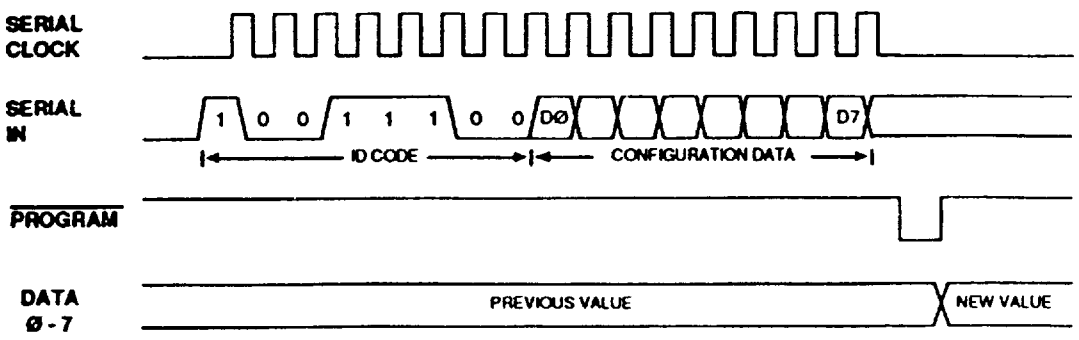
Note: Vdelta = (Vr1 - Vr2)

DATA	Vwiper
Ø	Vr2 + 1/256 Vdelta
1	Vr2 + 2/256 Vdelta
2	Vr2 + 3/256 Vdelta
:	
255	(Vr2 + Vdelta) or Vr1

TYPICAL READ TIMING



TYPICAL WRITE TIMING



ABSOLUTE MAXIMUM RATINGS

VDD.....-.3 TO +12V
Inputs (All).....+VSS -.3V to +VDD + .3V
Operating Temperature
Plastic Package.....-40 to + 85° C
Ceramic Package.....-55 to + 125° C
Storage Temperature.....-65 to + 150° C

Note: Specifications for the Military Temperature Range are available upon request.

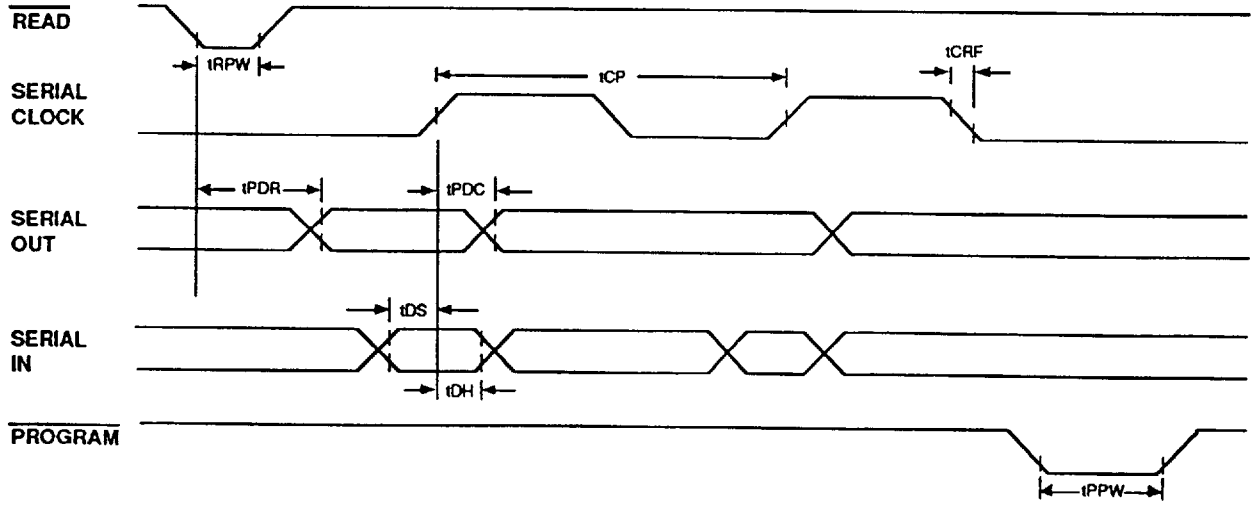
NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at VDD = 5V

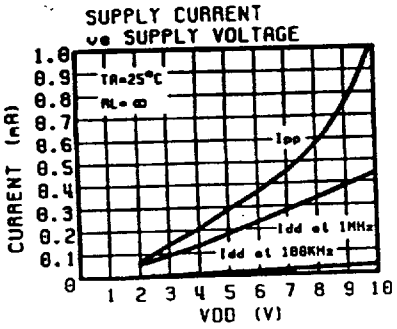
PARAMETER	SYMBOL	CONDITION	-40° C		25° C			85° C		UNITS
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Operating Voltage	VDD		3	10	3	-	10	3	10	V
Quiescent Current	IQ	$\overline{Prog}$, $\overline{Read}$=VDD	-	10	-	< 0.1	10	-	10	µA
Dynamic Current (1)	Idd	CLOCK Freq = 1MHz	-	250	-	175	250	-	250	µA
Programming Current	Ipp	$\overline{Prog}$ = 0 V	-	1	-	0.3	0.5	-	0.25	mA
Pull Up Resistance (2)	Rint		10	50	15	35	75	20	100	KΩ
Input High Level	Vih		3.5	-	3.5	2.75	-	3.5	-	V
Input Low Level	Vil		-	1.5	-	2.25	1.5	-	1.5	V
Input Leakage Current	IL	Vin = 2.5V	-	1	-	< 0.001	1	-	1	µA
Input Capacitance	Ci		-	-	-	5	-	-	-	pF
Output High Level	Voh	Iin = 1 mA	4.80	-	4.70	4.85	-	4.60	-	V
Output Low Level	Vol	Iin = 1 mA		0.10		0.06	0.15	-	0.20	V
Clock Rate	tCP	50% Duty Cycle	DC		DC	5	2	DC	1	MHz
Clock Rise/Fall Times	tCRF		-	1	-	-	1	-	1	µs
Data Set-up Time	tDS		15	-	20	10	-	25	-	ns
Data Hold Time	tDH		10	-	10	- 10	-	10	-	ns
Read Pulse Width	tRPW		75	-	100	20	-	125	-	ns
Program Pulse Width	tPPW		1	100	1	-	100	1	100	ms
Data Out Prop. Delay	tPDC	Cload = 50pF	-	115	-	85	150	-	200	ns
Data Out Prop. Delay	tPDR	Cload = 50pF	-	115	-	85	150	-	200	ns
Nonvolatile Endurance	NVE	tPPW = 10 ms	-	10^5	-	10^6	10^5	-	10^5	Cycles
Nonvolatile Retention	NVR	Temp ≤ 125°C	10	-	10	-	-	10	-	Years
NonLinearity 2010	NLin	RL = 10 MΩ	-	-	-	1.7	2.5	-	-	%FS
NonLinearity 2012	NLin	RL = 10 MΩ	-	-	-	1.4	2.0	-	-	%FS
Maximum Step Error 2010	MSE	RL = 10 MΩ	-	-	-	1	2	-	-	LSB
Maximum Step Error 2012	MSE	RL = 10 MΩ	-	-	-	0.5	1	-	-	LSB
Temperature Drift 2010	TD	Data = 80 (Hex)	-	-	-	-30	-50	-	-	ppm/°C
Temperature Drift 2012	TD	Data = 80 (Hex)	-	-	-	-15	-30	-	-	ppm/°C

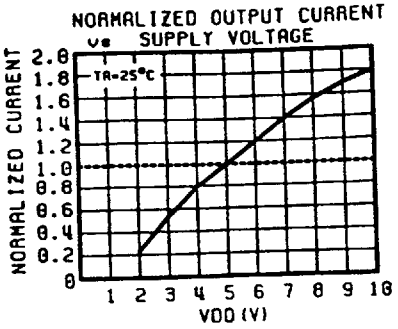
Note (1): $\overline{Read}$ and $\overline{Program}$ = VDD, Serial In = 0.5 MHz Square Wave, Serial Out Load = 10pF.
Note (2): $\overline{Read}$ and $\overline{Program}$ inputs

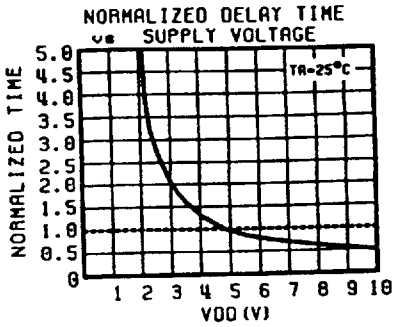
TIMING DIAGRAM

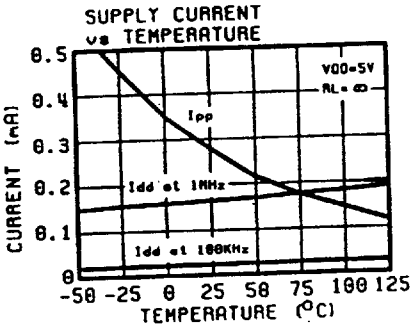


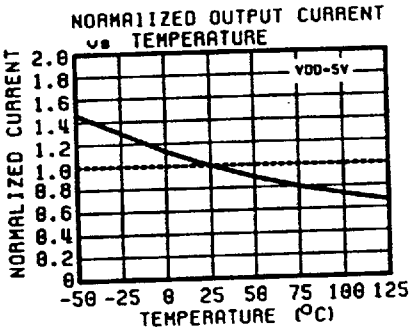
TYPICAL OPERATING CHARACTERISTICS

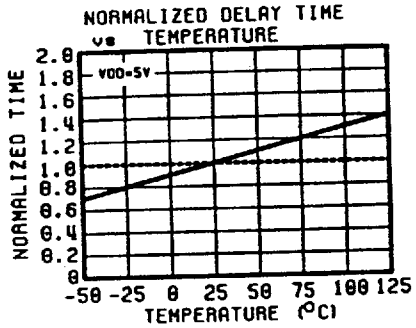


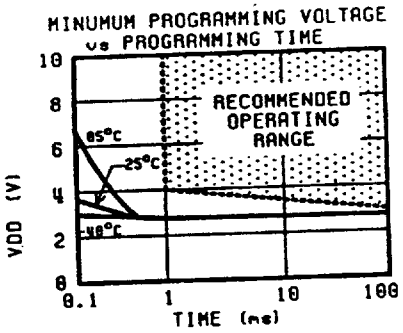


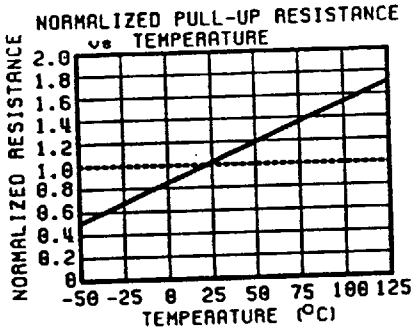


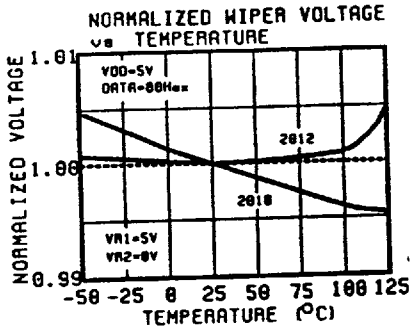






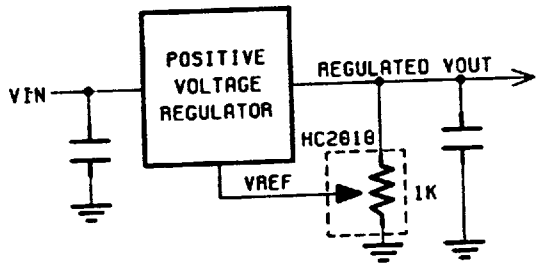




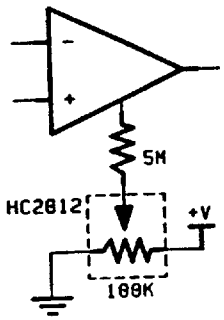


TYPICAL APPLICATIONS

ADJUSTABLE REGULATORS

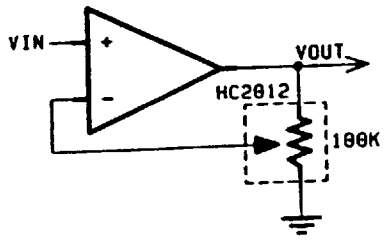


OFFSET ADJUST



ADJUSTABLE GAIN AMPLIFERS

NONINVERTING



INVERTING