HC2090 NSP FAMILY

HUGHES

SEMICONDUCTOR
PRODUCTS CENTER

NONVOLATILE SERIALLY PROGRAMMABLE
16 BIT DIVIDE BY N COUNTER

DESCRIPTION

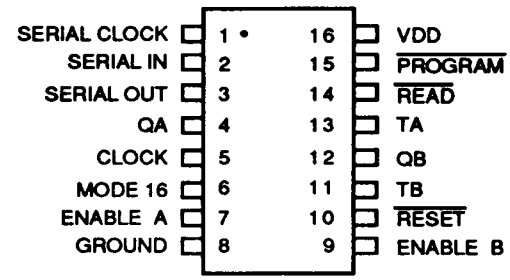
The Hughes HC2090 is a dual mode programmable clock divider. In the 16 bit mode it can divide the clock frequency by 1 to 2^{16}. In the 8 bit mode, two separately enabled sections can divide the clock by 1 to 2^{8}. The TA and TB are terminal count outputs. The QA and QB outputs are the terminal counts divided by 2 to provide a 50% duty cycle.

Nonvolatile data latches retain the last programmed state when power is removed. The correct state is automatically restored when power is reapplied. A standard serial interface, common to all the NSP devices, is used to access the nonvolatile memory.

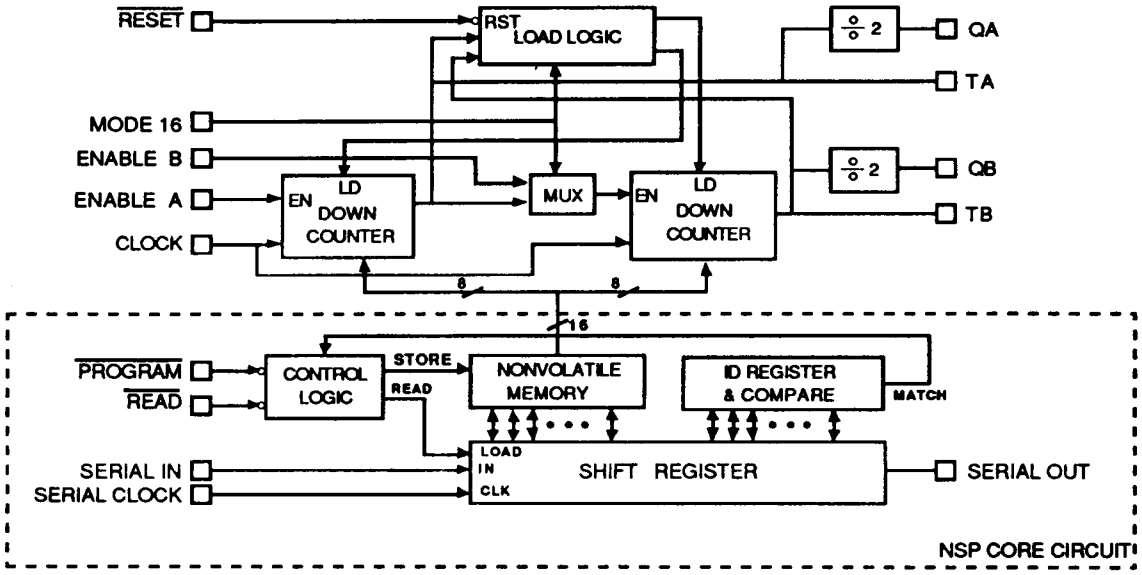
FEATURES

- CMOS
- Wide Supply Range (3 to 10 volts)
- Standard "NSP" Serial Interface
- 16 Bit Mode or Dual 8 Bit Mode
- Separate Enables
- Strobe and Clocked Output
- Fully Synchronous Operation
- Nonvolatile Data Latches

PIN CONFIGURATION



BLOCK DIAGRAM



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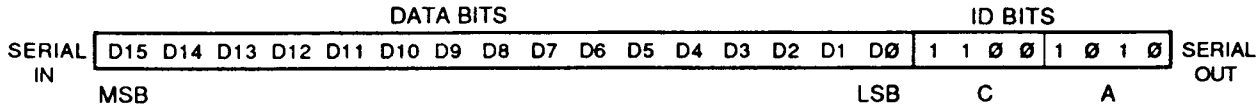
SERIAL INTERFACE BIT ALLOCATION



DETAIL DESCRIPTION

The ID code and configuration data are read on the SERIAL OUT pin by pulsing READ low and then clocking the SERIAL CLOCK pin. New data is written into the NV memory by first entering the correct ID code and data into the shift register using the SERIAL IN and SERIAL CLOCK inputs; and then pulsing PROGRAM low for at least 1 ms. The new data replaces the previous data on the rising edge of PROGRAM. Both the READ and PROGRAM inputs have internal pull-up resistors.

The HC2090 programmable counter has two modes of operation. When the MODE16 input is high, the device operates as a 16 bit programmable counter. When MODE16 is low, it is configured as two independent 8 bit programmable counters that share common clock and reset inputs. All inputs are synchronous.

When operated in the 16 bit mode, the input clock frequency is divided by (N+1), where N is the number programmed in the nonvolatile (NV) memory. The division is accomplished by loading a down counter with the value stored in the NV memory and then decrementing the counter until its value equals zero. On the next rising edge of the clock pulse, the counter is again loaded with the NV memory value. In this mode, the ENABLE A input gates the clock. When ENABLE A is a logic "1", the counter is decremented on the rising edge of the clock. If ENABLE A is held low, the clock is disabled, freezing the state of the counter. A synchronous reset is provided. If the RESET input is active (low), the value stored in the NV memory is loaded into the counter on the rising edge of the clock. After reseting the counter, (N+1) clocks are required to toggle the QB output. An internal pull-up resistor holds RESET inactive unless it is externally driven low. Only the TB and QB outputs are used in the 16 bit mode. The terminal count output (TB) pulses high for one clock cycle at the completion of each counter cycle. This output allows devices to be easily cascaded. For example, a 32 bit programmable counter can be realized by connecting the TB output of one device to the ENABLE A input of a second HC2090 device. The terminal count signal should only be used to enable action on a clock edge. * The other output available in the 16 bit mode is the QB output. It provides a 50% duty cycle output by dividing the TB output by 2.

In the dual 8 bit mode, the 16 bit counter is reconfigured to provide two 8 bit counters. Each 8 bit counter has separate clock enable (ENABLE A and ENABLE B) and separate outputs (TA, QA and TB, QB). They share common CLOCK and RESET inputs. Each counter functions similarly to the 16 bit counter described above.

OUTPUT	OUTPUT FREQUENCY		
	MODE 16 = Ø DUAL 8 BIT	MODE 16 = 1 16 BIT	
TA	Fclk / (M+1)	Not Used	M = D15 thru D8 D8 = LSB
QA	Fclk / 2(M+1)	Not Used	
TB	Fclk / (L+1)	Fclk/(N+1)	L = D7 thru DØ DØ = LSB
QB	Fclk / 2(L+1)	Fclk/2(N+1)	N = D15 thru DØ DØ = LSB

*** Design Note**
The terminal count outputs are created with ripple circuitry and may become invalid briefly after the rising edge of the clock. If these outputs are used as clocks or as inputs to static logic, they should be sampled or strobed to eliminate false terminal count pulses.

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