

**COS/MOS
INTEGRATED
CIRCUITS**

7929225 S G S SEMICONDUCTOR CORP

T-45-23-29

DECADE COUNTERS/DIVIDERS**WITH DECODED 7-SEGMENT DISPLAY OUTPUTS AND: DISPLAY ENABLE 4026B
RIPPLE BLANKING 4033B**

- COUNTER AND 7-SEGMENT DECODING IN ONE PACKAGE
- EASILY INTERFACED WITH 7-SEGMENT DISPLAY TYPES
- FULLY STATIC COUNTER OPERATION: DC TO 6 MHz (TYP.) AT $V_{DD} = 10V$
- IDEAL FOR LOW-POWER DISPLAYS
- DISPLAY ENABLE OUTPUT -4026B
- "RIPPLE BLANKING" AND LAMP TEST - 4033B
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4026B/4033B** (extended temperature range) and **HCF 4026B/4033B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4026B** and **HCC/HCF 4033B** each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display. These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important. Inputs common to both types are **CLOCK**, **RESET**, & **CLOCK INHIBIT**; common outputs are **CARRY OUT** and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the **HCC/HCF 4026B** include **DISPLAY ENABLE** input and **DISPLAY ENABLE** and **UNGATED "C-SEGMENT"** outputs. Signals peculiar to the **HCC/HCF 4033B** are **RIPPLE-BLANKING INPUT** AND **LAMP TEST INPUT** and a **RIPPLE-BLANKING OUTPUT**. A high **RESET** signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the **CLOCK INHIBIT** signal is low. Counter advancement via the clock line is inhibited when the **CLOCK INHIBIT** signal is high. Antilock gating is provided on the **JOHNSON** counter, thus assuring proper counting sequence. The **CARRY-OUT** (C_{out}) signal completes one cycle every ten **CLOCK INPUT** cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the **HCC/HCF 4033B**; in the **HCC/HCF 4026B** these outputs go high only when the **DISPLAY ENABLE IN** is high.

HCC/HCF 4026B - When the **DISPLAY ENABLE IN** is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing. The **CARRY OUT** and **UNGATED "C-SEGMENT"** signals are not gated by the **DISPLAY ENABLE** and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

HCC/HCF 4033B - The **HCC/HCF 4033B** has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the **RBI** terminal of the **HCC/HCF 4033B** associated with the most significant digit in the display to a low-level voltage and connecting the **RBO** terminal of that stage to the **RBI** terminal of the **HCC/HCF 4033B** in the next-lower significant position in the display. This procedure is continued for each succeeding **HCC/HCF 4033B** on the integer side of the display. On the fraction side of the display the **RBI** of the **HCC/HCF 4033B** associated with the least significant bit is connected to a low-level voltage and the **RBO** of that **HCC/HCF 4033B** is connected to the **RBI** terminal of the **HCC/HCF 4033B** in the next more-significant-bit position. Again, this procedure is continued for all **HCC/HCF 4033B**'s on the fraction side of the display. In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the **RBI** of that stage to a high level voltage (instead of to the **RBO** of the next more-significant-stage). For example: optional zero $\rightarrow$ 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the **RBI** of the **HCC/HCF 4033B** associated with it to a high-level voltage. Ripple blanking of non-significant zeros provides an appreciable savings in display power. The **HCC/HCF 4033B** has a **LAMP TEST** input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.



HCC/HCF 4026B
HCC/HCF 4033B

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ABSOLUTE MAXIMUM RATINGS

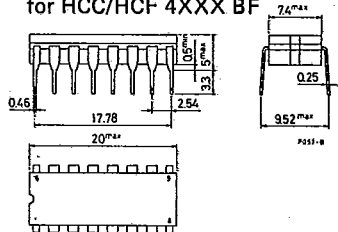
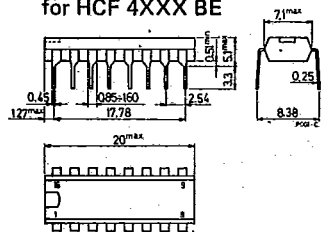
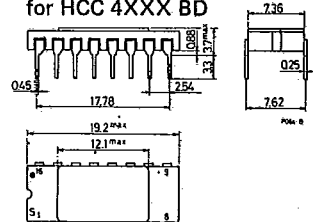
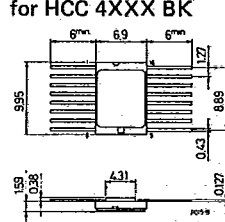
V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20 -0.5 to 18	V V
V_I	Input voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for T_{op} = full package-temperature range	200 100	mW mW
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 -40 to 85	°C °C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HCC/HCF 4XXX BFDual in-line plastic package
for HCF 4XXX BEDual in-line ceramic package
for HCC 4XXX BDCeramic flat package
for HCC 4XXX BK

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: HCC types HCF types	3 to 18 3 to 15	V V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 -40 to 85	°C °C

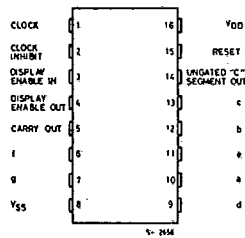


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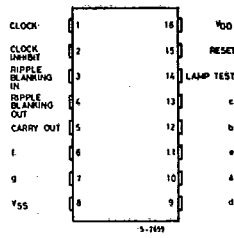
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CONNECTION DIAGRAMS

for 4026B

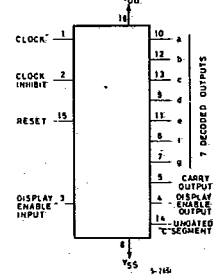


for 4033B

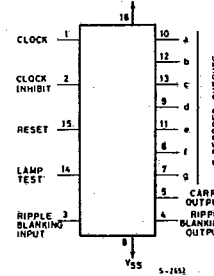


FUNCTIONAL DIAGRAMS

for 4026B

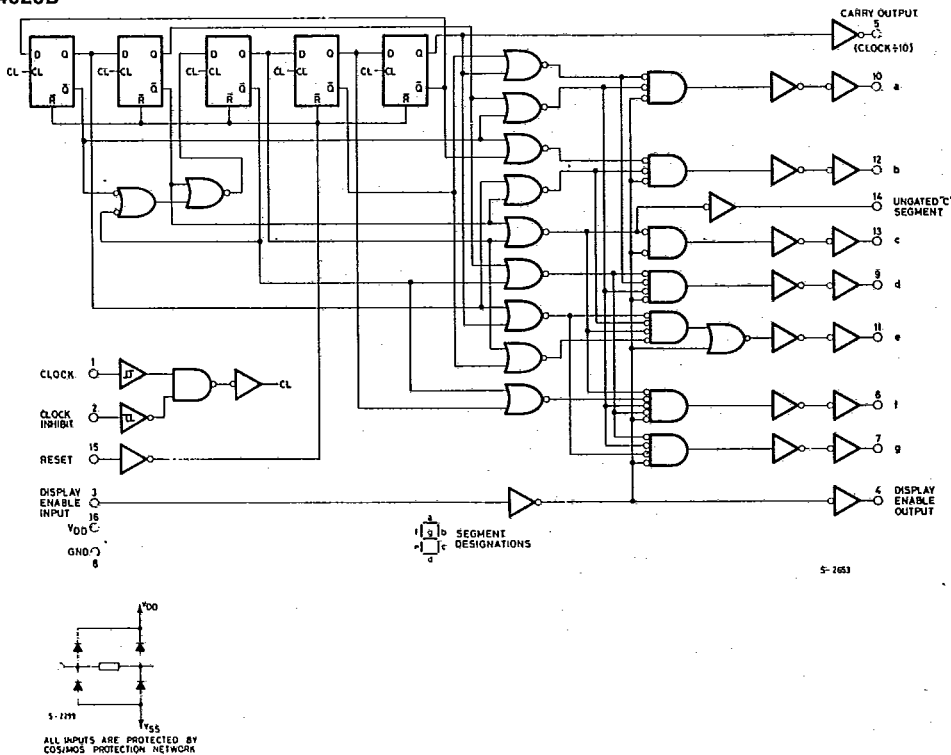


for 4033B

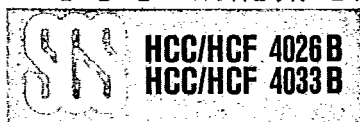


LOGIC DIAGRAMS

for 4026B



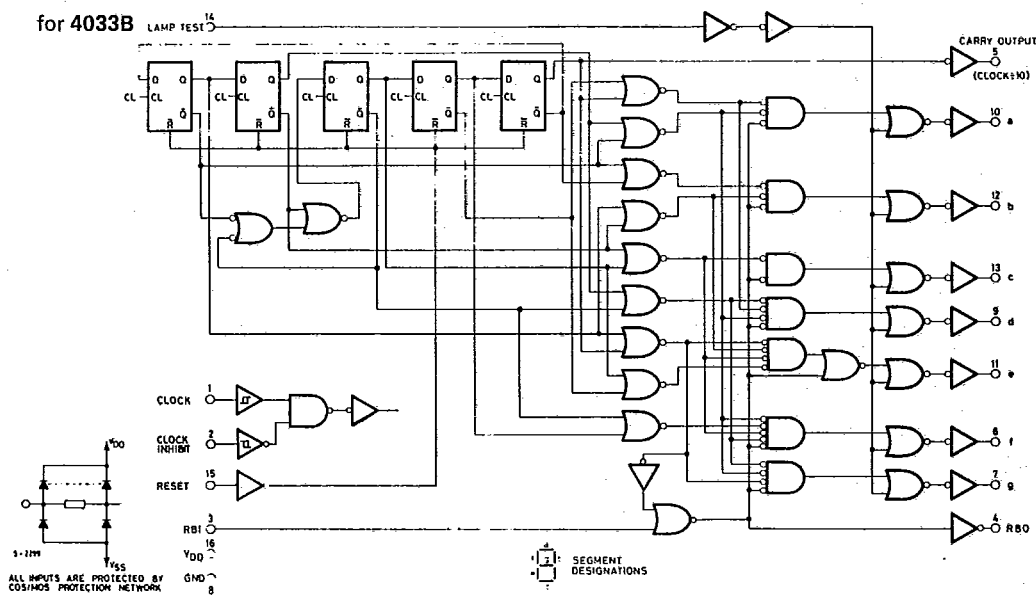
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LOGIC DIAGRAMS (continued)

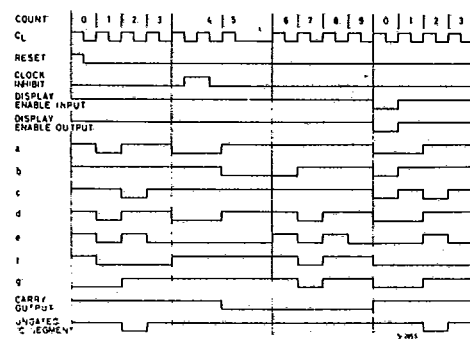
for 4033B



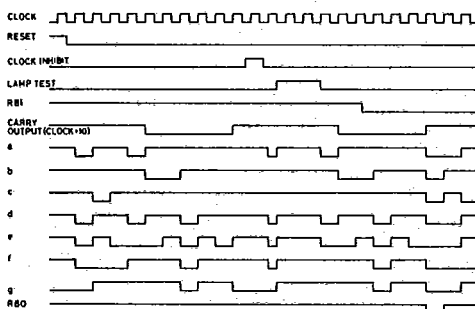
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TIMING DIAGRAMS

for 4026B



for 4033B



0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2

5-2654



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STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values						Unit	
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V _{OH}	Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95			V
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage	5/0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15	mA	
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		±10 ⁻⁵	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		±10 ⁻⁵	±0.3		± 1	
C _I	Input capacitance			Any input					5	7.5			pF	

* T_{Low} = - 55°C for HCC device; -40°C for HCF device.* T_{High} = +125°C for HCC device; +85°C for HCF device.The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V



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DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^{\circ}\text{C}$, all input rise and all fall times = 20 ns)

Parameter		Test conditions	Values			Unit	
			V _{DD} (V)	Min.	Typ.		Max.
CLOCKED OPERATION							
t _{PLH} , t _{PHL}	Propagation delay time Carry Out Line		5		250	500	ns
			10		100	200	
			15		75	150	
t _{PLH} , t _{PHL}	Propagation delay time Decode Out Lines		5		350	700	ns
			10		125	250	
			15		90	180	
t _{THL} , t _{TLH}	Transition time Carry Out Line		5		100	200	ns
			10		50	100	
			15		25	50	
f _{CL} *	Maximum clock input frequency		5	2.5	5		MHz
			10	5.5	11		
			15	8	16		
t _{WC}	Clock pulse width		5		110	270	ns
			10		50	100	
			15		40	80	
t _r , t _f	Clock input rise or fall time		5	Unlimited			μs
			10				
			15				
RESET OPERATION							
t _{PLH} , Carry Out Line	Propagation delay time Carry Out Line		5		275	550	ns
			10		120	240	
			15		80	160	
t _{PLH} , t _{PHL}	Propagation delay time Decode Out Lines		5		300	600	ns
			10		125	250	
			15		90	180	
t _{WR}	Rset pulse width		5		100	120	ns
			10		50	100	
			15		25	50	
t _{rem}	Reset removal time		5		0	30	ns
			10		0	15	
			15		0	10	

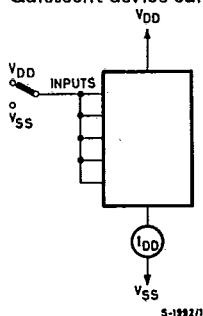
* Measured with respect to carry output line.



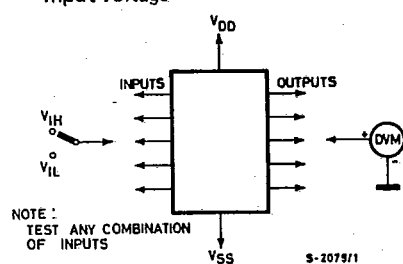
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TEST CIRCUITS

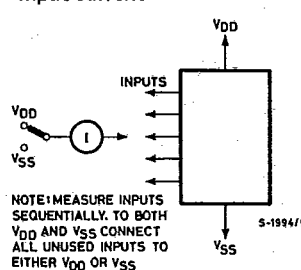
Quiescent device current



Input voltage

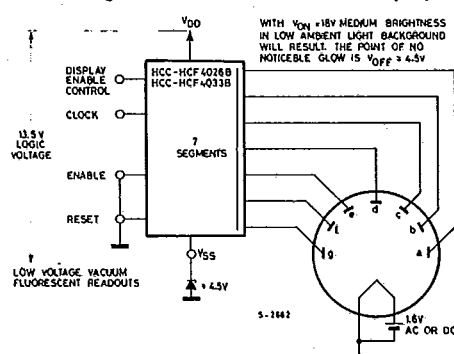


Input current

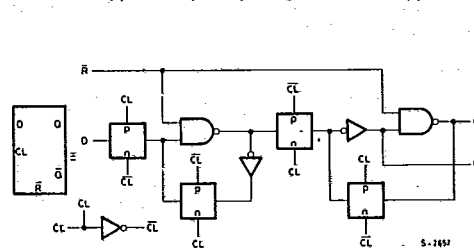


TYPICAL APPLICATIONS

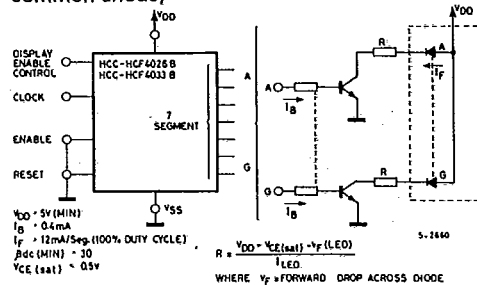
Interfacing with filament fluorescent display



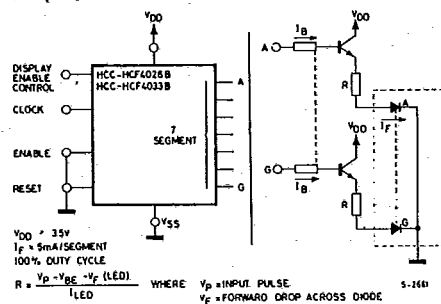
Detail of typical flip-flop stage for both types

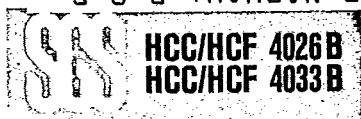


Interfacing with LED displays (display common anode)



(display common cathode)



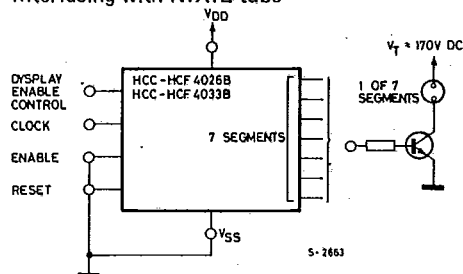


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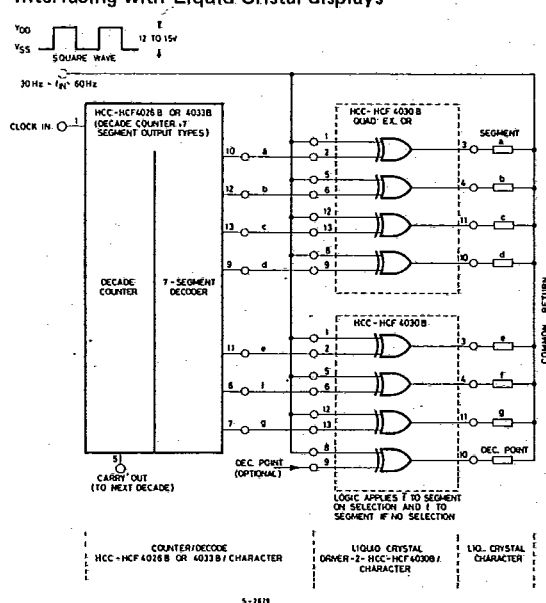
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TYPICAL APPLICATIONS (continued)

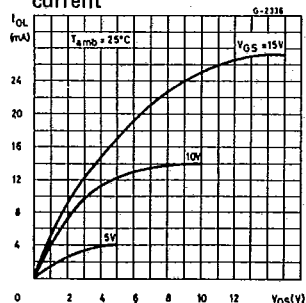
Interfacing with NIXIE tube



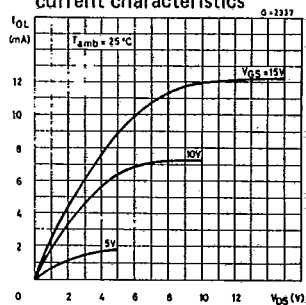
Interfacing with Liquid Crystal displays



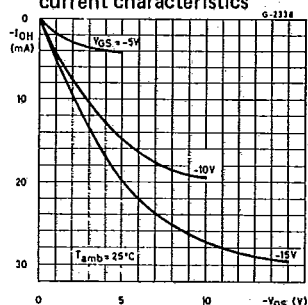
Typical output low (sink) current



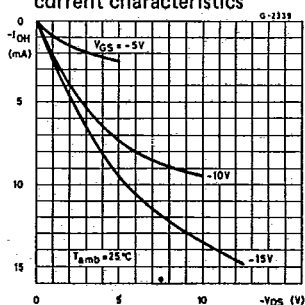
Minimum output low (sink) current characteristics

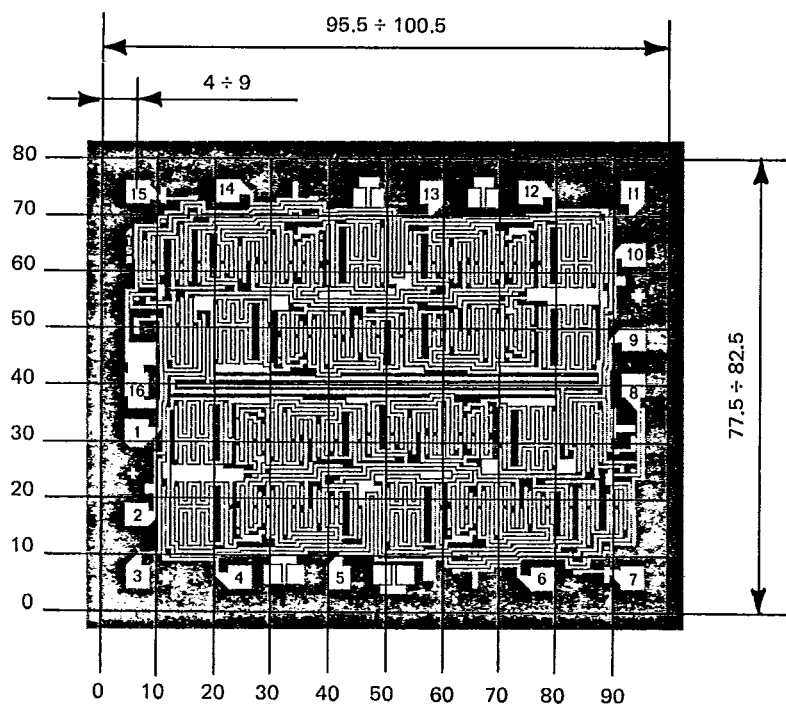


Typical output high (source) current characteristics

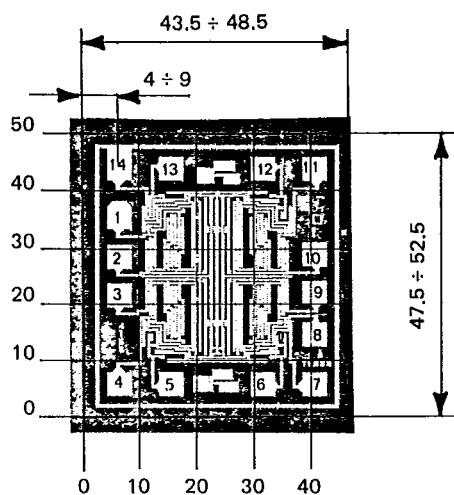


Minimum output high (source) current characteristics





4015B



4016B