CMOS/MOS INTEGRATED CIRCUIT

HCC/HCF 4048B

MULTIFUNCTION EXPANDABLE 8-INPUT GATE

- THREE-STATE OUTPUT
- MANY LOGIC FUNCTIONS AVAILABLE IN ONE PACKAGE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4048B** (extended temperature range) and **HCF 4048B** (intermediate temperature range) are monolithic integrated circuit,available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4048B** is an 8-input gate having four control inputs. Three binary control inputs - Ka, Kb, and Kc - provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input - Kd- provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one **HCC/HCF 4048B**. For example, two **HCC/HCF 4048B**'s can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

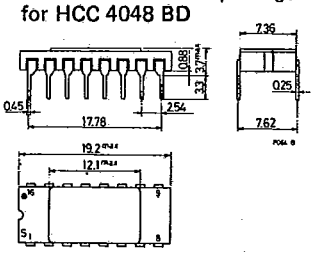
ORDERING NUMBERS:

HCC 4048 BD for dual in-line ceramic package
HCC 4048 BF for dual in-line ceramic package, frit seal
HCC 4048 BK for ceramic flat package
HCF 4048 BE for dual in-line plastic package
HCF 4048 BF for dual in-line ceramic package, frit seal

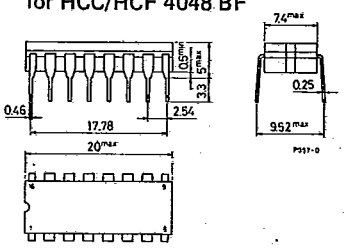
HCC/HCF 4048 B

MECHANICAL DATA (dimensions in mm)

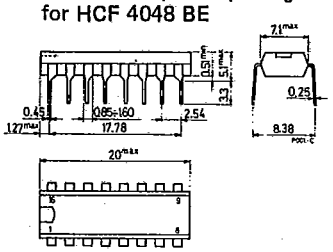
Dual in-line ceramic package for HCC 4048 BD



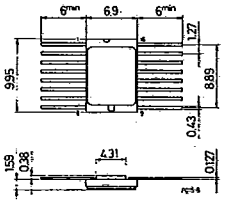
Dual in-line ceramic package for HCC/HCF 4048 BF



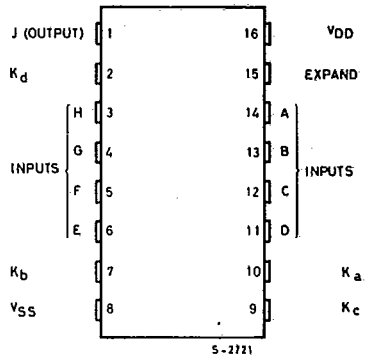
Dual in-line plastic package for HCF 4048 BE



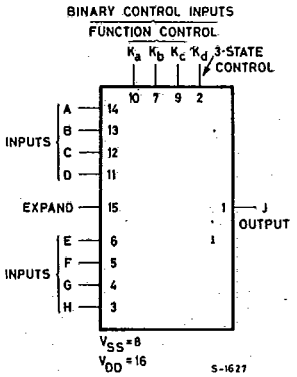
Ceramic flat package for HCC 4048 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

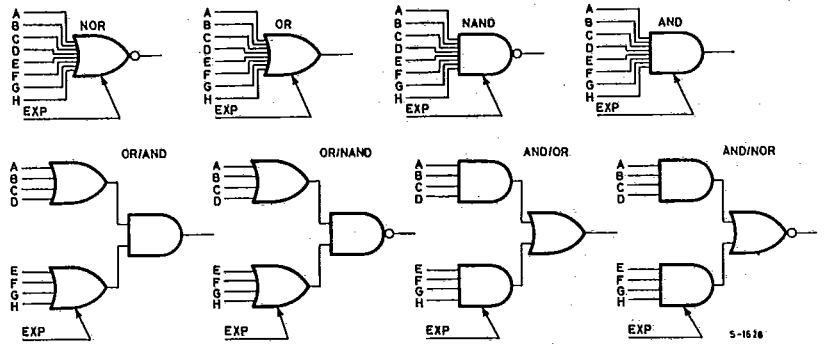


RECOMMENDED OPERATING CONDITIONS

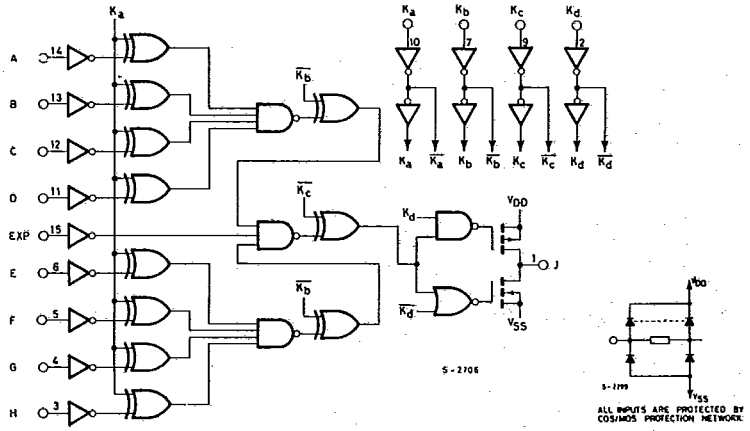
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

HCC/HCF 4048B

BASIC LOGIC CONFIGURATIONS



LOGIC DIAGRAM



FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}

$K_d=1$ Normal Inverter Action
$K_d=0$ High Impedance Output

EXPAND Input = 0

HCC/HCF 4048B

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

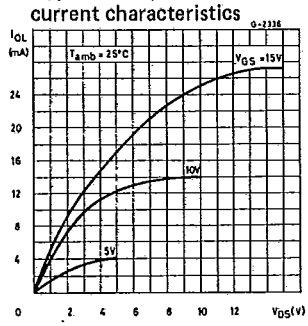
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent current	HCC types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		HCF types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$±10^{-5}$	±0.3		± 1	
I_{OH}	3-state output current	HCC types	0/18	0/18		18		±0.4		$±10^{-4}$	±0.4		±12	μA
		HCF types	0/15	0/15		15		±1.0		$±10^{-4}$	±1.0		±7.5	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = − 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

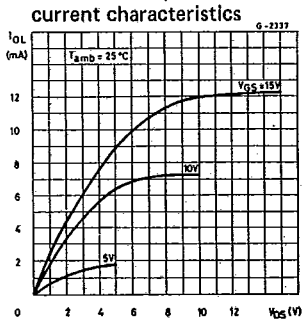
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values				Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time Inputs to output and Ka to Output		5		300	600	ns
			10		150	300	
			15		120	240	
	Kb to Output		5		225	450	
			10		85	170	
			15		55	110	
	Kc to Output		5		140	280	
			10		50	100	
			15		40	80	
	Expand Input to Output		5		190	380	
			10		90	180	
			15		65	130	
t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	3-state propagation delay time Kd to Output	R_L = 1 kΩ	5		80	160	
			10		35	70	
			15		25	50	
t_{THL}, t_{TLH}	Transition time		5		100	200	
			10		50	100	
			15		40	80	
3-state output capacitance					5	10	pF

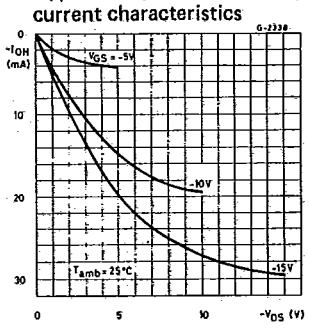
Typical output low (sink) current characteristics



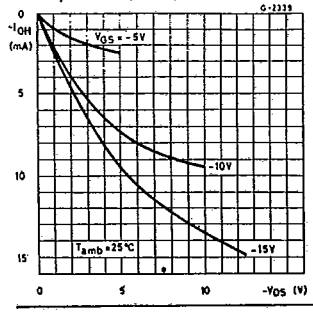
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

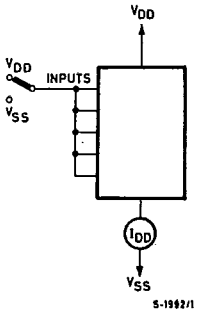


Minimum output high (source) current characteristics

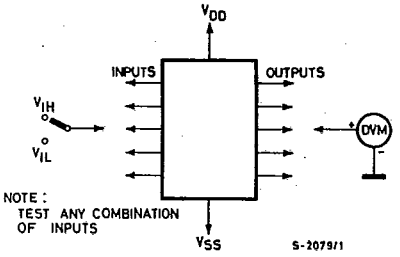


TEST CIRCUITS

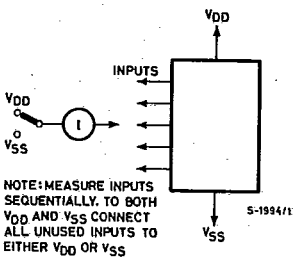
Quiescent device current



Input voltage

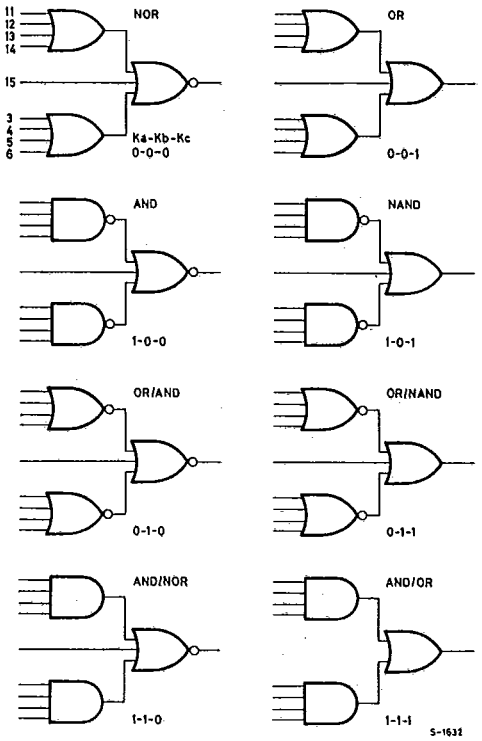


Input current



APPLICATIONS OF EXPAND INPUT

Actual-circuit logic configurations



Expansion logic and truth table

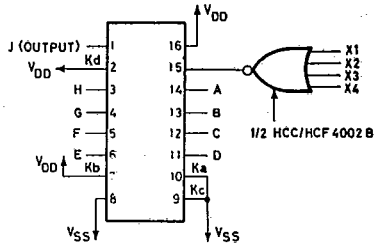
IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A+B+C+D+E+F+G+H) + (EXP)}$
OR	OR	$J = (A+B+C+D+E+F+G+H) + (EXP)$
AND	NAND	$J = (ABCDEFGH) \cdot (EXP)$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
OR/AND	NOR	$J = \overline{(A+B+C+D) \cdot (E+F+G+H) \cdot (EXP)}$
OR/NAND	NOR	$J = (A+B+C+D) \cdot (E+F+G+H) \cdot (EXP)$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$)

APPLICATIONS (continued)

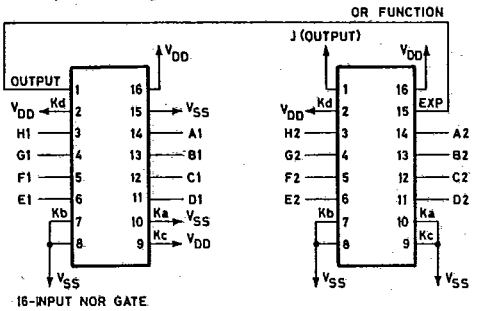
12-input OR/AND gate



12-INPUT OR/AND GATE
$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(X1+X2+X3+X4)$

S-2719

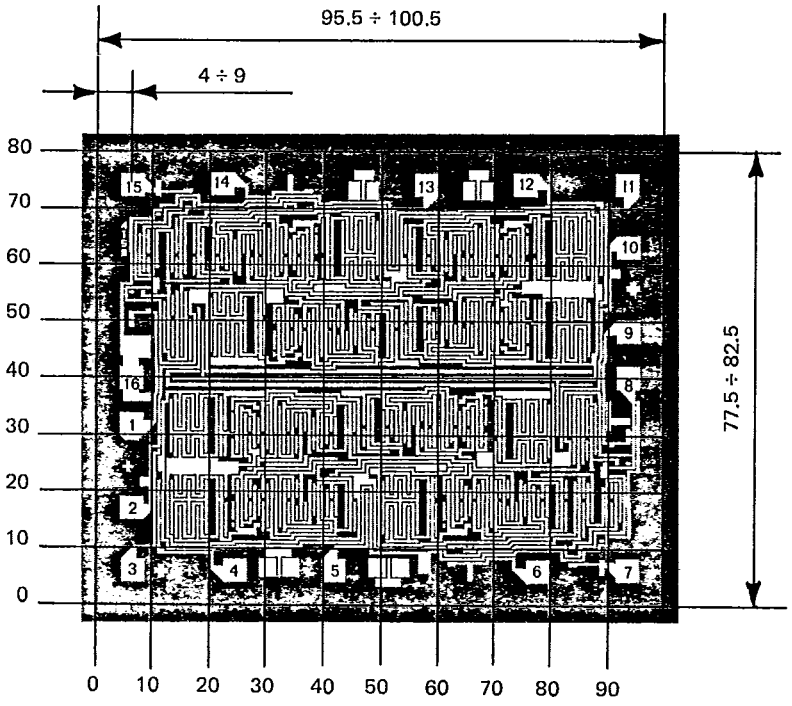
16-input NOR gate



16-INPUT NOR GATE

$\overline{J=A1+B1+C1+D1+E1+F1+G1+H1+A2+B2+C2+D2+E2+F2+G2+H2}$

S-1631



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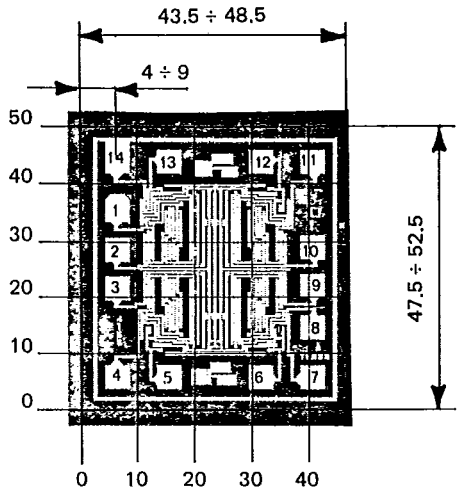

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