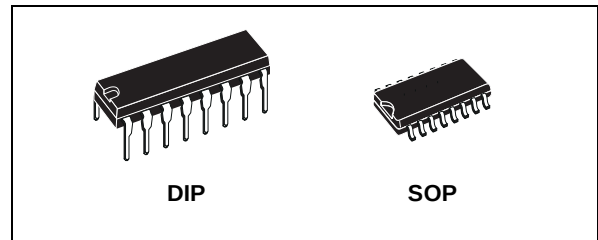


LOOK-AHEAD CARRY GENERATOR

- GENERATES HIGH-SPEED CARRY ACROSS FOUR ADDERS OR ADDER GROUPS
- HIGH-SPEED OPERATIONAL: $t_{PHL} = t_{PLH} = 100 \text{ ns (typ.)}$ AT $V_{DD} = 10V$
- CASCADABLE FOR FAST CARRIES OVER N BITS
- DESIGNED FOR USE WITH HCF40181B ALU
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- INPUT LEAKAGE CURRENT
 $I_l = 100nA \text{ (MAX)} \text{ AT } V_{DD} = 18V \text{ } T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

HCF40182B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. He is a high speed look-ahead carry generator capable of anticipating a carry across four binary adders or adder groups. HCF40182B is cascadable to perform full look-ahead across n-bit adders. Carry propagate-carry, and generate-carry functions are provided as

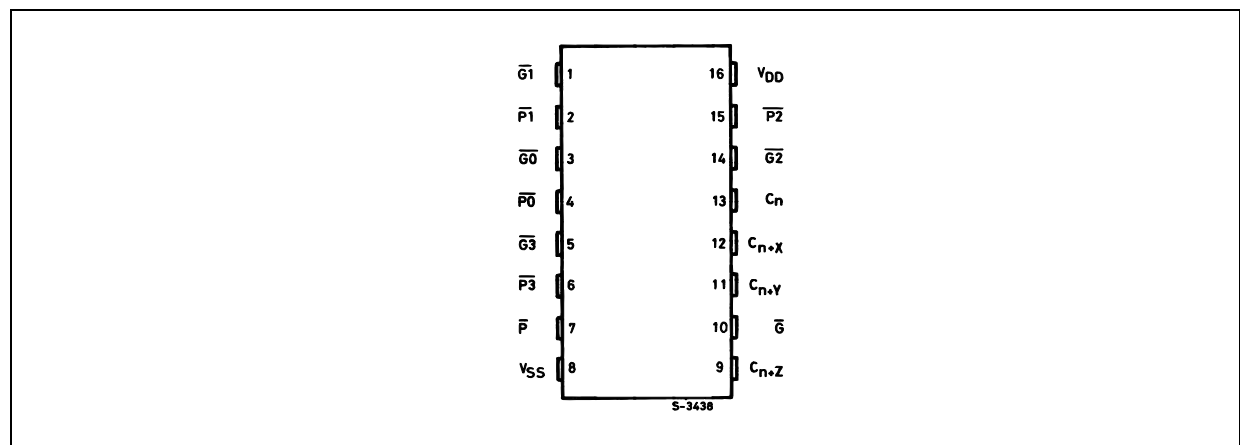


ORDER CODES

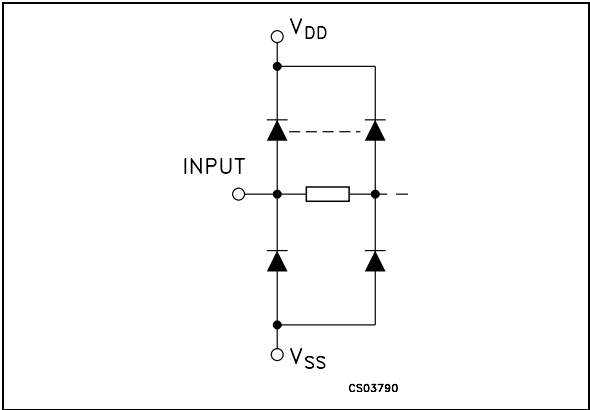
PACKAGE	TUBE	T & R
DIP	HCF40182BEY	
SOP	HCF40182BM1	HCF40182M013TR

enumerated in the terminal designation below. HCF40182B, when used in conjunction with the HCF40181B arithmetic logic unit (ALU), provides full high-speed look-ahead carry capability for up to n-bit words. Each HCF40182B generates the look-ahead (anticipated carry) across a group of four ALUs. In addition, other HCF40182Bs may be employed to anticipate the carry across sections of four look-ahead blocks up to n-bits.

PIN CONNECTION



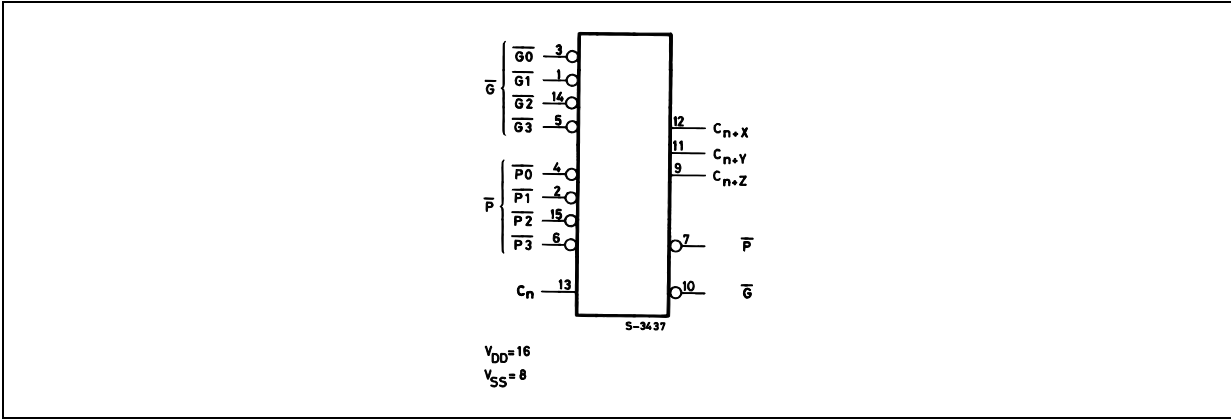
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G0}$ to $\overline{G3}$	Carry Generate Inputs (Active LOW)
4, 2, 15, 6	$\overline{P0}$ to $\overline{P3}$	Carry Propagate Inputs (Active LOW)
13	C_n	Active-high Carry Input
12, 11, 9	$C_{n+x}, C_{n+y}, C_{n+z}$	Active-high Carry Outputs
10	$\overline{G}$	Carry Propagate Output (Active LOW)
7	$\overline{P}$	Carry Generate Output (Active LOW)
8	Vss	Negative Supply Voltage
16	Vdd	Positive Supply Voltage

FUNCTIONAL DIAGRAM



TRUTH TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
ALL OTHER COMBINATIONS							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
ALL OTHER COMBINATIONS				H

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
ALL OTHER COMBINATIONS			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
ALL OTHER COMBINATIONS					L

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
ALL OTHER COMBINATIONS							L

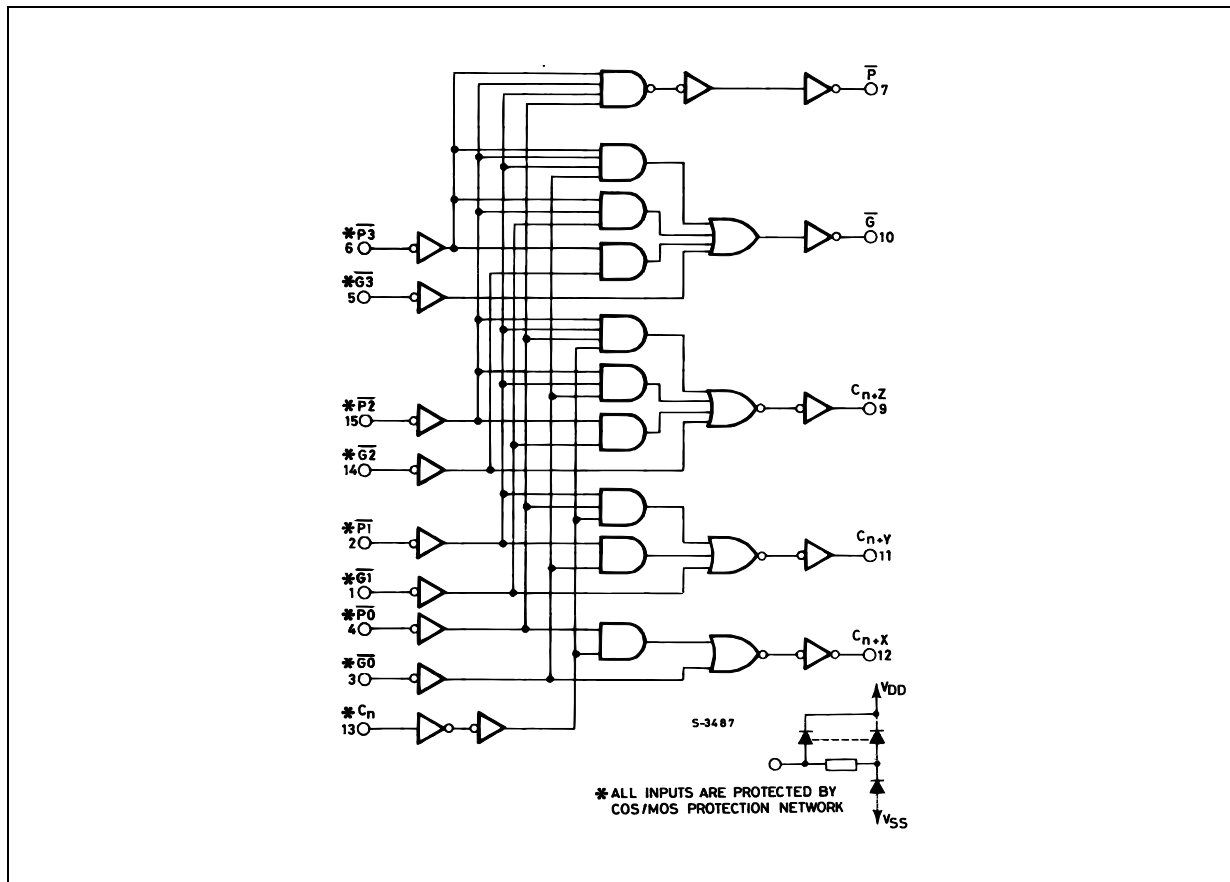
X : Don't Care

 $Cn+x = G0 + P0Cn$ $Cn+y = G1 + P1G0 + P1P0Cn$ $Cn+z = G2 + P2G1 + P2P1G0 + P2P1P0Cn$ $G = \overline{G3} + G3 + P3G2 + P3P2G1 + P3P2P1G0$ $P = \overline{P3}P2P1P0$

or

 $Cn+x = \overline{Y0} + (X0 + Cn)$ $Cn+y = \overline{Y1} + [X1 + Y0(X0 + Cn)]$ $Cn+z = \overline{Y2} + \{X2 + Y1[X1 + Y0(X0 + Cn)]\}$ $G = Y3 + (X3 + Y2)(X3 + X2 + Y1)(X3 + X2 + X1 + Y0)$ $P = X3 + X2 + X1 + X0$

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions				Value							Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/18.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		0.5/4.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			1.5/18.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5		5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6		5	-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4		5	0.44	1		0.36		0.36		mA
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	any input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input Capacitance		any input				5	7.5					pF

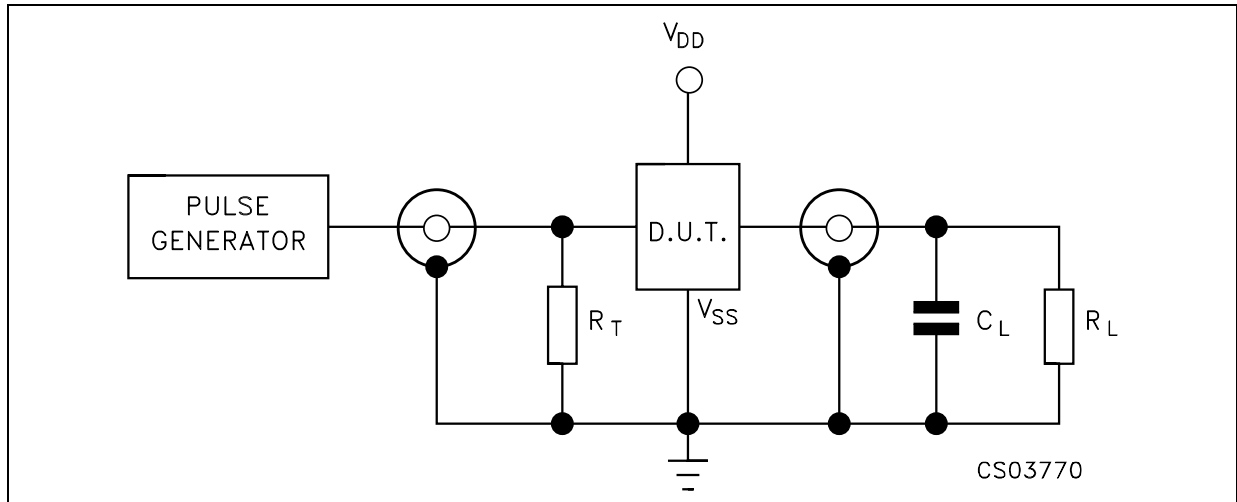
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200K Ω , t_r = t_f = 20 ns)

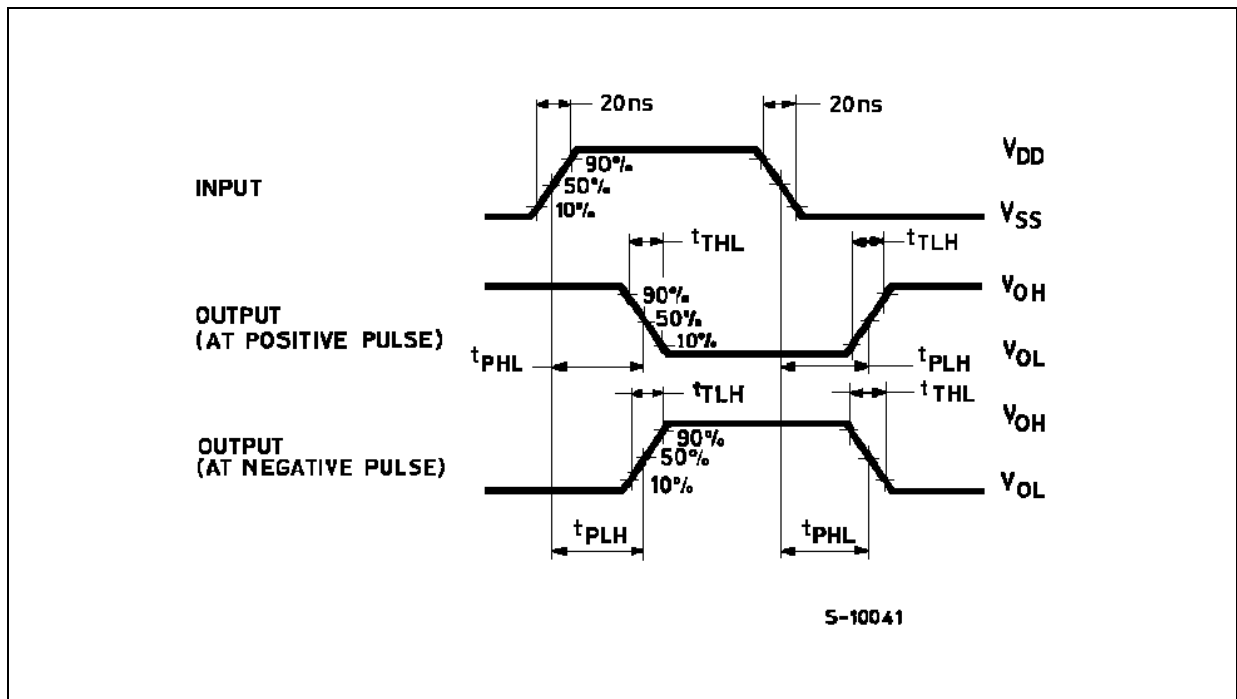
Symbol	Parameter	Test Condition		Value (*)			Unit
		V _{DD} (V)	See Timing Chart	Min.	Typ.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time P, G, in to P $\overline{G}$ Out and Carry Outs	5			200	400	ns
		10			100	200	
		15			75	150	
t _{PLH} t _{PHL}	Cn to Carry Outputs	5			240	480	ns
		10			120	240	
		15			90	180	
t _{THL} t _{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

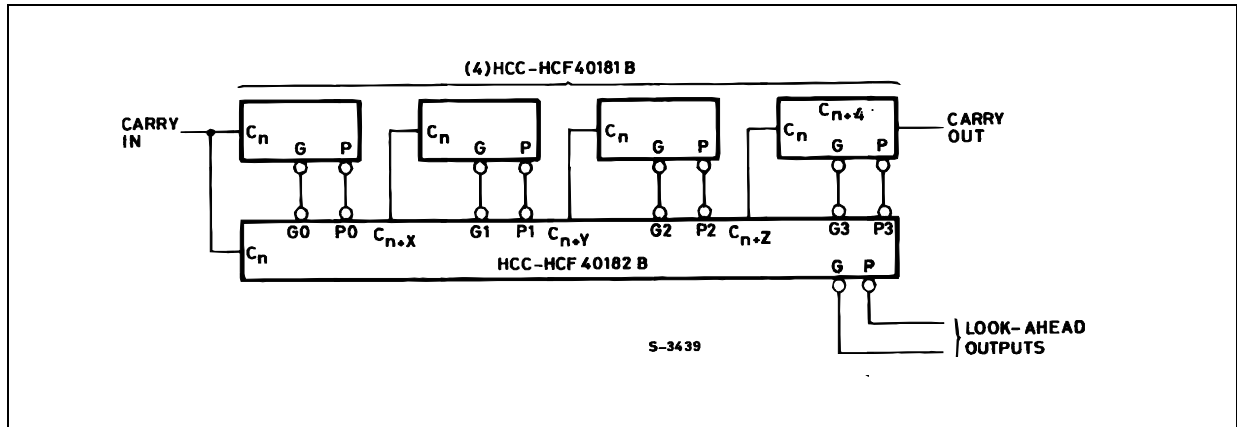
TEST CIRCUIT



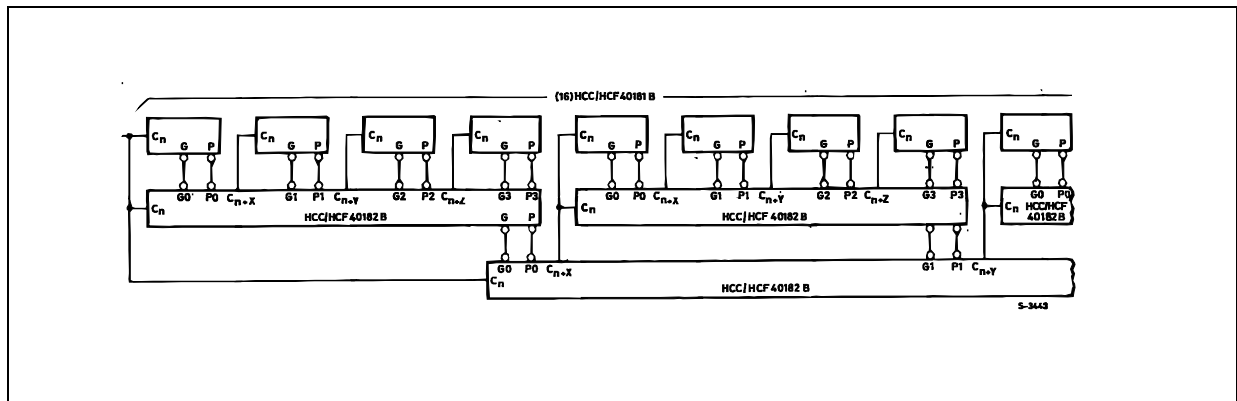
$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{k}\Omega$
 $R_T = Z_{\text{OUT}}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)

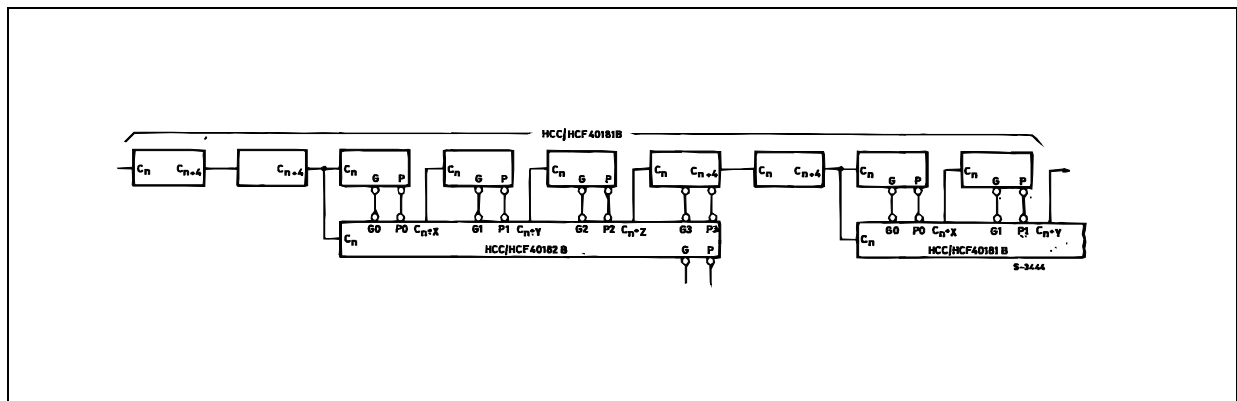
TYPICAL APPLICATION: 16-BIT TWO-LEVEL LOOK-AHEAD ALU



TYPICAL APPLICATION: 64-BIT FULL CARRY LOOK-AHEAD ALU IN 3 LEVELS

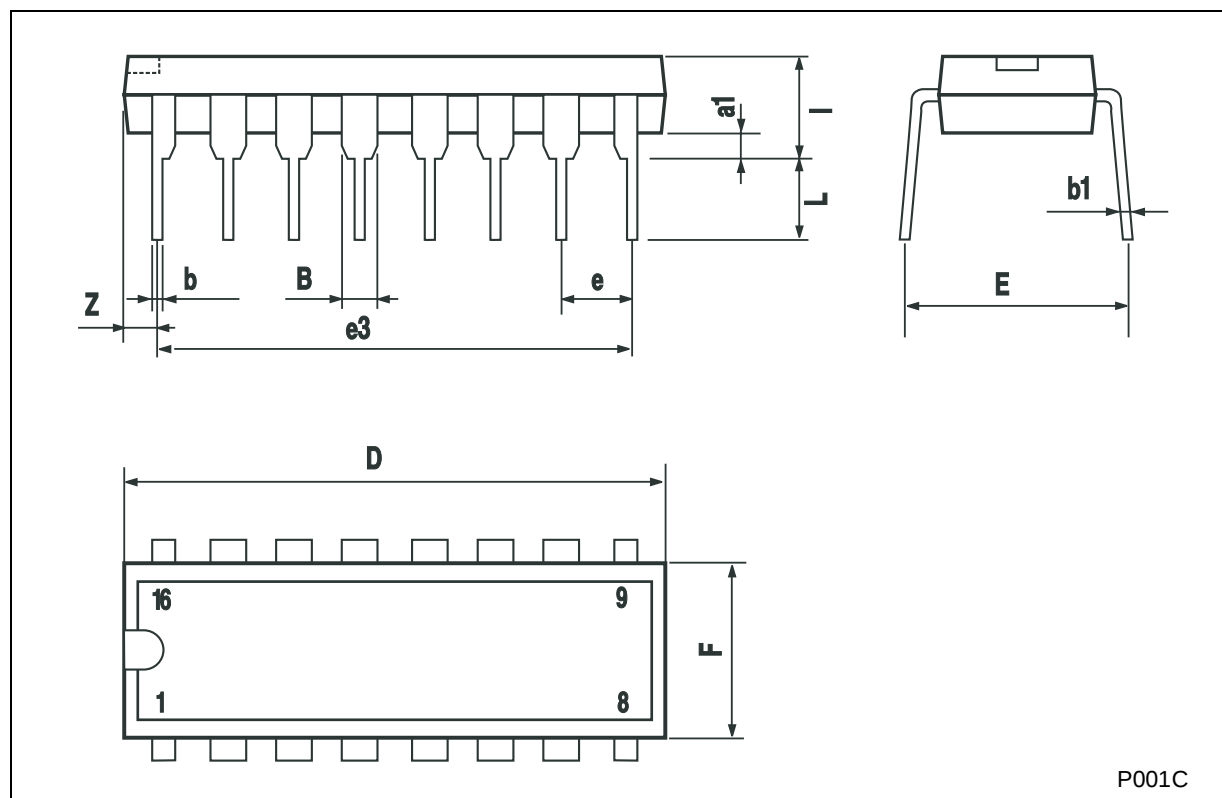


TYPICAL APPLICATION: COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE-CARRY ALU



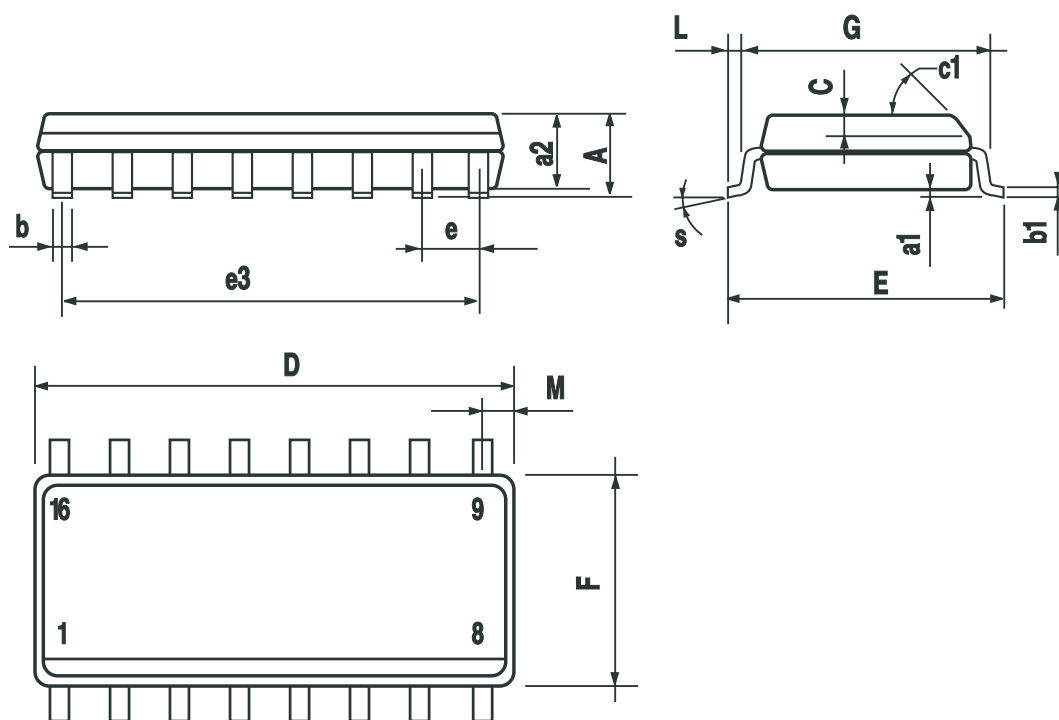
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>