

COS/MOS INTEGRATED CIRCUIT

4503 B

HCC/HCF 4503 B

HEX BUFFER

- 1 TTL-LOAD OUTPUT DRIVE CAPABILITY
- 2 OUTPUT-DISABLE CONTROLS
- 3 STATE OUTPUTS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4503B** (extended temperature range) and **HCF 4503B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.

The **HCC/HCF 4503B** is a hex noninverting buffer with 3-state outputs having high sink and source-current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20 V -0.5 to 18 V
V_I	Input voltage	-0.5 to V_{DD} +0.5 V
I_I	DC input current (any one input)	± 10 mA
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for T_{op} = full package-temperature range	200 mW 100 mW
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 °C -40 to 85 °C
T_{stg}	Storage temperature	-65 to 150 °C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* All voltages are with respect to V_{SS} (GND).

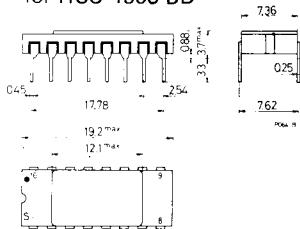
ORDERING NUMBERS:

- HCC 4503 BD for dual in-line, ceramic package
HCC 4503 BF for dual in-line ceramic package, frit seal
HCC 4503 BK for ceramic flat package
HCF 4503 BE for dual in-line plastic package
HCF 4503 BF for dual in-line ceramic package, frit seal

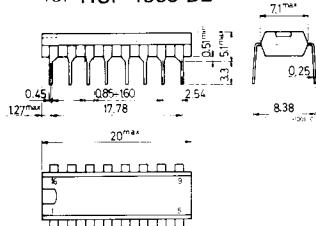
HCC/HCF 4503B

MECHANICAL DATA (dimensions in mm)

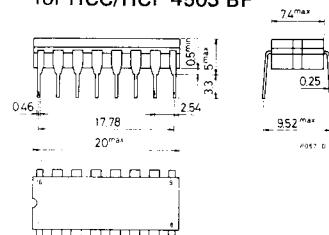
Dual in-line ceramic package
for HCC 4503 BD



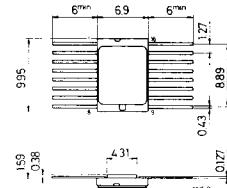
Dual in-line plastic package
for HCF 4503 BE



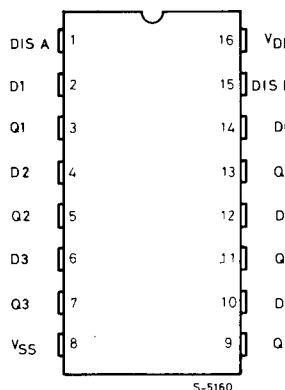
Dual in-line ceramic package
for HCC/HCF 4503 BF



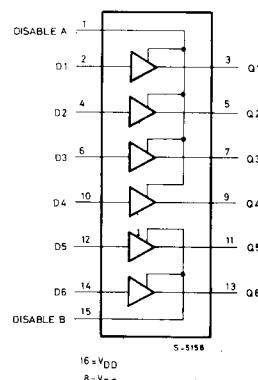
Ceramic flat package for
HCC 4503 BK



PIN CONNECTIONS



FUNCTIONAL DIAGRAM

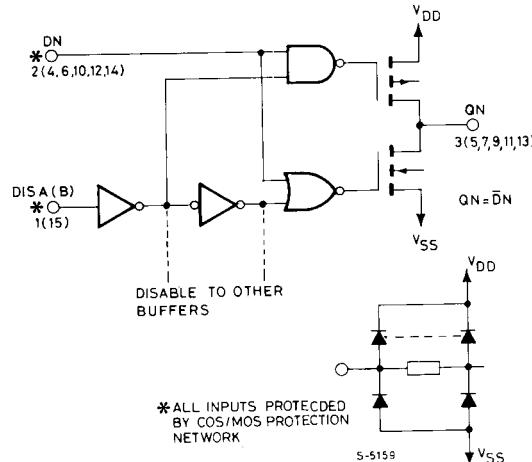


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: HCC types HCF types
V_I T_{Op}	Input voltage Operating temperature: HCC types HCF types

3 to 18	V
3 to 15	V
0 to V_{DD}	V
-55 to 125	$^{\circ}C$
-40 to 85	$^{\circ}C$

LOGIC DIAGRAM AND TRUTH TABLE

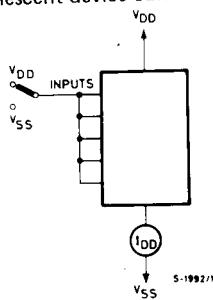


DN	DIS A (B)	QN
0	0	0
1	0	1
X	1	HIGH Z

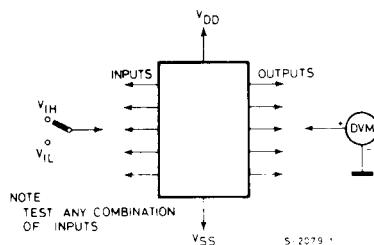
X = DON'T CARE

TEST CIRCUITS

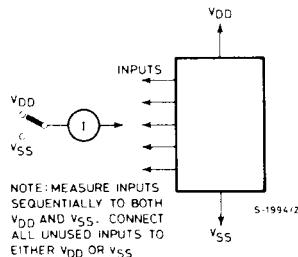
Quiescent device current



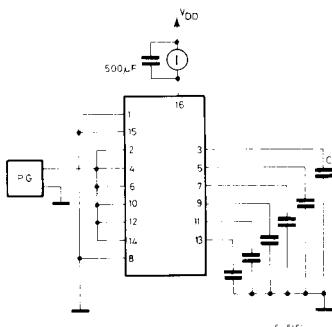
Input voltage



Input leakage current



Dynamic power dissipation



HCC/HCF 4503B

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions				Values						Unit		
		V_i (V)	V_O (V)	$ I_{O1} $ (μA)	V_{DD} (V)	T_{Low}^*		25°C			T_{High}^*			
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I_L Quiescent current	HCC types	0/ 5			5		1		0.02	1		30	μA	
		0/10			10		2		0.02	2		60		
		0/15			15		4		0.02	4		120		
		0/20			20		20		0.04	20		600		
	HCF types	0/ 5			5		4		0.02	4		30		
		0/10			10		8		0.02	8		60		
		0/15			15		16		0.02	16		120		
		0/ 5	< 1	5	4.95		4.95			4.95				
V_{OH} Output high voltage		0/10	< 1	10	9.95		9.95			9.95			V	
		0/15	< 1	15	14.95		14.95			14.95				
		5/0	< 1	5	0.05				0.05			0.05		
V_{OL} Output low voltage		10/0	< 1	10	0.05				0.05			0.05	V	
		15/0	< 1	15	0.05				0.05			0.05		
		0.5/4.5	< 1	5	3.5		3.5			3.5				
V_{IH} Input high voltage		1/9	< 1	10	7		7			7			V	
		1.5/13.5	< 1	15	11		11			11				
		4.5/0.5	< 1	5	1.5				1.5			1.5		
V_{IL} Input low voltage		9/1	< 1	10	3				3			3	V	
		13.5/1.5	< 1	15	4				4			4		
		0/ 5	2.5	5	-5.8		-4.8		-6.1			-3		
I_{OH} Output drive current	HCC types	0/ 5	4.6	5	-1.2		-1.02		-1.9			-0.7	mA	
		0/10	9.5	10	-3.1		-2.6		-3.7			-1.8		
		0/15	13.5	15	-8.2		-6.8		-14.1			-4.8		
		0/ 5	2.5	5	-4.8		-4.1		-5.2			-2.9		
	HCF types	0/ 5	4.6	5	-1		-0.8		-1.6			-0.6		
		0/10	9.5	10	-2.5		-2.2		-3.1			-1.6		
		0/15	13.5	15	-6.8		-5.8		-11.9			-4.2		
		0/ 5	0.4	5	2.6		2.1		2.3			1.3		
I_{OL} Output sink current	HCC types	0/10	0.5	10	6.5		5.5		2.6			3.8	mA	
		0/15	1.5	15	19.2		16.1		23			11.2		
		0/ 5	0.4	5	2.1		1.8		1.9			1.2		
	HCF types	0/10	0.5	10	5.4		4.7		5.3			3.3		
		0/15	1.5	15	1.6		13.7		19.5			9.7		
		0/18	Any input		18		± 0.1		$\pm 10^{-5}$		± 0.1		± 1	μA
I_{IH}, I_{IL} Input leakage current		0/15			15		± 0.3		$\pm 10^{-5}$		± 0.3		± 1	
3-state output	HCC types	0/18	0/18		18		± 0.4		$\pm 10^{-4}$		± 0.4		± 12	μA
	HCF types	0/15	0/15		15		± 1.0		$\pm 10^{-4}$		± 1.0		± 7.5	
C_I	Input capacitance		Any input							5	7.5			pF

* $T_{Low} = -55^\circ C$ for HCC device; $-40^\circ C$ for HCF device.

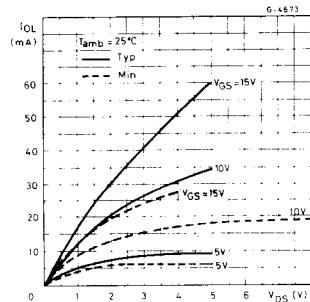
* $T_{High} = +125^\circ C$ for HCC device; $+85^\circ C$ for HCF device.

The Noise Margin for both "1" and "0" level is:
 1V min. with $V_{DD} = 5V$
 2V min. with $V_{DD} = 10V$
 2.5V min. with $V_{DD} = 15V$

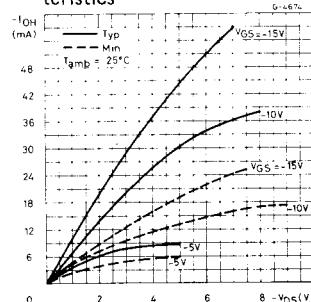
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, typical temperature coefficient for all $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ values, all input rise and fall time = 20 ns)

Parameter	Test conditions	Values			Unit	
		V_{DD} (V)	Min.	Typ.		
t_{PLH}, t_{PHL}	Low-to-High	5		75	150	ns
		10		35	70	
		15		25	50	
		5		55	110	
		10		25	50	
		15		17	35	
	High-to-Low	5		70	140	
		10		30	60	
		15		25	50	
		5		90	180	
		10		40	80	
t_{PZH}, t_{PHZ}	3-state propagation delay time	15		35	70	ns
		5		90	180	
		10		40	80	
		15		35	70	
		5		50	90	
	3-state propagation delay time	10		30	45	
		15		25	35	
		5		35	70	
		10		20	40	
		15		13	25	

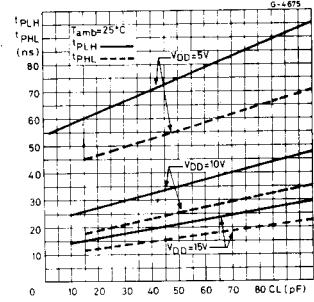
N-Channel output low(sink) current characteristics



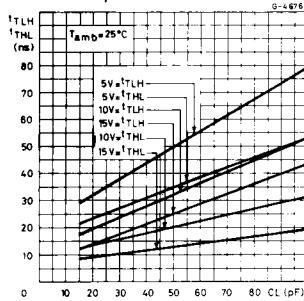
P-Channel output high (source) current characteristics



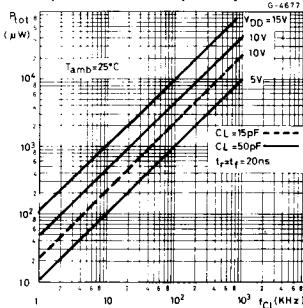
Typical propagation delay time vs. load capacitance



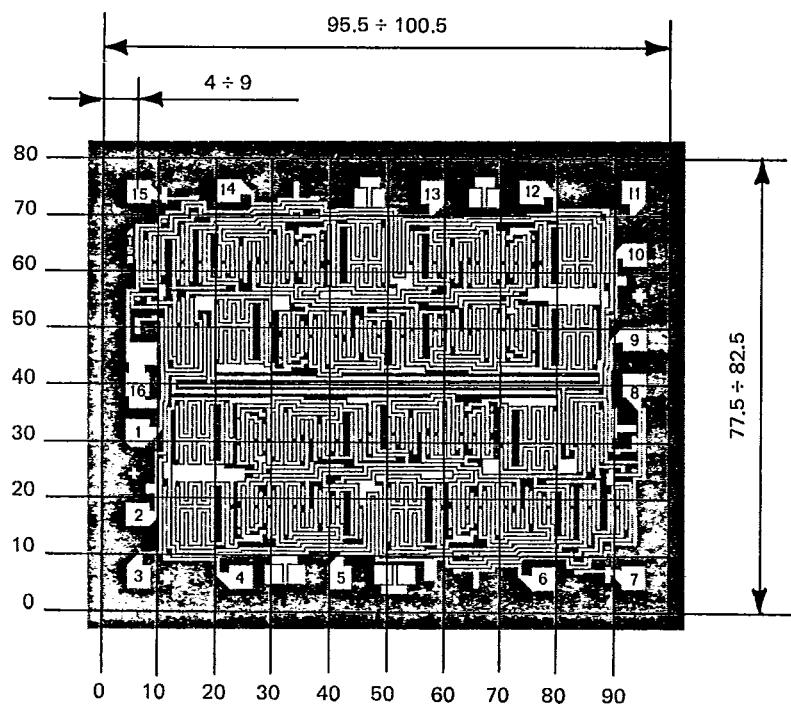
Typical transition time vs.
load capacitance



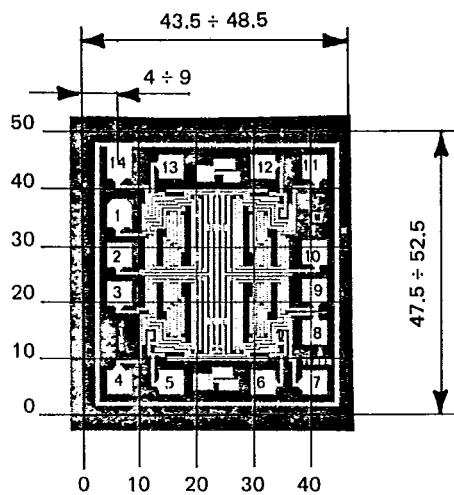
Typical dynamic power dis-
sipation vs. frequency



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7929225 S G S SEMICONDUCTOR CORP



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