SIGNAL PROCESSING TECHNOLOGIES

HCMP96870A

DUAL ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay <2.3 ns
- Propagation Delay Skew <300 ps
- 300 MHz Minimum Tracking Bandwidth
- Low Offset ±3 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

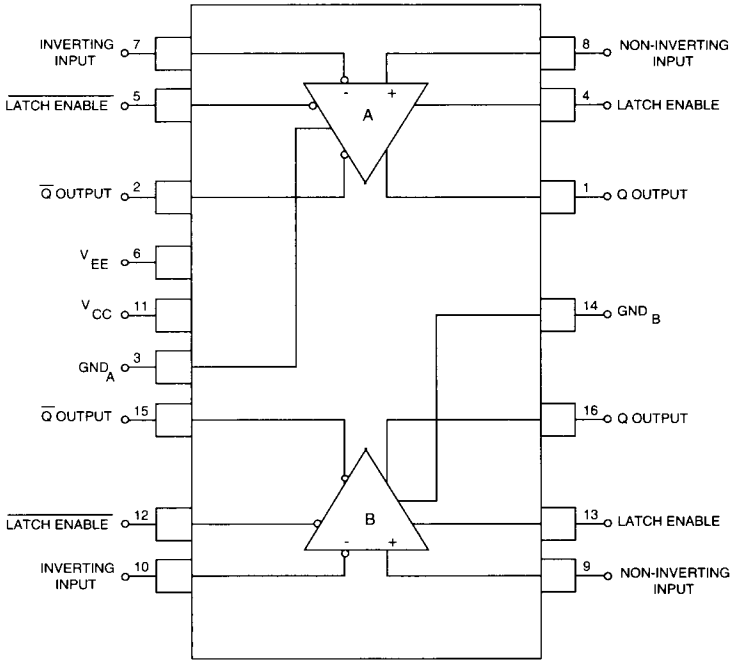
GENERAL DESCRIPTION

The HCMP96870A is a dual, very high speed monolithic comparator. It is pin-compatible with, and has improved performance over AMD's AM6687 and Analog Devices AD9687. The HCMP96870A is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96870A is available in a 16 lead cerdip, 16 lead PDIP, 20 contact leadless chip carrier (LCC), 20 lead PLCC, and in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND)..... -0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND)..... -6.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5 V

Input Voltages

Input Voltage.....-4.0 to +4.0 V
Differential Input Voltage.....-5.0 to +5.0 V
Input Voltage, Latch Controls.....V_{EE} to 0.5 V

Output

Output Current.....30 mA

Temperature

Operating Temperature, ambient.....0 to +70 °C
junction.....+150 °C
Lead Temperature, (soldering 60 seconds)..... +300 °C
Storage Temperature..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	III	-3	±.5	+3	mV
Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
Offset Voltage Tempco		V		4		µV/°C
Input Bias Current		I		6	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7	±38	µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		7	10	mA
Negative Supply Current		I		27	36	mA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	IV	50	100		dB
Common Mode Rejection Ratio		IV	50	85		dB

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Power Dissipation	I_{OUTPUT} = 0 mA	I		185	250	mW
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[1]						
Propagation Delay	10 mV OD	III		2.0	2.3	ns
Latch Set-up Time		III		0.6	1	ns
Latch to Output Delay	50 mV OD	III			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		III			0.5	ns
Rise Time	20% to 80%	V		1.2		ns
Fall Time	20% to 80%	V		1.2		ns
Min Clock Rate		V		300		MHz

Note 1. 100 mV input step.

TEST LEVEL CODES

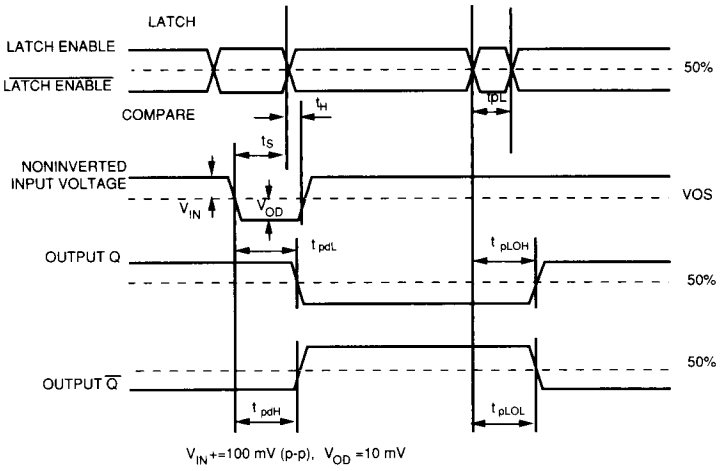
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected (LE is the inverse of $\overline{LE}$).

SWITCHING TERMS (refer to Figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

$t_{pdL} - t_{pdH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.

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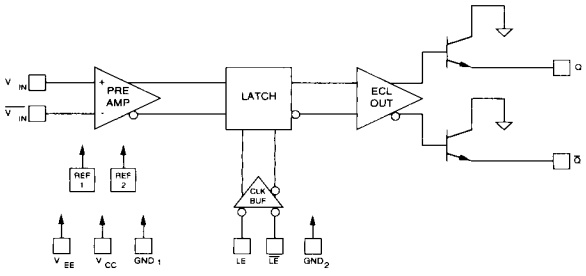
INTERNAL FUNCTIONAL DIAGRAM



GENERAL INFORMATION

The HCMP96870A is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The HCMP96870A has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

This comparator offers the following improvements over existing devices:

- Shorter propagation delays
- Lower offset voltage and temperature coefficient
- Lower overall system power
- Better rejection between comparator channels
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in Figure 2. Although it needs few external components and is easy to apply, there are several conditions that should be met to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96870A comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, and the input impedance to the part should be kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96870A is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the HCMP96870A, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states. Please note that the Latch Enable and $\overline{\text{Latch Enable}}$ notations are not consistent with the industry standard; these names have always been opposite to the pins' functional descriptions. Please see the timing diagram in Figure 1 for absolute clarification.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and LE rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused latch enable pins should be connected to the appropriate supplies: ground or V_{EE}.

Figure 2 - Typical Interface Circuit

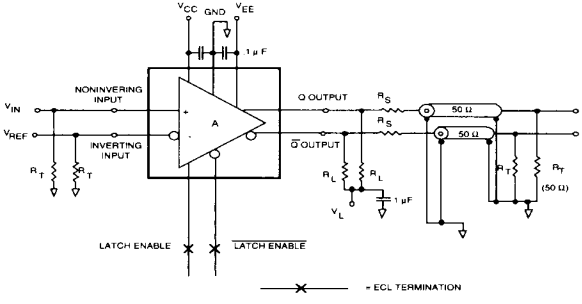


Figure 3 - Equivalent Input Circuit

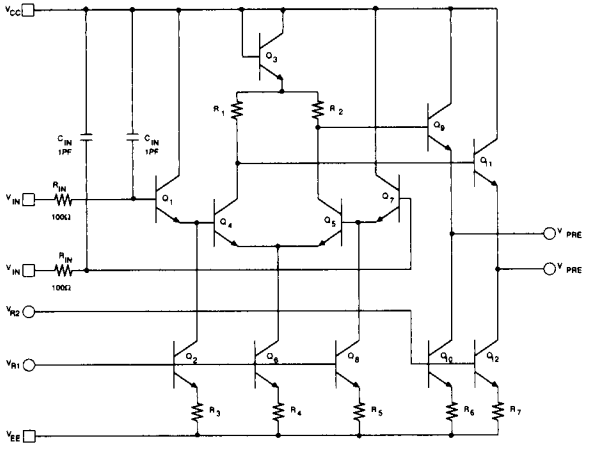


Figure 4 - Output Circuit

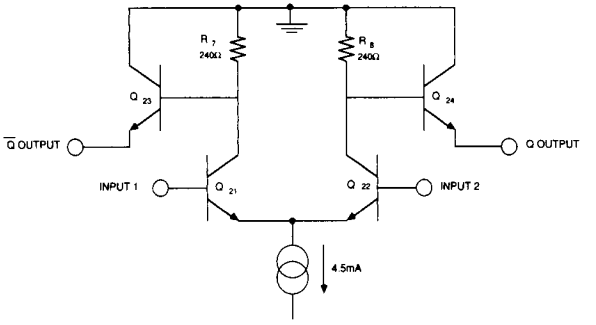


Figure 5A - Test Load

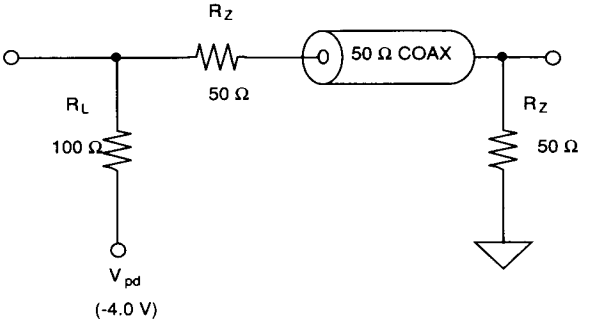
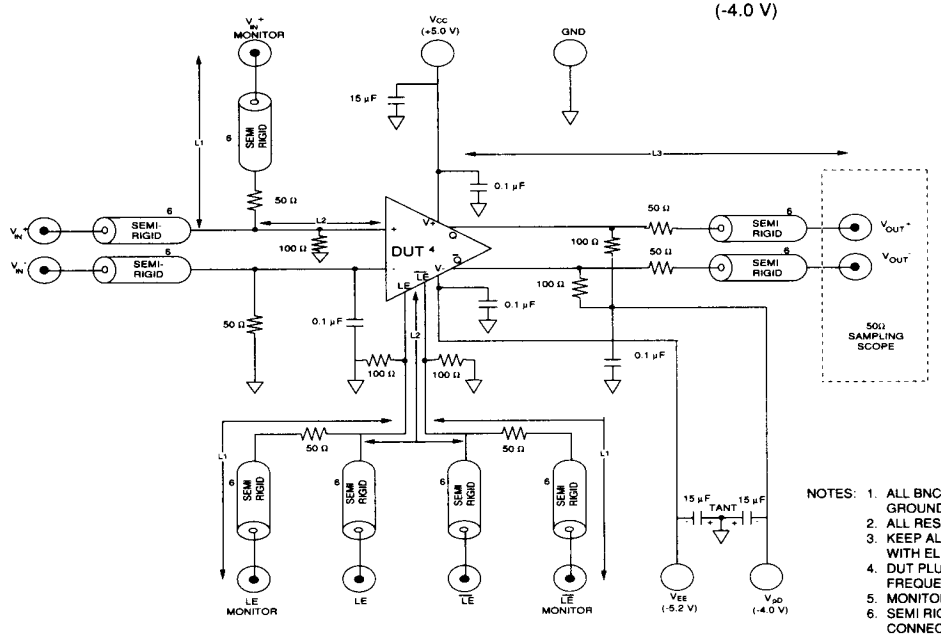


Figure 5B - AC Test Fixture



NOTES:
1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (50 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. DUT PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

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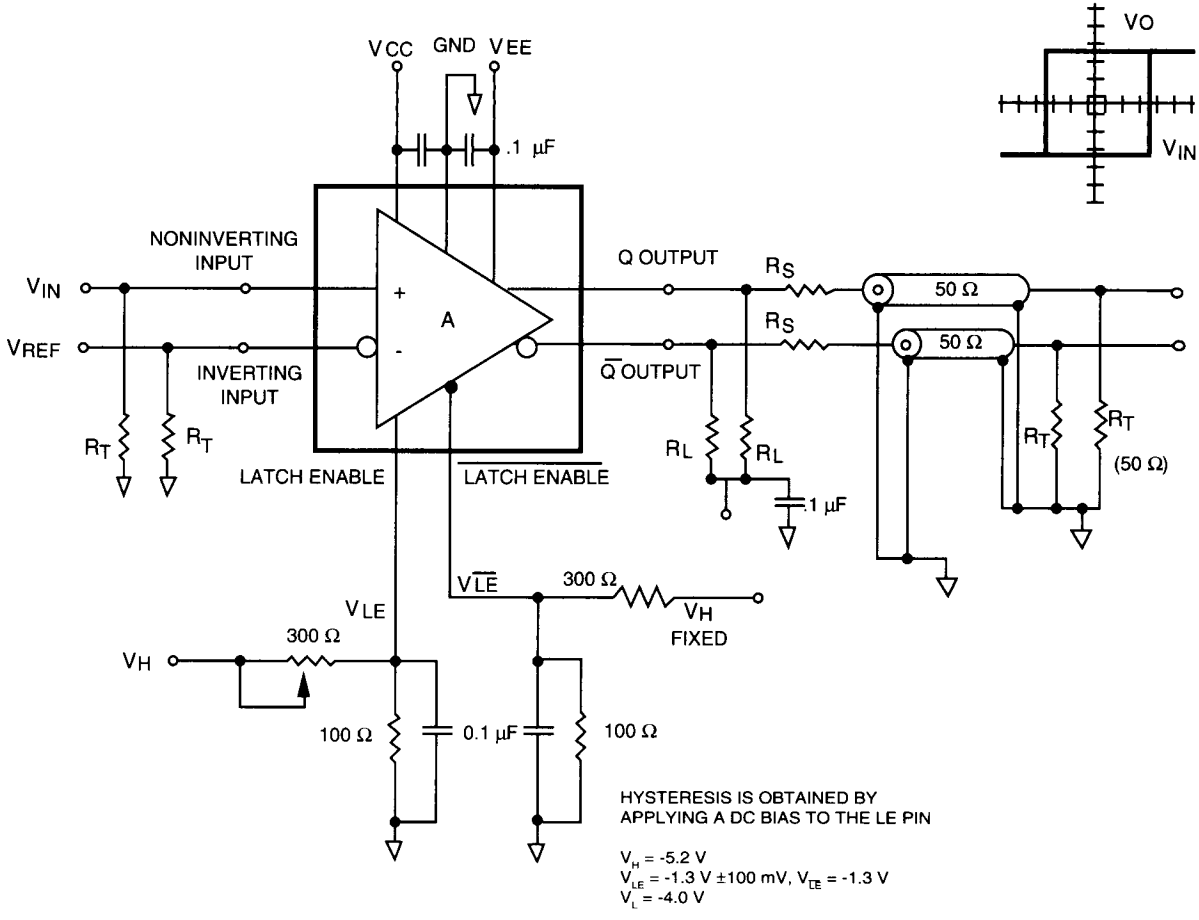
Figure 6 - HCMP96870A with Hysteresis



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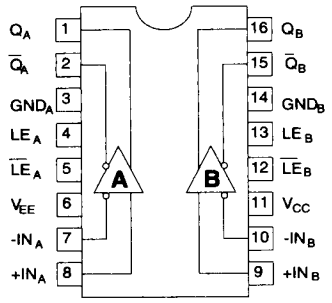
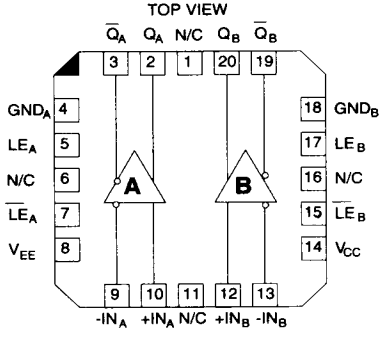
PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

TOP VIEW



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PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Latch Enabled B
$\overline{LE}_B$	Inverted Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

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