



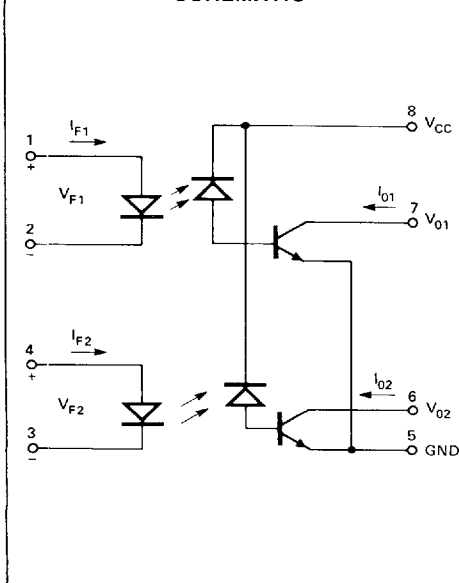
HEWLETT  
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# DUAL LOGIC INTERFACE OPTOCOUPLER

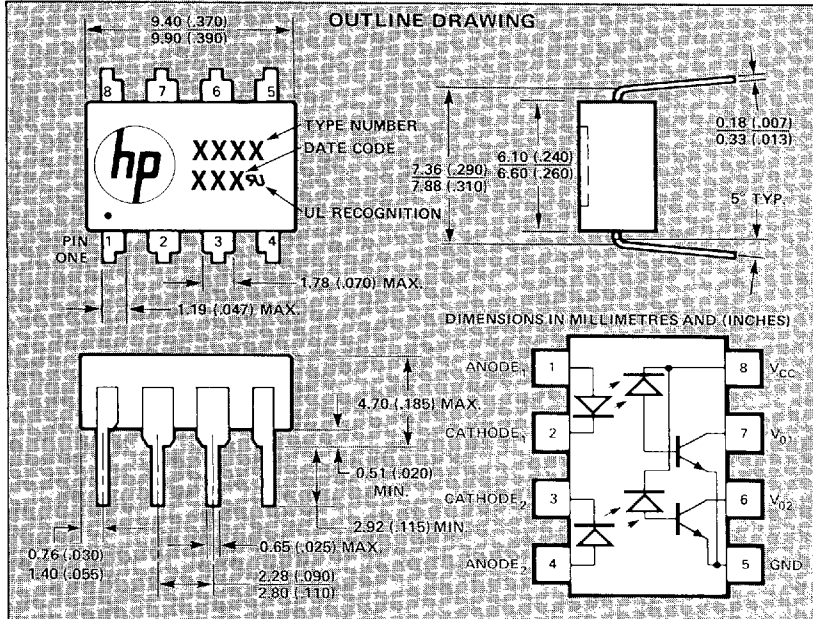
HCPL-2533

TECHNICAL DATA DECEMBER 1981

**SCHEMATIC**



**OUTLINE DRAWING**



## Features

- DATA RATES TO 250k b/s NRZ
- LSTTL COMPATIBLE
- HIGH COMMON MODE TRANSIENT IMMUNITY:  
>1000V/ $\mu$ s
- HIGH DENSITY PACKAGING
- 3000 Vdc WITHSTAND TEST VOLTAGE
- OPEN COLLECTION OUTPUTS
- RECOGNIZED UNDER THE COMPONENT  
PROGRAM OF UNDERWRITERS  
LABORATORIES, INC. (FILE NO. E55361)

## Description

The HCPL-2533 is a dual channel optocoupler which is specified for use in LSTTL to LSTTL and TTL to LSTTL logic interfaces. A nominal 8 mA LSTTL sink current through the input LED will provide enough output current for proper operation of 1 LSTTL gate under worst-case conditions when used in the recommended circuits. The CTR of the HCPL-2533 is 15% minimum at  $I_F = 8$  mA.

The HCPL-2533 contains a pair of light emitting diodes and integrated photon detectors with a 3000V dc withstand test between input and output. Separate connection for the photodiode bias and output transistor collector reduce the base-collector capacitance, giving improved speed compared with conventional phototransistor couplers.

## Applications

- HIGH SPEED LOGIC GROUND ISOLATION —  
LSTTL-TO-LSTTL AND TTL-TO-LSTTL

## Absolute Maximum Ratings

|                                                                      |                                                           |
|----------------------------------------------------------------------|-----------------------------------------------------------|
| Storage Temperature                                                  | -55°C to +125°C                                           |
| Operating Temperature                                                | -55°C to +100°C                                           |
| Lead Solder Temperature                                              | 260°C for 10s<br>(1.6mm below seating plane)              |
| Average Input Current — $I_F$ (each channel)                         | 25mA <sup>(1)</sup>                                       |
| Peak Input Current — $I_F$ (each channel)                            | 50mA <sup>(2)</sup><br>(50% duty cycle, 1 ms pulse width) |
| Peak Transient Input Current —<br>$I_F$ (each channel)               | 1.0 A<br>( $\leq 1\mu$ s pulse width, 300pps)             |
| Reverse Input Voltage — $V_R$ (each channel)                         | 5V                                                        |
| Input Power Dissipation (each channel)                               | 45mW <sup>(3)</sup>                                       |
| Average Output Current — $I_O$ (each channel)                        | 8mA                                                       |
| Peak Output Current — $I_O$ (each channel)                           | 16mA                                                      |
| Supply and Output Voltage — $V_{CC}$ (Pin 8-5),<br>$V_O$ (Pin 7,6-5) | -0.5V to 7V                                               |
| Output Power Dissipation (each channel)                              | 35mW <sup>(4)</sup><br>(See notes, following page.)       |

## Electrical Specifications, LSTTL/LSTTL

Over recommended temperature ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ) unless otherwise specified.

| Parameter                                  | Symbol                          | Min. | Typ.* | Max. | Units                      | Test Conditions                                                                               | Fig. | Note |
|--------------------------------------------|---------------------------------|------|-------|------|----------------------------|-----------------------------------------------------------------------------------------------|------|------|
| Current Transfer Ratio                     | CTR                             | 15   | 22    |      | %                          | $I_F = 8\text{mA}$ , $V_O = 0.5\text{V}$ , $V_{CC} = 4.5\text{V}$<br>$T_A = 25^\circ\text{C}$ | 1    | 5,6  |
|                                            |                                 | 11   | 15    |      | %                          | $I_F = 8\text{mA}$ , $V_O = 0.5\text{V}$ , $V_{CC} = 4.5\text{V}$                             |      |      |
| Logic Low Output Voltage                   | $V_{OL}$                        |      | 0.2   | 0.5  | V                          | $I_F = 8\text{mA}$ , $I_O = 0.7\text{mA}$ ,<br>$V_{CC} = 4.5\text{V}$                         |      | 5    |
| Logic Low Supply Current                   | $I_{CCL}$                       |      | 40    |      | $\mu\text{A}$              | $I_{F1} = I_{F2} = 8\text{mA}$<br>$V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 5.5\text{V}$    |      |      |
| Input Forward Voltage                      | $V_F$                           |      | 1.5   | 1.7  | V                          | $I_F = 8\text{mA}$ , $T_A = 25^\circ\text{C}$                                                 | 2    | 5    |
| Temperature Coefficient of Forward Voltage | $\frac{\Delta V_F}{\Delta T_A}$ |      | -1.6  |      | $\text{mV}/^\circ\text{C}$ | $I_F = 8\text{mA}$                                                                            |      | 5    |

## Switching Specifications at $T_A = 25^\circ\text{C}$

$V_{CC} = 5\text{V}$ ,  $I_F = 8\text{mA}$ ,  $R_L = 7.5\text{k}\Omega$  unless otherwise specified.

| Parameter                                                 | Symbol    | Min. | Typ.  | Max. | Units                  | Test Conditions                                  | Fig. | Note |
|-----------------------------------------------------------|-----------|------|-------|------|------------------------|--------------------------------------------------|------|------|
| Propagation Delay Time to Logic Low at Output             | $t_{PHL}$ |      | 0.8   | 1.5  | $\mu\text{s}$          |                                                  | 4,6  | 10   |
| Propagation Delay Time to Logic High at Output            | $t_{PLH}$ |      | 1.0   | 2.5  | $\mu\text{s}$          |                                                  | 4,6  | 10   |
| Common Mode Transient Immunity at Logic High Level Output | $CM_H$    |      | 1000  |      | $\text{V}/\mu\text{s}$ | $I_F = 0\text{mA}$ , $V_{CM} = 10\text{V}_{p-p}$ | 7    | 9,10 |
| Common Mode Transient Immunity at Logic Low Level Output  | $CM_L$    |      | -1000 |      | $\text{V}/\mu\text{s}$ | $V_{CM} = 10\text{V}_{p-p}$                      | 7    | 9,10 |

## Electrical Specifications, TTL/LSTTL

Over recommended temperature ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ) unless otherwise specified.

| Parameter                                  | Symbol                          | Min. | Typ.* | Max. | Units                      | Test Conditions                                                                                  | Fig. | Note |
|--------------------------------------------|---------------------------------|------|-------|------|----------------------------|--------------------------------------------------------------------------------------------------|------|------|
| Current Transfer Ratio                     | CTR                             | 12   | 18    |      | %                          | $I_F = 16\text{mA}$ , $V_O = 0.5\text{V}$ ,<br>$V_{CC} = 4.5\text{V}$ , $T_A = 25^\circ\text{C}$ | 1    | 5,5  |
|                                            |                                 | 9    | 13    |      | %                          | $I_F = 16\text{mA}$ , $V_O = 0.5\text{V}$ ,<br>$V_{CC} = 4.5\text{V}$                            |      |      |
| Logic Low Output Voltage                   | $V_{OL}$                        |      | 0.2   | 0.5  | V                          | $I_F = 16\text{mA}$ , $I_O = 1.1\text{mA}$ ,<br>$V_{CC} = 4.5\text{V}$                           |      | 5    |
| Logic Low Supply Current                   | $I_{CCL}$                       |      | 80    |      | $\mu\text{A}$              | $I_{F1} = I_{F2} = 16\text{mA}$<br>$V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 5.5\text{V}$      |      |      |
| Input Forward Voltage                      | $V_F$                           |      | 1.5   | 1.7  | V                          | $I_F = 16\text{mA}$ , $T_A = 25^\circ\text{C}$                                                   | 2    | 5    |
| Temperature Coefficient of Forward Voltage | $\frac{\Delta V_F}{\Delta T_A}$ |      | -1.6  |      | $\text{mV}/^\circ\text{C}$ | $I_F = 16\text{mA}$                                                                              |      | 5    |

## Switching Specifications at $T_A = 25^\circ\text{C}$

$V_{CC} = 5\text{V}$ ,  $I_F = 16\text{mA}$ ,  $R_L = 4.7\text{k}\Omega$  unless otherwise specified.

| Parameter                                                 | Symbol    | Min. | Typ.  | Max. | Units                  | Test Conditions                                  | Fig. | Note |
|-----------------------------------------------------------|-----------|------|-------|------|------------------------|--------------------------------------------------|------|------|
| Propagation Delay Time to Logic Low at Output             | $t_{PHL}$ |      | 0.3   | 1.5  | $\mu\text{s}$          |                                                  | 4,6  | 11   |
| Propagation Delay Time to Logic High at Output            | $t_{PLH}$ |      | 1.1   | 2.5  | $\mu\text{s}$          |                                                  | 4,6  | 11   |
| Common Mode Transient Immunity at Logic High Level Output | $CM_H$    |      | 1000  |      | $\text{V}/\mu\text{s}$ | $I_F = 0\text{mA}$ , $V_{CM} = 10\text{V}_{p-p}$ | 7    | 9,11 |
| Common Mode Transient Immunity at Logic Low Level Output  | $CM_L$    |      | -1000 |      | $\text{V}/\mu\text{s}$ | $V_{CM} = 10\text{V}_{p-p}$                      | 7    | 9,11 |

\*All typicals at  $25^\circ\text{C}$ .

(See following page for notes.)

# Electrical Specifications

Over recommended temperature ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ) unless otherwise specified

| Parameter                               | Symbol    | Min. | Typ.*     | Max. | Units         | Test Conditions                                                                                       | Fig. | Note |
|-----------------------------------------|-----------|------|-----------|------|---------------|-------------------------------------------------------------------------------------------------------|------|------|
| Logic High Output Current               | $I_{OH}$  |      | 0.5       |      | nA            | $T_A = 25^\circ\text{C}$ , $I_{F1} = I_{F2} = 0\text{mA}$<br>$V_{O1} = V_{O2} = V_{CC} = 5.5\text{V}$ | 5    | 5    |
|                                         |           |      |           | 50   | $\mu\text{A}$ | $I_{F1} = I_{F2} = 0\text{mA}$<br>$V_{O1} = V_{O2} = V_{CC} = 5.5\text{V}$                            |      | 5    |
| Logic High Supply Current               | $I_{CCH}$ |      | 0.05      | 4    | $\mu\text{A}$ | $I_{F1} = I_{F2} = 0\text{mA}$<br>$V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 5.5\text{V}$            |      |      |
| Input Reverse Breakdown Voltage         | $V_R$     | 5    |           |      | V             | $I_F = 10\text{ }\mu\text{A}$ , $T_A = 25^\circ\text{C}$                                              |      | 5    |
| Input Capacitance                       | $C_{IN}$  |      | 60        |      | pF            | $f = 1\text{ MHz}$ , $V_F = 0\text{V}$                                                                |      | 5    |
| Input-Output Insulation Leakage Current | $I_{I-O}$ |      |           | 1.0  | $\mu\text{A}$ | 45% Relative Humidity, $t = 5\text{s}$<br>$V_{I-O} = 3000\text{V dc}$ , $T_A = 25^\circ\text{C}$      |      | 7    |
| Resistance (Input-Output)               | $R_{I-O}$ |      | $10^{12}$ |      | $\Omega$      | $V_{I-O} = 500\text{V dc}$                                                                            |      | 7    |
| Capacitance (Input-Output)              | $C_{I-O}$ |      | 0.6       |      | pF            | $f = 1\text{ MHz}$                                                                                    |      | 7    |
| Input-Input Insulation Leakage Current  | $I_{I-I}$ |      | 0.005     |      | $\mu\text{A}$ | 45% Relative Humidity, $t = 5\text{s}$<br>$V_{I-I} = 500\text{V dc}$                                  |      | 8    |
| Resistance (Input-Input)                | $R_{I-I}$ |      | $10^{11}$ |      | $\Omega$      | $V_{I-I} = 500\text{V dc}$                                                                            |      | 8    |
| Capacitance (Input-Input)               | $C_{I-I}$ |      | 0.25      |      | pF            | $f = 1\text{ MHz}$                                                                                    |      | 8    |

## Notes:

- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.8\text{mA}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $1.6\text{mA}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.9\text{mW}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $1.0\text{mW}/^\circ\text{C}$ .
- Each channel.
- CURRENT TRANSFER RATIO is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.
- Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
- Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
- Common mode transient immunity in Logic High level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse  $V_{CM}$ , to assure that the output will remain in a Logic High state (i.e.,  $V_O > 2.0\text{V}$ ). Common mode transient immunity in Logic Low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a Logic Low state (i.e.,  $V_O < 0.8\text{V}$ ).
- The  $7.5\text{k}\Omega$  load represents 1 LSTTL until load of  $0.36\text{mA}$  and a  $20\text{k}\Omega$  pull-up resistor.
- The  $4.7\text{k}\Omega$  load represents 1 LSTTL unit load of  $0.36\text{mA}$  and an  $8.2\text{k}\Omega$  pull-up resistor.

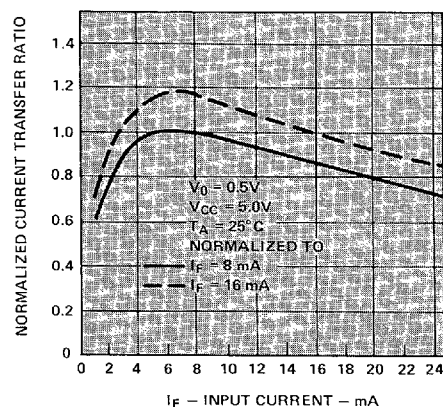


Figure 1. Current Transfer Ratio vs. Input Current

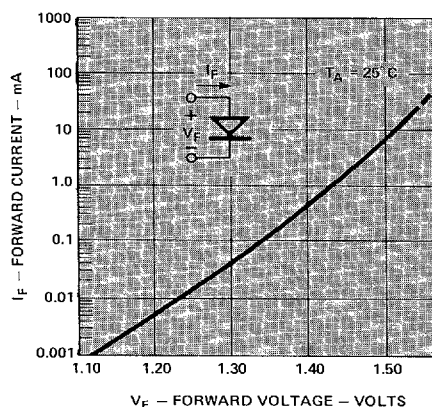


Figure 2. Input Current vs. Forward Voltage

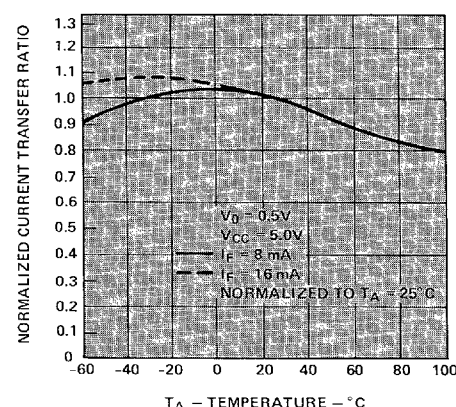


Figure 3. Current Transfer Ratio vs. Temperature

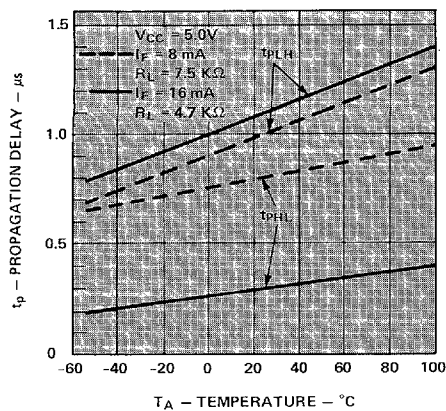


Figure 4. Propagation Delay vs. Temperature

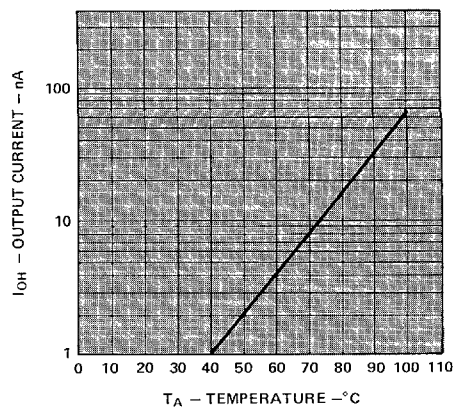


Figure 5. Logic High Output Current vs. Temperature

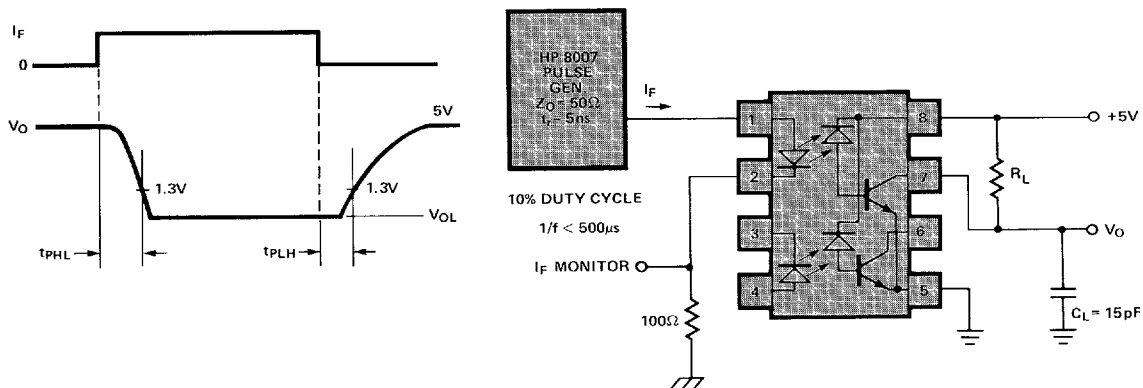


Figure 6. Switching Test Circuit

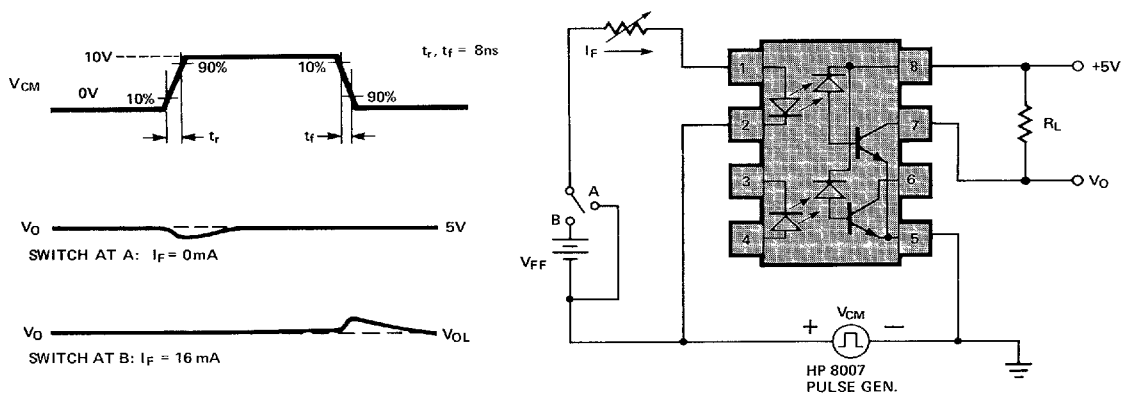


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms

## Recommended Operation

The HCPL-2533 optocoupler is specified for use in LSTTL-to-LSTTL and TTL-to-LSTTL interfaces. The recommended circuits show the interface design and give suggested component values. The input current  $I_F$  is given as both a nominal value and a range. The range in  $I_F$  results from the tolerances in  $V_{CC}$  and the input resistor  $R_{IN}$ . The CTR of the optocoupler

is given as the minimum initial value over temperature, taken directly from the Electrical Specifications. The value given for  $I_{OL}(\min)$  is based on the minimum CTR and the minimum  $I_F$  using worst case values for  $R_L$  and  $V_{CC}$ . The resulting  $I_{OL}(\min)$  has ample design margin, allowing more than 20% for CTR degradation even under these worst case conditions. For additional information on CTR degradation see Application Note 1002.

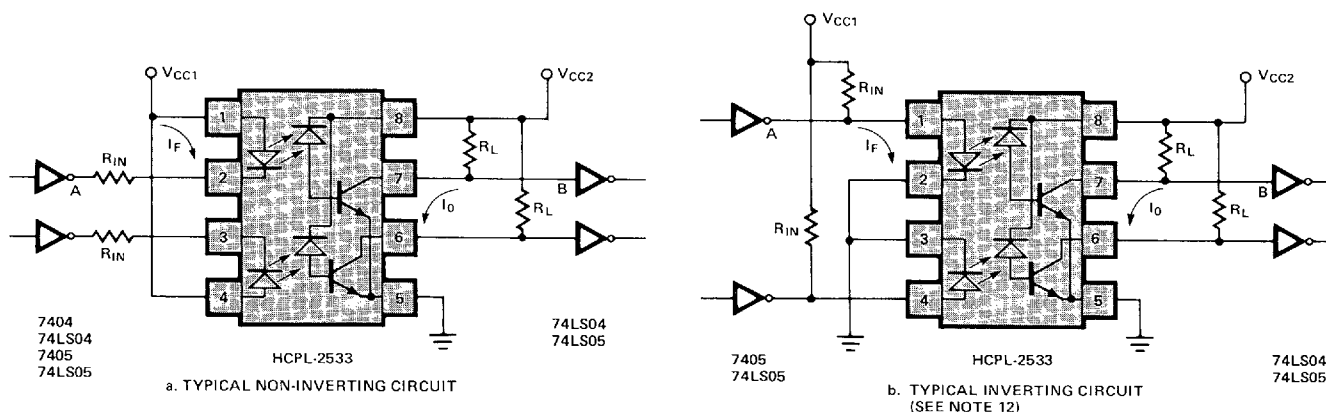


Figure 8. Recommended Circuits

## Recommended Circuit Design Parameters

| Parameter                             | Symbol         | LSTTL to LSTTL | TTL to LSTTL | Units      | Comments                                               | Fig. | Note |
|---------------------------------------|----------------|----------------|--------------|------------|--------------------------------------------------------|------|------|
| <b>INPUT</b>                          |                |                |              |            |                                                        |      |      |
| Logic Low Output Voltage — Input Gate | $V_{OL(A)}$    | 0.5            | 0.4          | V          | Maximum                                                |      |      |
| Supply Voltage — Input                | $V_{CC1}$      | 5.0            | 5.0          | V          | +5%                                                    |      |      |
| Input Resistor                        | $R_{IN}$       | 360            | 180          | $\Omega$   | +5%                                                    | 8a   |      |
|                                       |                | 430            | 200          |            |                                                        | 8b   |      |
| Input Current                         | $I_F$          | 8              | 16           | mA         | Nominal                                                |      |      |
| Input Current Range                   | $I_F$          | 6.75–10        | 14.0–20      | mA         |                                                        | 8a   |      |
|                                       |                |                | 14.5–20      |            |                                                        | 8b   |      |
| <b>OUTPUT</b>                         |                |                |              |            |                                                        |      |      |
| Logic Low Output Voltage — HCPL-2533  | $V_{OL(B)}$    | 0.5            | 0.5          | V          | Maximum                                                |      |      |
| Supply Voltage — Output               | $V_{CC2}$      | 5.0            | 5.0          | V          | +5%                                                    |      |      |
| Pull-Up Resistor                      | $R_L$          | 20             | 8.2          | k $\Omega$ | +5%                                                    |      | 13   |
| Required Current Sink for Logic Low   | $I_{OL}(\max)$ | 0.61           | 1.0          | mA         | Worst Case $V_{CC}$ , $R_L$ , $I_L(B)$                 |      | 14   |
| HCPL-2533 Current Transfer Ratio      | CTR            | 11             | 9            | %          | Minimum $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ |      |      |
| Logic Low Output Current — HCPL-2533  | $I_{OL}(\min)$ | 0.74           | 1.26         | mA         | Worst Case $V_{CC}$ , CTR, $I_F$                       | 8a   | 15   |
|                                       |                |                | 1.30         |            | $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$         | 8b   |      |
| Data Rate                             | $f_D$          | 250            | 250          | Kb/s       | NRZ, $T_A = 25^\circ\text{C}$                          |      | 16   |

### Notes:

- The inverting circuit has higher power consumption and must use open collector gates on the input.
- The load resistor  $R_L$  must be large enough to guarantee logic LOW and small enough to guarantee logic HIGH under worst case conditions:

$$\frac{V_{CC}(\max) - V_{OL}}{I_{OL}(2533) - I_{IL}(B)} \leq R_L \leq \frac{V_{CC}(\min) - V_{IH}(B)}{I_{OH}(2533) - I_{IH}(B)}$$

The selection of  $R_L$  is the same for both inverting and non-inverting circuits.

- The maximum current sink required for logic LOW is:

$$I_{OL}(\max) = I_{IL}(B)(\max) + I_R(\max)$$

where  $I_R$  is the current through  $R_L$ .

- The ratio of  $I_{OL}(\min)$  to  $I_{OL}(\max)$  gives the design margin for CTR degradation. See Application Note 1002.

- The maximum data rate is defined as

$$f_D = \frac{1}{t_{PHL} + t_{PLH}} \text{ bits/second NRZ}$$