HEWLETT PACKARD

High CMR, High Speed TTL Compatible Optocoupler

Technical Data

6N137
HCPL-2601
HCPL-2611

Features

- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-2601: 10,000 V/µs at V_{CM} = 50 V (Typical)
  HCPL-2611: 15,000 V/µs at V_{CM} = 1000 V (Typical)
- **High Speed: 10 MBd Typical**
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature: -40°C to +85°C**
- **Strobable Output**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute and 5000 Vac, 1 Minute (Option 020)**
- **CSA Approved under Component Acceptance Notice No. 5 (File No. LR 88324)**
- **Hermetic Equivalent Device Available (HCPL-5600/1)**

*JEDEC Registered Data (The HCPL-2601 and HCPL-2611 are not registered.)

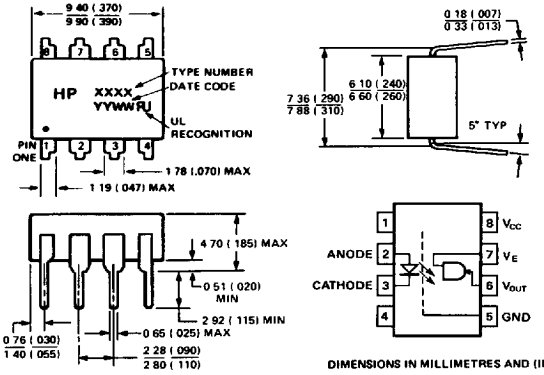
Description

The 6N137/HCPL-2601/11 optically coupled gates combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5000 V/µs for the 2601, and 10,000 V/µs for the 2611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C allowing troublefree system performance.

The 6N137/HCPL-2601/11 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Outline Drawing*



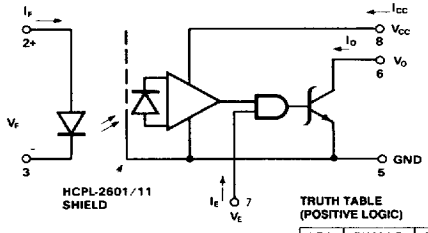
DIMENSIONS IN MILLIMETRES AND (INCHES)

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Applications

- **Isolated Line Receiver**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**

Schematic



USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	H
OFF	NC	H

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	μA
Input Current, High Level	I_{FH}**	5	15	mA
Supply Voltage Power	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (at R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	-40	85	°C

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% CTR degradation guardband.

Absolute Maximum Ratings*

(No Derating Required up to 85°C)
Storage Temperature ..... -55°C to +125°C
Operating Temperature** ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Forward Input Current – I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage – V_{CC} ..... 7 V (1 Minute Maximum)
Enable Input Voltage – V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current – I_O ..... 50 mA
Output Collector Power Dissipation ..... 85 mW
Output Collector Voltage – V_O ..... 7 V
(Selection for higher output voltages up to 20 V is available.)

*JEDEC Registered Data.
**0°C to 70°C on JEDEC Registration.

Electrical Characteristics

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. (See note 1.)

Parameter	Sym.	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA, V_E = 2.0 V	1	14
Low Level Output Voltage	V_{OL}*		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 5, 15	
High Level Supply Current	I_{CCH}		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 0		15
			6.5			V_E = V_{CC}		
Low Level Supply Current	I_{CCL}		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 10 mA		16
			8.5			V_E = V_{CC}		
High Level Enable Current	I_{EH}		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		17
High Level Enable Voltage	V_{EH}	2.0			V			12
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F	1.4	1.5	1.75*	V	T_A = 25°C; I_F = 10 mA	3, 14	
		1.3		1.80				
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 10 mA	14	
Input-Output Insulation	I_{I-O}*			1	µA	45% RH, t = 5 s, V_{I-O} = 3 kVdc, T_A = 25°C		3, 18
	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min		3, 18
OPT 020	V_{ISO}	5000						3, 19
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to +70°C. HP specifies -40°C to +85°C.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75*	ns	T_A = 25°C		6, 7	4
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75*	ns	T_A = 25°C		6, 7	5
					100	ns				
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			3.5	35	ns	R_L = 350 Ω, C_L = 15 pF		9	13
Propagation Delay Skew	t_{PSK}				40	ns				6, 13
Output Rise Time (10-90%)	t_r			24		ns			12	
Output Fall Time (90-10%)	t_f			10		ns			12	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			20		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	8
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	6N137		10,000		V/μs	V_{CM} = 10 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C	13	9, 11, 12
		HCPL-2601	5000	10,000			V_{CM} = 50 V			
		HCPL-2611	10,000	15,000			V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L \rvert$	6N137		10,000		V/μs	V_{CM} = 10 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA T_A = 25°C	13	10, 11, 12
		HCPL-2601	5000	10,000			V_{CM} = 50 V			
		HCPL-2611	10,000	15,000			V_{CM} = 1000 V			

*JEDEC registered data for the 6N137.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Notes:

1. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 16. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
11. For sinusoidal voltages,

$$\left(\frac{\lvert dv_{CM} \rvert}{dt}\right)_{max} = \pi f_{CM} V_{CM}\,(p\text{-}p)$$

OPTO COUPLERS

Notes: (Continued)

12. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
13. See the last 2 pages of this data sheet for more information.
14. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 μA. HP guarantees a maximum I_{OH} of 100 μA.
15. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. HP guarantees a maximum I_{CCH} of 10 mA.
16. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. HP guarantees a maximum I_{CCL} of 13 mA.
17. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of −2.0 mA. HP guarantees a maximum I_{EL} of −1.6 mA.
18. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for one second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
19. In accordance with UL 1577, each option 020 optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for one second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

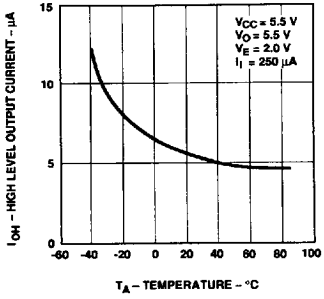


Figure 1. High Level Output Current vs. Temperature.

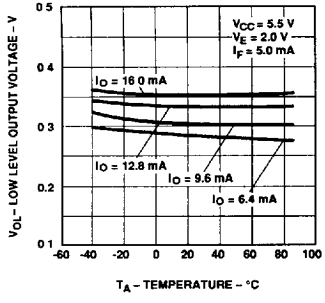


Figure 2. Low Level Output Voltage vs. Temperature.

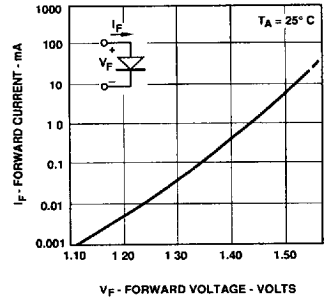


Figure 3. Input Diode Forward Characteristic.

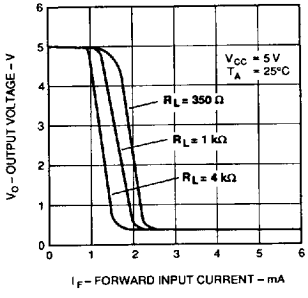


Figure 4. Output Voltage vs. Forward Input Current.

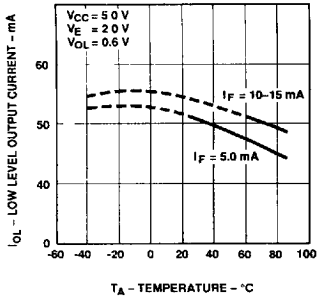


Figure 5. Low Level Output Current vs. Temperature.

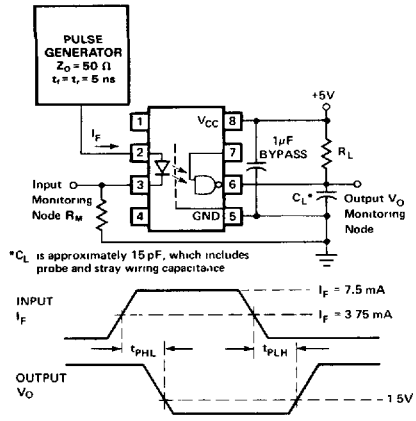


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.****

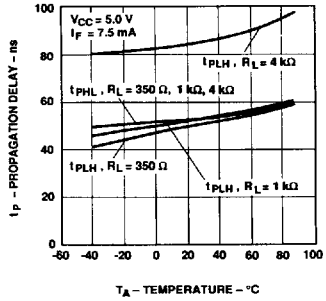


Figure 7. Propagation Delay vs. Temperature.

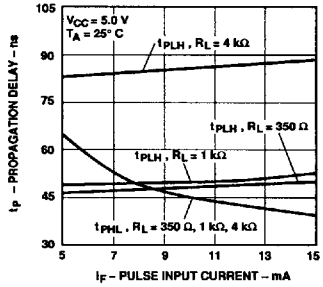


Figure 8. Propagation Delay vs. Pulse Input Current.

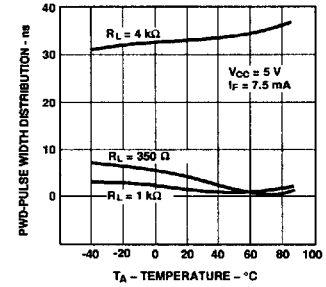


Figure 9. Pulse Width Distortion vs. Temperature.

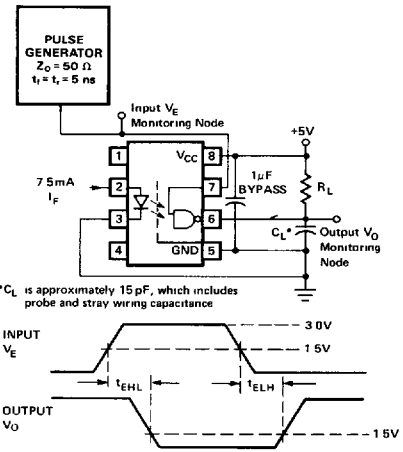


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

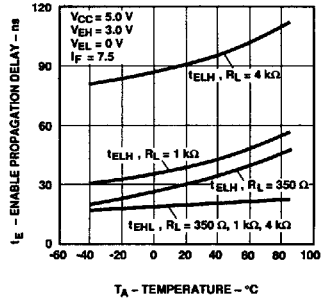


Figure 11. Enable Propagation Delay vs. Temperature.

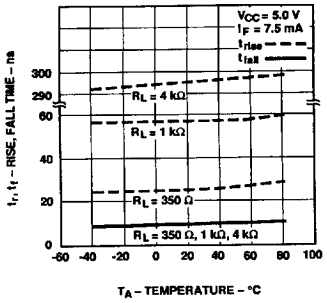


Figure 12. Rise and Fall Time vs. Temperature.

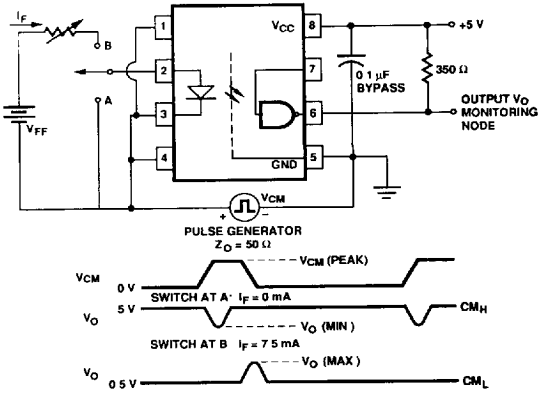


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

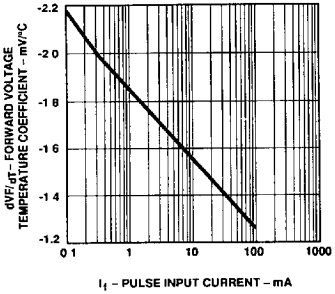


Figure 14. Temperature Coefficient for Forward Voltage vs. Input Current.

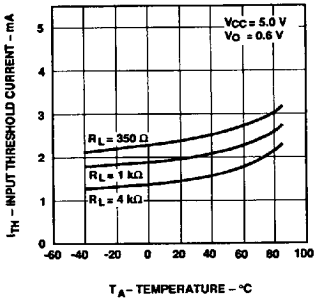


Figure 15. Input Threshold Current vs. Temperature.

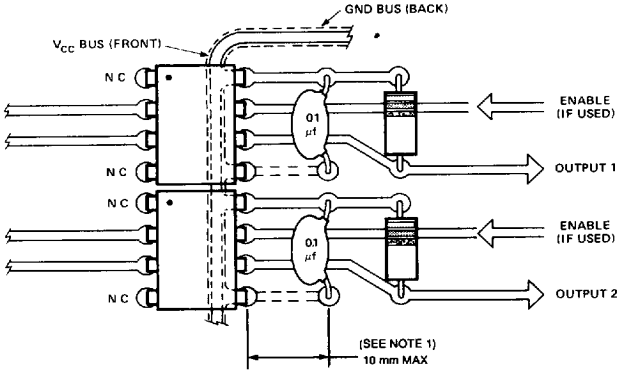


Figure 16. Recommended Printed Circuit Board Layout.

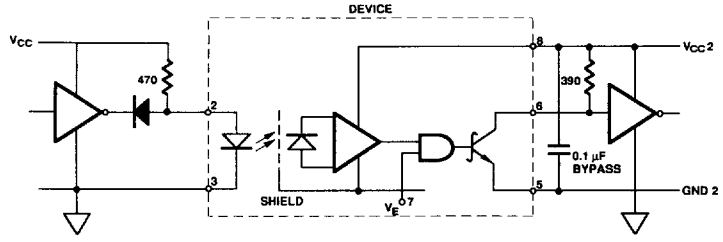


Figure 17. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232. RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PLH}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 18, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 19 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 19 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{psk} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulsewidth distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

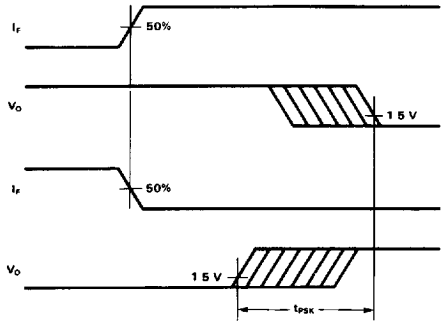


Figure 18. Illustration of Propagation Delay Skew—t_{PSK}.

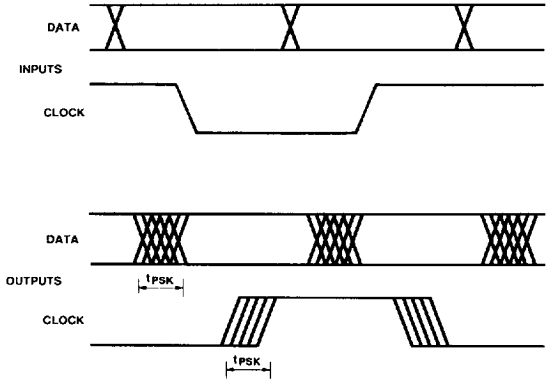


Figure 19. Parallel Data Transmission Example.