HEWLETT® PACKARD

Dual Channel, High Speed Optocouplers 8 Pin DIP and SOIC-8

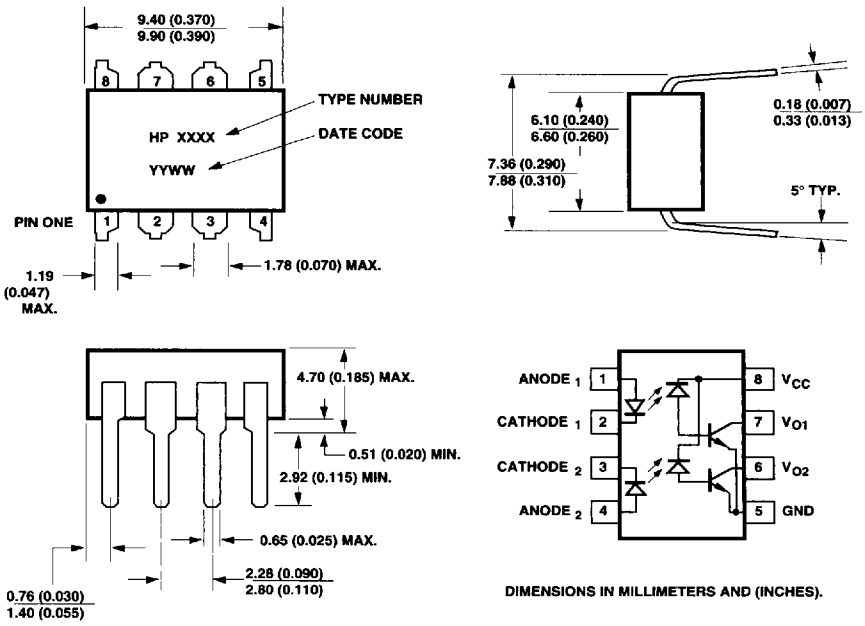
Technical Data

HCPL-2530 HCPL-0530
HCPL-2531 HCPL-0531
HCPL-4534 HCPL-0534

Features

- **Available in 8 Pin DIP and SOIC-8 packages**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Very High Common Mode Transient Immunity: 15000 V/μs @ V_{CM} = 1500 V (HCPL-4534/0534)**
- **High Density Packaging**
- **3 MHz Bandwidth**
- **Open Collector Outputs**
- **Recognized Under the Component Program of UL1577 (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 V_{rms}, 1 Minute**
- **5000 V_{rms}, 1 Minute (Option 020) (HCPL-2530/2531/4534)**
- **CSA Approved Under Component Acceptance Notice No. 5 (File No. CA88324) (HCPL-2530/2531/4534)**
- **MIL-STD-1772 Version Available (HCPL-5530/31)**
- **Surface Mount Gull Wing Option Available for 8 Pin DIP (Option 300)**

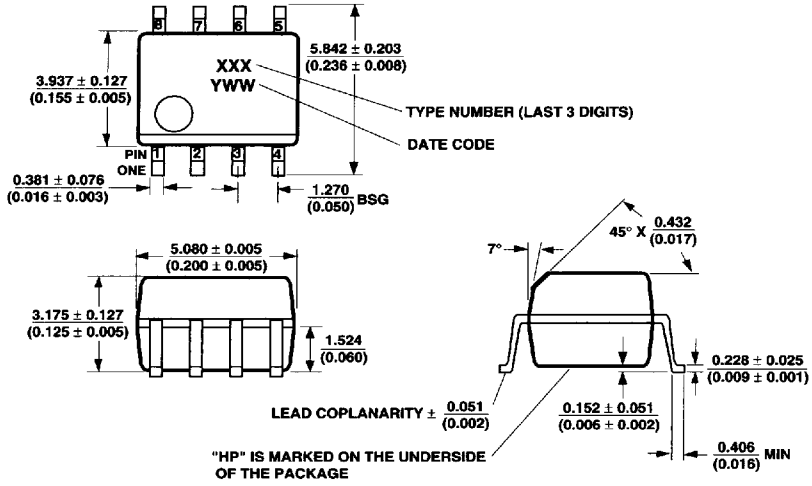
Outline Drawing - 8 Pin DIP



DIMENSIONS IN MILLIMETERS AND (INCHES).

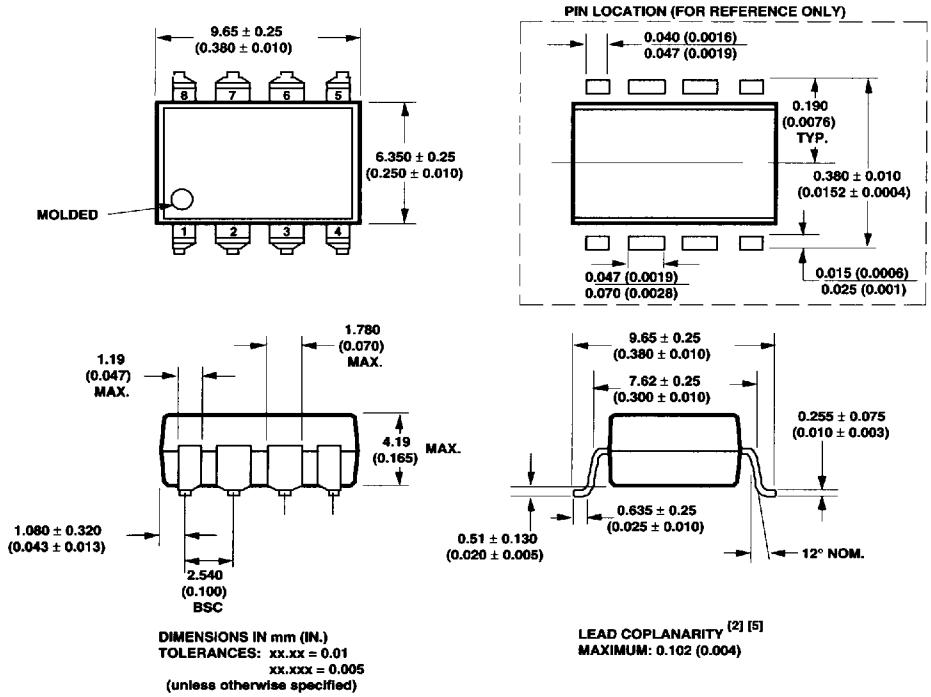
CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Outline Drawing - SO-8



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline Drawing - Option 300



DIMENSIONS IN mm (IN.)
TOLERANCES: xx.xx = 0.01
xx.xxx = 0.005
(unless otherwise specified)

LEAD COPLANARITY [2] [5]
MAXIMUM: 0.102 (0.004)

Description

These dual channel optocouplers contain a pair of light emitting diodes and integrated photo detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

These dual channel optocouplers are available in an 8 Pin DIP and in an industry standard SOIC-8 package. The following is a cross reference table listing the 8 Pin DIP part number and the electrically equivalent SOIC-8 part number.

8 Pin DIP	SOIC-8 Package
HCPL-2530	HCPL-0530
HCPL-2531	HCPL-0531
HCPL-4534	HCPL-0534

The SOIC-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCPL-2530/0530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the HCPL-2530/0530 is 7% minimum at I_F = 16 mA.

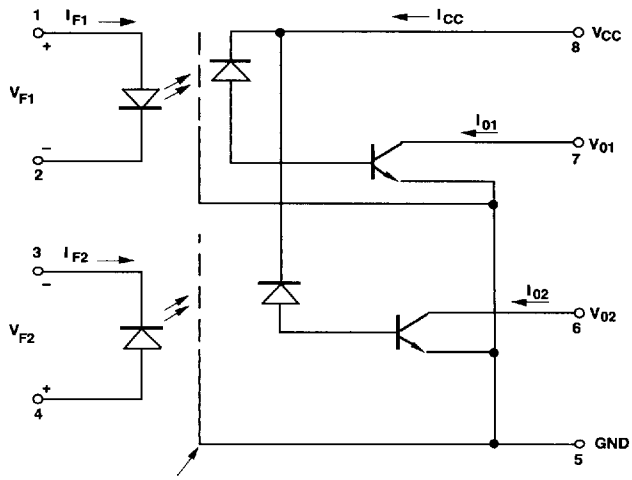
The HCPL-2531/0531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the HCPL-2531/0531 is 19% minimum at I_F = 16 mA.

The HCPL-4534/0534 is an HCPL-2531/0531 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 V guaranteed.

Applications

- **Line Receivers** – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

Schematic

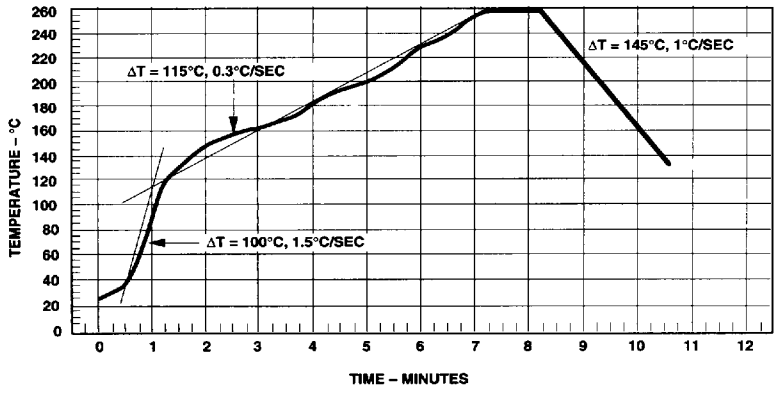


USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 9.)

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to +100°C
Lead Solder Temperature (8 Pin DIP) .....260°C for 10 s
(1.6 mm below seating plane)
Average Input Current – I_F (each channel) .....25 mA
Peak Input Current – I_F (each channel) .....50 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F (each channel) .....1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R (each channel) ..... 5 V
Input Power Dissipation (each channel).....45 mW
Average Output Current – I_O (each channel).....8 mA
Peak Output Current – I_O (each channel) .....16 mA
Supply Voltage – V_{CC} (Pin 8-5)..... -0.5 V to 30 V
Output Voltage – V_O (Pin 7, 6-5) .....-0.5 V to 20 V
Output Power Dissipation (each channel) .....35 mW[13]
Infrared and Vapor Phase
Reflow Temperature .....See Thermal Profile
(SOIC-8 & Option 300)

Thermal Profile



Maximum Solder Reflow Thermal Profile. (Note: Use of non-chlorine activated fluxes is highly recommended.)

Electrical Specifications

Over recommended temperature (T_A=0°C to 70°C) unless otherwise specified. See note 9.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	HCPL-2530/ 0530	7	18	50	%	T_A=25°C		I_F=16 mA, V_{CC}=4.5V V_O=0.5 V	1, 2 4	1, 2
			5								
		HCPL-2531/ 0531 HCPL-4534/ 0534	19	24	50	%	T_A=25°C				
			15								
Logic Low Output Voltage	V_{OL}	HCPL-2530/ 0530		0.1	0.5	V	T_A=25°C	I_O=1.1 mA	I_F=16 mA, V_{CC}=4.5V	1	1
					0.5			I_O=0.8 mA			
		HCPL-2531/ 0531 HCPL-4534/ 0534		0.1	0.5	V	T_A=25°C	I_O=3.0 mA			
					0.5			I_O=2.4 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A=25°C	V_O= Open V_{CC}=5.5 V	I_F=0 mA	6	1
					50			V_O= Open V_{CC}=15.0 V			
Logic Low Supply Current	I_{CCL}			100	400	µA	I_F=16 mA, V_O=Open, V_{CC}=15 V				
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_F=0 mA, V_O=Open, V_{CC}=15 V				
Input Forward Voltage	V_F			1.5	1.7	V	T_A=25°C	I_F=16 mA		3	1
					1.8						
Input Reverse Breakdown Voltage	BV_R		5			V	I_R=10 µA				1

Electrical Specifications (cont'd.)

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F=16 mA		
Input Capacitance	C_{IN}			60		pF	f=1 MHz, V_F=0 V		1
Input-Output Insulation Voltage	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t=1 min., T_A=25°C		3, 10
Opt. 020	V_{ISO}	HCPL-2530/ 2531/4534	5000						3, 11
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	RH ≤ 45% V_{I-O}=500 Vdc, t=5 s		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f=1 MHz		12
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	RH ≤ 45%, t=5 s V_{I-I}=500 Vdc		4
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω			4
Capacitance (Input-Input)	C_{I-I}	HCPL-2530/ 2531/4534		0.03		pF	f=1 MHz		4
		HCPL-0530/ 0531/0534		0.25					

*All typicals at 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2530/ 0530		0.2	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	6, 7
					2.0					
		2531/ 0531/ 4534/ 0534		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	2530/ 0530		1.3	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	6, 7
					2.0					
		2531/ 0531/ 4534/ 0534		0.6	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	2530/ 0530	1	10		kV/µs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	5, 6, 7
		2531/ 0531	1	10			R_L = 1.9 kΩ			
		4534/ 0534	15	30			R_L = 1.9 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	2530/ 0530	1	10		kV/µs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{P-P}	10	5, 6, 7
		2531/ 0531	1	10			R_L = 1.9 kΩ			
		4534/ 0534	15	30			R_L = 1.9 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{P-P}		
Bandwidth	BW			3		MHz	R_L = 100 Ω		7, 8	

Insulation Related Specifications

Parameter	Symbol	DIP Value	SOIC-8 Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥7	≥4	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥7	≥4	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	200	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0110)		IIIa	IIIa		Material group (DIN VDE 0110)

Notes:
1. Each channel.
2. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
5. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
6. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
7. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and the 6.1 kΩ pull-up resistor.
8. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
9. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
12. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
13. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C for the SOIC-8 package.

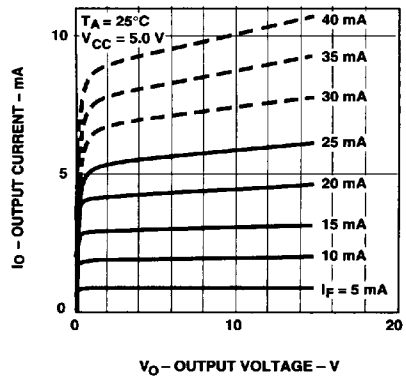


Figure 1. DC and Pulsed Transfer Characteristics.

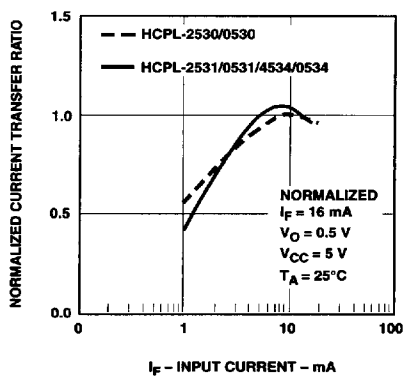


Figure 2. Current Transfer Ratio vs. Input Current.

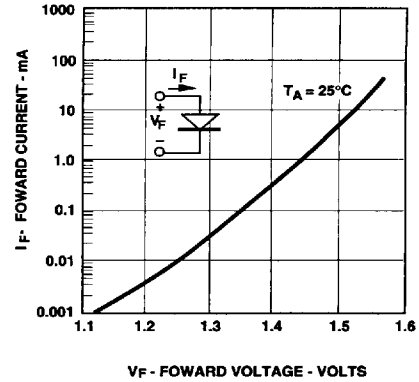


Figure 3. Input Current vs. Forward Voltage.

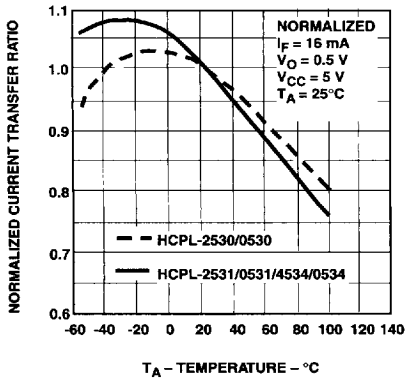


Figure 4. Current Transfer Ratio vs. Temperature.

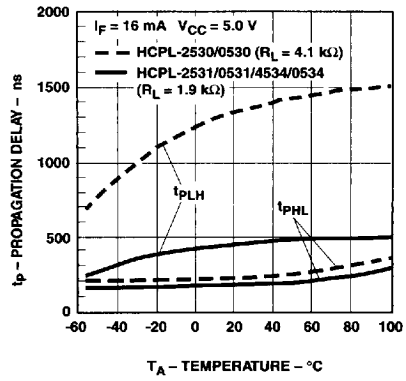


Figure 5. Propagation Delay vs. Temperature.

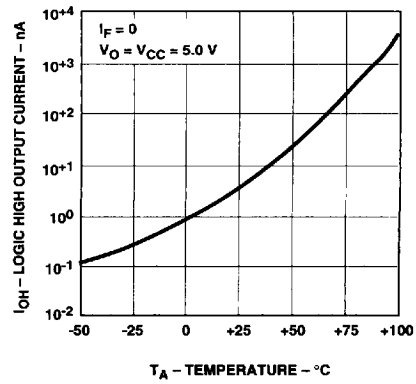


Figure 6. Logic High Output Current vs. Temperature.

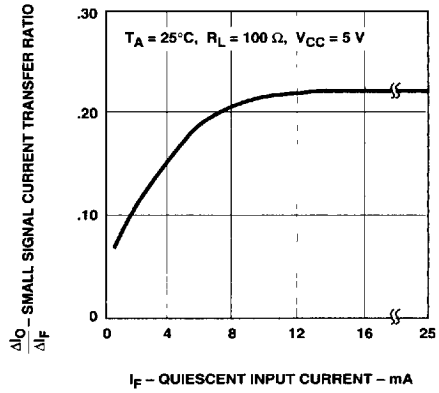


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

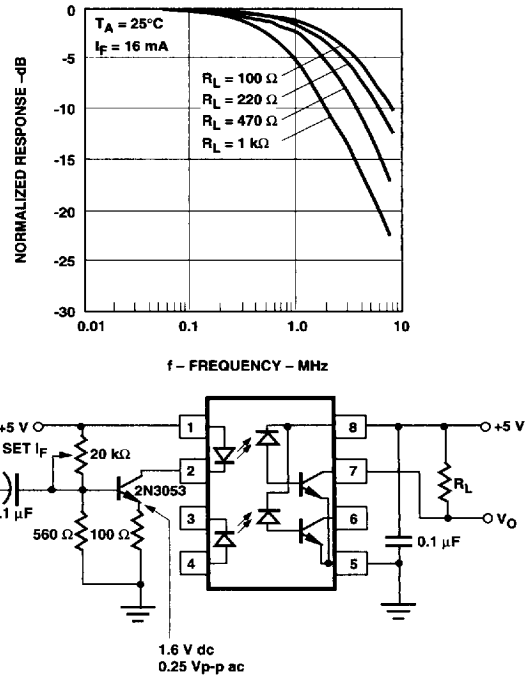


Figure 8. Frequency Response.

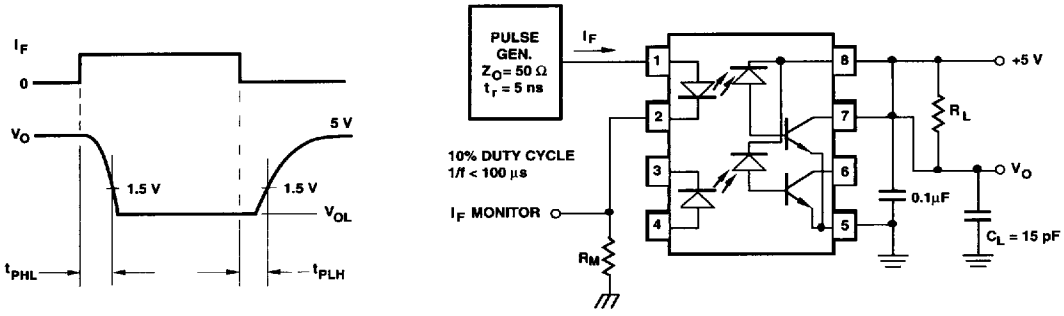


Figure 9. Switching Test Circuit.

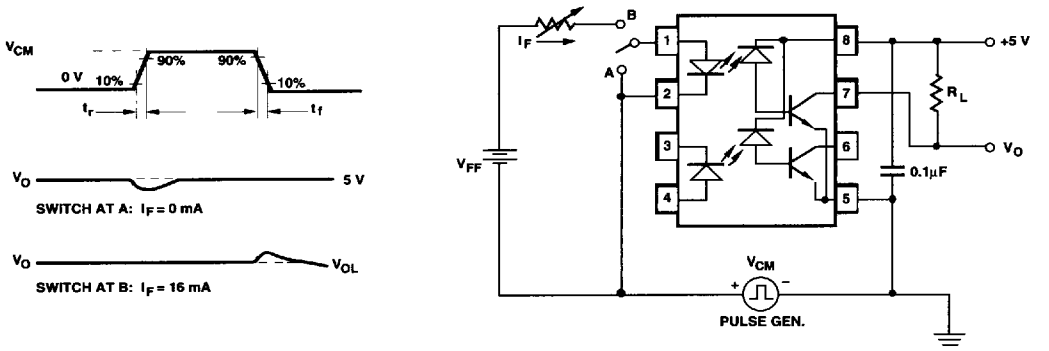


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

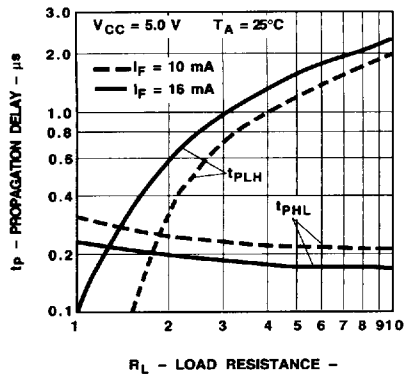


Figure 11. Propagation Delay Time vs. Load Resistance.

For more information:

United States: call your local HP sales office listed in your telephone directory. Ask for a Components representative.

Canada: (416) 206-4725

Europe: (49) 7031/14-0

Asia Pacific/Australia: (65) 290-6360

Japan: (81 3) 3331-6111

Obsoletes 5091-0587E (1/91)
Printed in U.S.A. 5091-9122E (12/93)