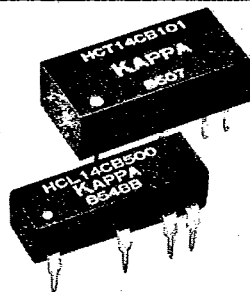


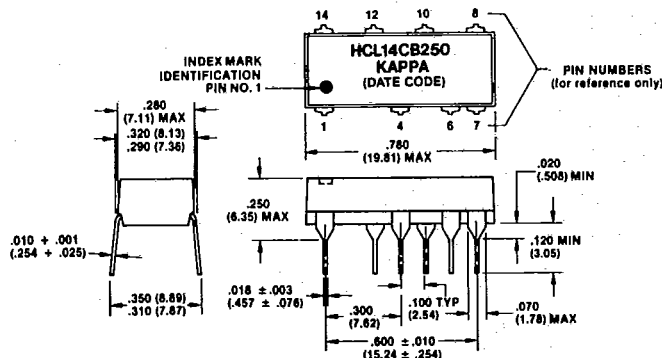
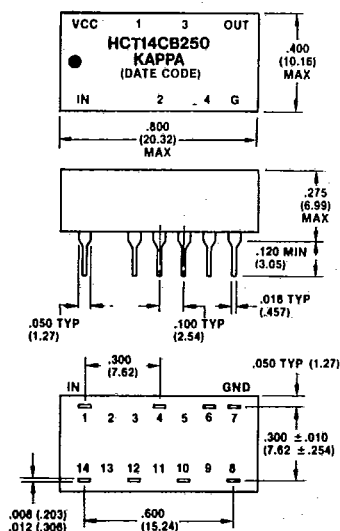
SERIES HCL14/HCT14 (14-PIN) 5-TAP HCMOS DELAY LINES



FEATURES

- HCMOS logic interfaced
- Delays from 50 to 500 ns
- 5 equally-spaced taps
- Available in auto-insertable (HCL14) and standard (HCT14) packages
- Drives up to 10 LS TTL loads
- Compatible with standard LS TTL family

MARKINGS AND DIMENSIONS, in (mm)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC} Supply Voltage		4V	4	5	6	V
V _{IH} High-Level Input Voltage		5V	1.5			V
		6V	4.2			
V _{IL} Low-Level Input Voltage		4V	0		0.3	V
		5V	0		0.9	
		6V	0		1.2	
V _I Input Voltage			0		V _{CC}	V
V _O Output Voltage			0		V _{CC}	V
I _{IK} Input Diode Current	V _I < 0 or V _I > V _{CC}				±20	mA
I _{OK} Output Diode Current	V _O < 0 or V _O > V _{CC}				±20	mA
I _O Continuous Output Current	V _O = 0 to V _{CC}				±25	mA
T _A Operating Free-Air Temperature			-40	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS

V _{OH} High-Level Output Voltage	V _I = V _{IH} or V _{IL} , I _{OH} = -20μA	4V	1.9			
		5V	4.4			
		6V	5.9			
		5V	3.84			V
		6V	5.34			
I _{OH} High-Level Output Current	V _I = V _{IH} or V _{IL} , I _{OH} = 4mA	4V			5	μA
	V _I = V _{IH} or V _{IL} , I _{OH} = 5.2mA	5V			0.1	
	V _I = V _{IH} or V _{IL} , V _O = V _{CC}	6V			0.1	
V _{OL} Low-Level Output Voltage	V _I = V _{IH} or V _{IL} , I _{OL} = 20μA	4V			0.1	V
		5V			0.4	
		6V			0.4	
		5V			±1.0	μA
I _I Input Current	V _I = V _{CC} or 0, I _O = 0	6V			10	mA
I _{CC} Supply Current	V _O = V _{OL} to V _{OH} , V _{CC} = min-to-max	6V			10	LS
N Fanout					10	TTL

INPUT PULSE TEST CONDITIONS

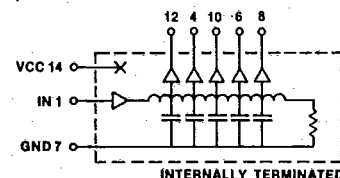
E _{IN} Pulse Voltage		3.1	3.2	3.3	V
T _{RI} Pulse Risettime				2.0	ns
T _W Pulse Width, in % of Total Delay Time		100			%
d Duty Cycle			33.3	50	%

AC ELECTRICAL CHARACTERISTICS

T _{PLH} Low-to-High Level Delay Time	V _{CC} = T _{YP} , T _A = T _{YP} , E _{IN} = T _{YP} , T _W = min, d = T _{YP} (1) (2) (4)		-5	+5	%
T _{RO} Output Risettime	V _{CC} = T _{YP} , T _A = T _{YP} , E _{IN} = T _{YP} , T _W = min, d = T _{YP} (3) (4)			8	ns

Notes:

1. Delays measured at 1.5V level on leading edge only.
2. Delay tolerances: ±5% or ±2 ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: V_{CC} = T_{YP}, T_A = T_{YP}, E_{IN} = T_{YP}, T_{RI} = max, T_W = min, P_{RR} = 1MHz (or d/t_W, whichever is less), R_L 1 megohm and C_L 2pf.
3. Risettime measured from 0.75V to 2.4V level.
4. Measured with no load on delay taps.
5. Other delays also available upon request.



KAPPA[®]

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