005520

5520 HP

HEWLETT PACKARD

GENERAL PURPOSE MOTION CONTROL IC

995 975

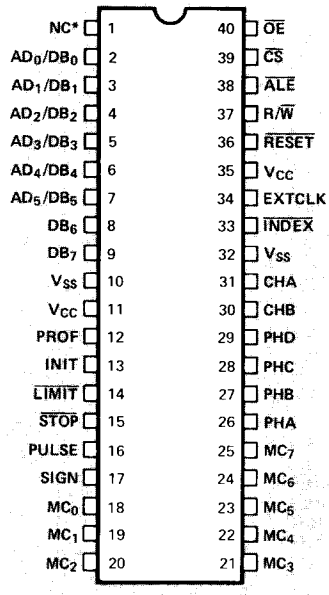
HCTL-1000

TECHNICAL DATA NOVEMBER 1985

Features

NEW

- DC, DC BRUSHLESS AND STEPPER MOTOR CONTROL
- POSITION CONTROL
- VELOCITY CONTROL
- PROGRAMMABLE VELOCITY PROFILING
- PROGRAMMABLE DIGITAL FILTER
- PROGRAMMABLE COMMUTATOR
- PROGRAMMABLE PHASE OVERLAP
- PROGRAMMABLE PHASE ADVANCE
- GENERAL 8 BIT PARALLEL I/O PORT
- 8 BIT PARALLEL MOTOR COMMAND PORT
- PWM MOTOR COMMAND PORT
- QUADRATURE DECODER FOR ENCODER SIGNALS
- 24 BIT POSITION COUNTER
- SINGLE 5V POWER SUPPLY
- TTL COMPATIBLE
- 1 OR 2 MHz CLOCK OPERATION



*Should be left floating

PINOUT

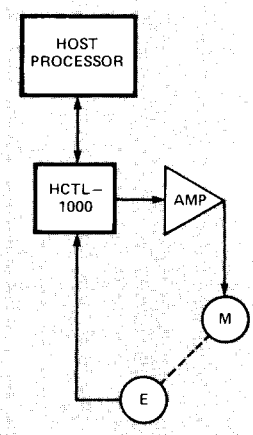
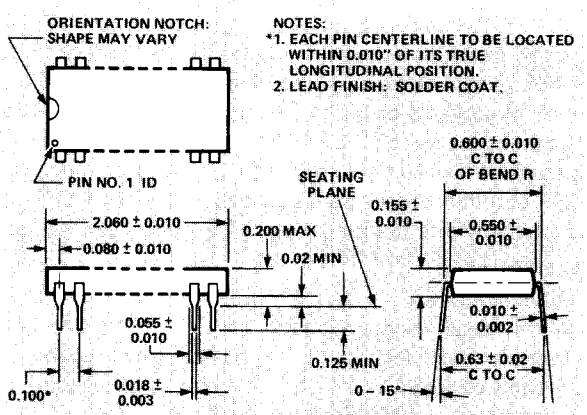


Figure 1. System Block Diagram

General Description

The HCTL-1000 is a high performance, general purpose motion control IC fabricated in Hewlett-Packard NMOS technology. It performs all the time-intensive tasks of digital motion control, thereby freeing the host processor for other tasks. The simple programmability of all control parameters provides the user with maximum flexibility and quick design of control systems with a minimum number of components. All that is needed for a complete servo system is a host processor to specify commands, an amplifier and motor with an incremental encoder. No analog compensation or velocity feedback is necessary (see Figure 1).

Package Dimensions



40-PIN PLASTIC DUAL-IN-LINE PACKAGE

Table of Contents

ESD WARNING: Since this is an NMOS device, normal precautions should be taken to avoid static damage.

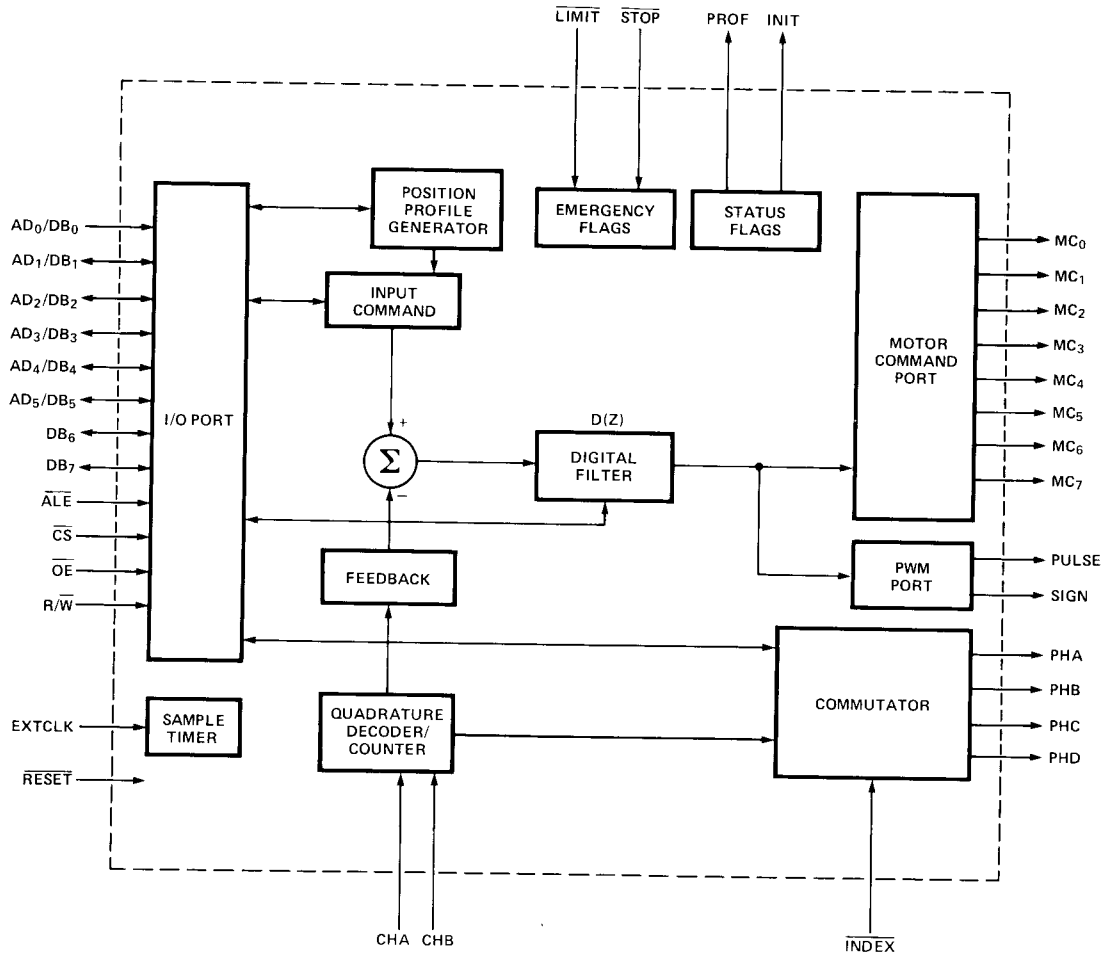


Figure 2. Internal Block Diagram

Introduction

The purpose of this section is to describe the organization of this data sheet. The front page includes the key features of the HCTL-1000, a general description of the part, the mechanical drawing and pin-out, and a Table of Contents. Following this section is the Theory of Operation, which gives the user a brief overview of how the HCTL-1000 operates by describing the internal block diagram shown in Figure 2. The following five sections give the specifications of the HCTL-1000, including Absolute Maximum Ratings, DC Characteristics, AC Characteristics, Timing Diagrams, and Functional Pin Descriptions. The final two sections include the detailed information on how to operate and interface to the HCTL-1000. The How to Operate section discusses the function and address of each software register, and describes how to use the four position and velocity control modes and the electronic commutator. The How to Interface section describes how to interface the HCTL-1000 to a microprocessor, an encoder, and an amplfier.

Theory of Operation

The HCTL-1000 is a general purpose motor controller which provides position and velocity control for dc, dc brushless and stepper motors. The internal block diagram of the HCTL-1000 is shown in Figure 2. The HCTL-1000 receives its input commands from a host processor and position feedback from an incremental encoder with quadrature output. An 8-bit bidirectional multiplexed address/data bus interfaces the HCTL-1000 to the host processor. The encoder feedback is decoded into quadrature counts and a 24-bit counter keeps track of position. The HCTL-1000 executes any one of four control algorithms selected by the user. The four control modes are:

- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control for point to point moves
- Integral Velocity Control with continuous velocity profiling using linear acceleration

The resident Position Profile Generator calculates the necessary profiles for Trapezoidal Profile Control and Integral Velocity Contol. The HCTL-1000 compares the desired position (or velocity) to the actual position (or velocity) to compute compensated motor commands using a programmable digital filter D(z). The motor command is externally available at the Motor Command Port as an 8-bit byte and at the PWM Port as a Pulse Width Modulated (PWM) signal.

The HCTL-1000 has the capability of providing electronic commutation for dc brushless and stepper motors. Using the encoder position information, the motor phases are enabled in the correct sequence. The commutator is fully programmable to encompass most motor encoder combinations. In addition, phase overlap and phase advance can be programmed to improve torque ripple and high speed performance. The HCTL-1000 contains a number of flags including two externally available flags, Profile and Initialization, which allow the user to see or check the status of the controller. It also has two emergency flags, $\overline{\text{Limit}}$ and $\overline{\text{Stop}}$, which allow operation of the HCTL-1000 to be interrupted under emergency conditions.

The HCTL-1000 controller is a digitally sampled data system. While information from the host processor is accepted asynchronously with respect to the control functions, the motor command is computed on a discrete sample time basis. The sample timer is programmable.

Absolute Maximum Ratings

Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −40°C to +125°C
Supply Voltage ..... −0.3 V to 7 V
Input Voltage ..... −0.3 V to 7 V
Maximum Power Dissipation ..... 0.95 W
Maximum Clock Frequency ..... 2 MHz

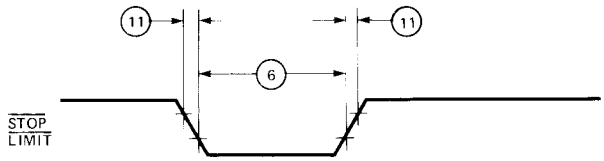
D.C. Characteristics T_a = 0°C to +70°C; V_{CC} = 5 V ± 5%; V_{SS} = 0 V

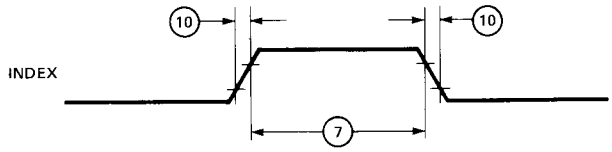
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Power Supply	V_{CC}	4.75	5.00	5.25	V	
Supply Current	I_{CC}		80	180	mA	
Input Leakage Current	I_{il}			10	μA	V_{in} = 5.25 V
Tristate Output Leakage Current	I_{loh}			±10	μA	V_{out} = −0.3 to 5.25 V
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}	−0.3		0.4	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −200 μA
Power Dissipation	P_D		400	950	mW	
Input Capacitance	C_{in}			20	pF	T_a = 25° C, f = 1 MHz unmeasured pins returned to ground
Output Capacitance Load	C_{out}		100		pF	Same as above

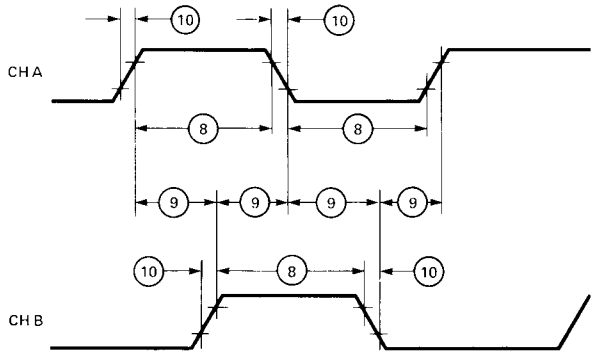
A.C. Electrical Specifications T_a = 0 to 70°C; V_{CC} = 5.0 V ± 5%; Units = nsec

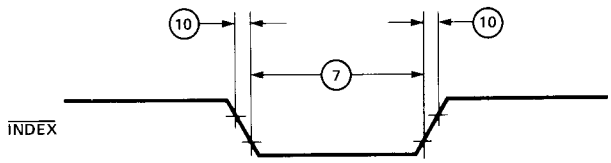
ID#	Signal	Symbol	Clock Frequency			
			2 MHz		1 MHz	
			Min.	Max.	Min.	Max.
1	Clock Period	t_{CPER}	500		1000	
2	Pulse Width, Clock High	t_{CPWH}	230		300	
3	Pulse Width, Clock Low	t_{CPWL}	200		200	
4	Clock Rise and Fall Time	t_{CR}		50		50
5	Input Pulse Width $\overline{\text{Reset}}$	t_{IRST}	2500		5000	
6	Input Pulse Width $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IP}	600		1100	
7	Input Pulse Width $\overline{\text{Index}}$, Index	t_{IX}	1600		3100	
8	Input Pulse Width CHA, CHB	t_{IAB}	1600		3100	
9	Delay CHA to CHB Transition	t_{AB}	600		1100	
10	Input Rise/Fall Time CHA, CHB, Index	t_{IABR}		450		900
11	Input Rise/Fall Time $\overline{\text{Reset}}$, $\overline{\text{ALE}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$, $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IR}		50		50
12	Input Pulse Width $\overline{\text{ALE}}$, $\overline{\text{CS}}$	t_{IPW}	80		80	
13	Delay Time, $\overline{\text{ALE}}$ Fall to $\overline{\text{CS}}$ Fall	t_{AC}	50		50	
14	Delay Time, $\overline{\text{ALE}}$ Rise to $\overline{\text{CS}}$ Rise	t_{CA}	50		50	
15	Address Set Up Time Before $\overline{\text{ALE}}$ Rise	t_{ASR1}	20		20	
16	Address Set Up Time Before $\overline{\text{CS}}$ Fall	t_{ASR}	20		20	
17	Write Data Set Up Time Before $\overline{\text{CS}}$ Rise	t_{DSR}	20		20	
18	Address/Data Hold Time	t_H	20		20	
19	Set Up Time, R/$\overline{\text{W}}$ Before $\overline{\text{CS}}$ Rise	t_{WCS}	20		20	
20	Hold Time, R/$\overline{\text{W}}$ After $\overline{\text{CS}}$ Rise	t_{WH}	20		20	
21	Delay Time, Write Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSAL}	1700		3400	
22	Delay Time, Read/Write, $\overline{\text{CS}}$ Rise to $\overline{\text{CS}}$ Fall	t_{CSCS}	1500		3000	
23	Write Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall	t_{WC}	1830		3530	
24	Delay time, $\overline{\text{CS}}$ Rise to $\overline{\text{OE}}$ Fall	t_{CSOE}	1700		3200	
25	Delay Time, $\overline{\text{OE}}$ Fall to Data Bus Valid	t_{OEDB}	100		100	
26	Delay Time, $\overline{\text{CS}}$ Rise to Data Bus Valid	t_{CSDB}	1800		3300	
27	Input Pulse Width $\overline{\text{OE}}$	t_{IPWOE}	100		100	
28	Hold Time, Data Held After $\overline{\text{OE}}$ Rise	t_{DOEH}	20		20	
29	Delay Time, Read Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSALR}	1820		3320	
30	Read Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall	t_{RC}	1950		3450	
31	Output Pulse Width, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OF}	500		1000	
32	Output Rise/Fall Time, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OR}	20	150	20	150
33	Delay Time, Clock Rise to Output Rise	t_{EP}	20	300	20	300
34	Delay Time, $\overline{\text{CS}}$ Rising to MC Port Valid	t_{CSMC}		1600		3200

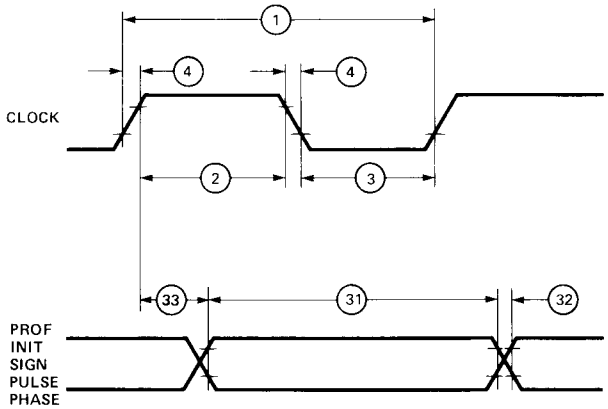
HCTL-1000 I/O Timing Diagrams

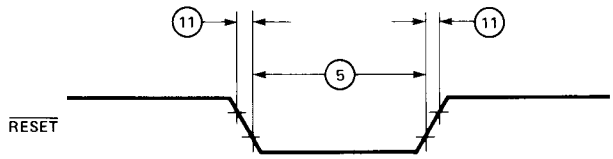










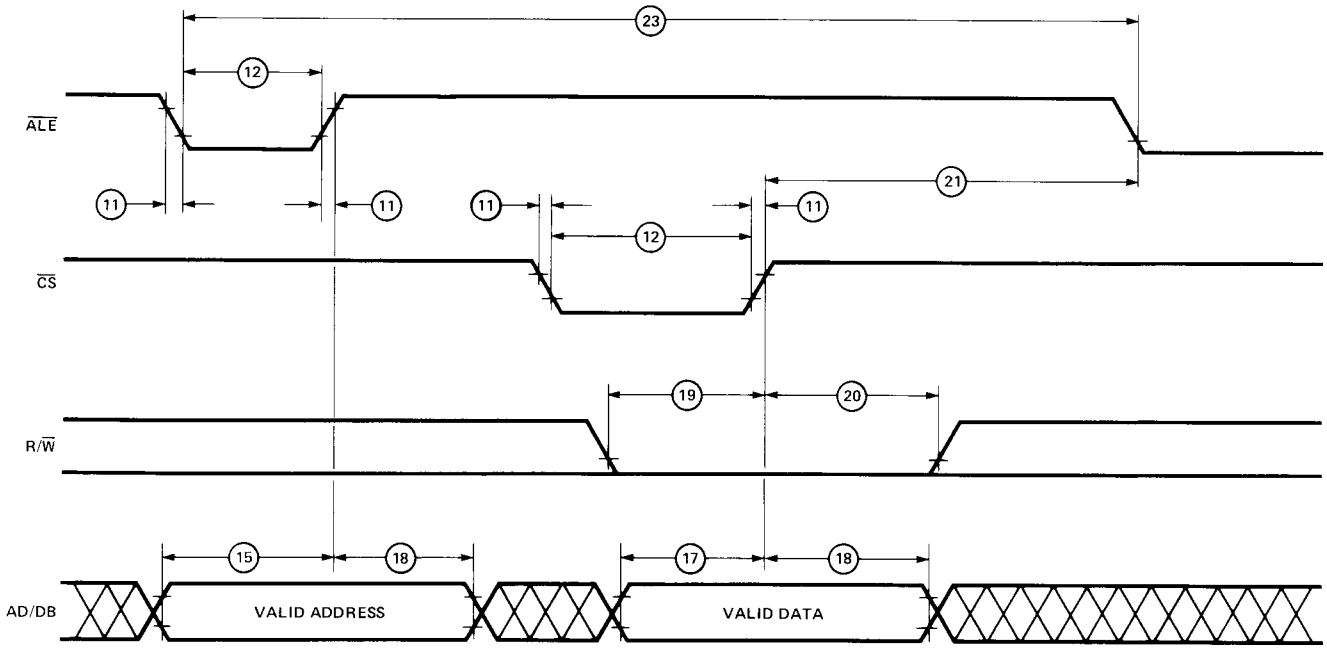


HCTL-1000 I/O Timing Diagrams

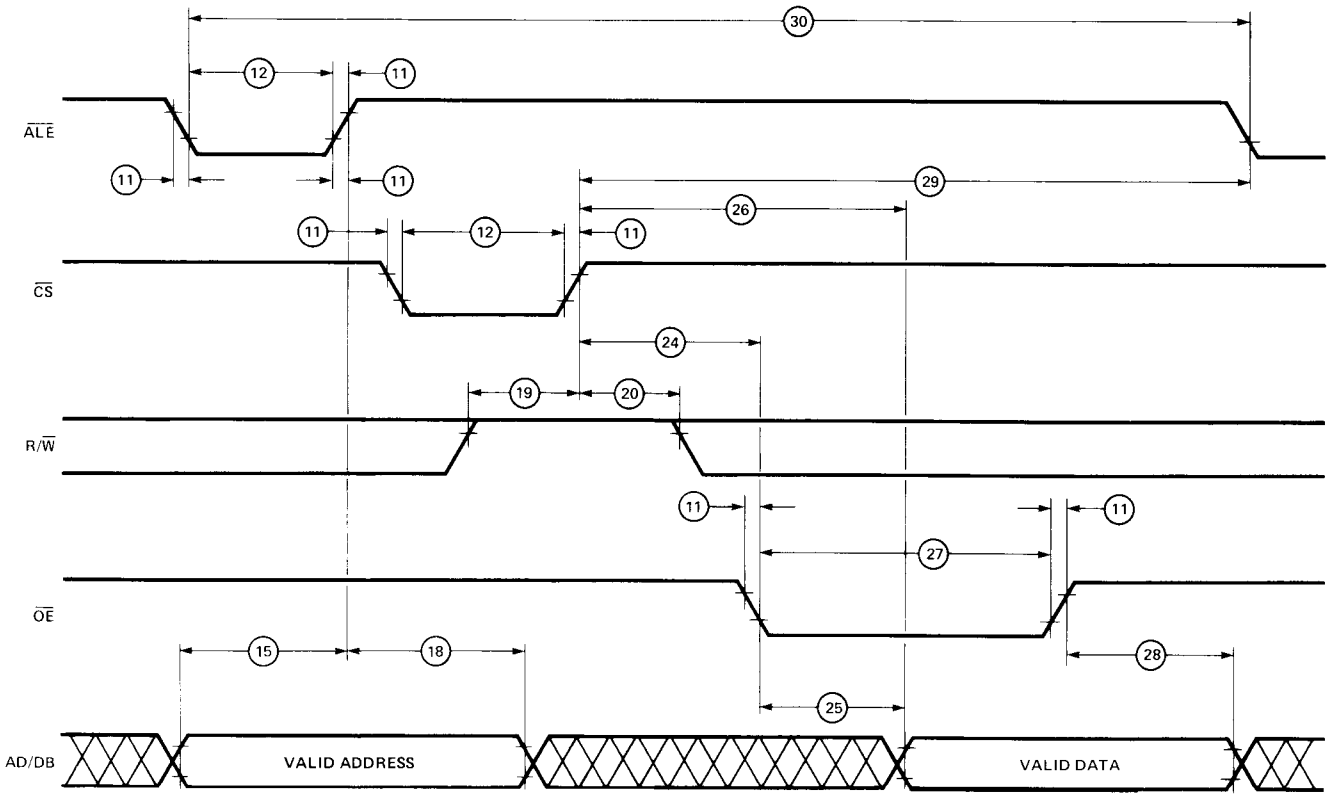
There are three different timing configurations which can be used to give the user flexibility to interface the HCTL-1000 to most microprocesors. See the I/O interface section for more details.

I. $\overline{ALE}/\overline{CS}$ NON OVERLAPPED

A. Write Cycle



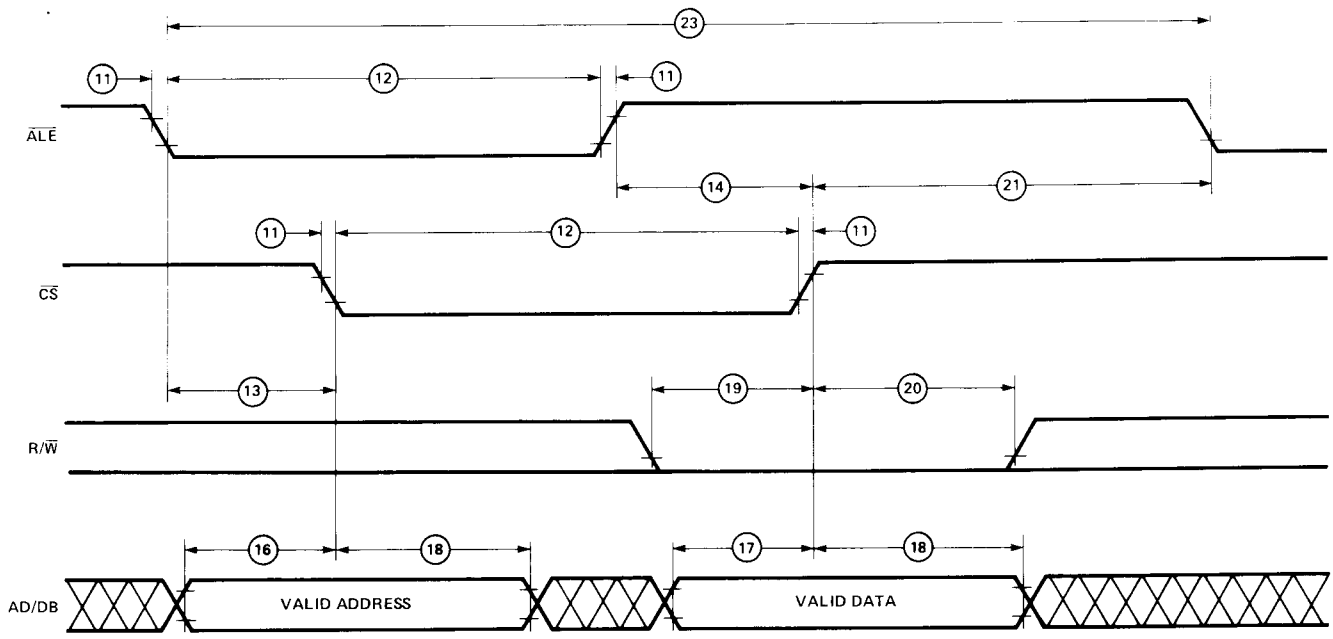
B. Read Cycle



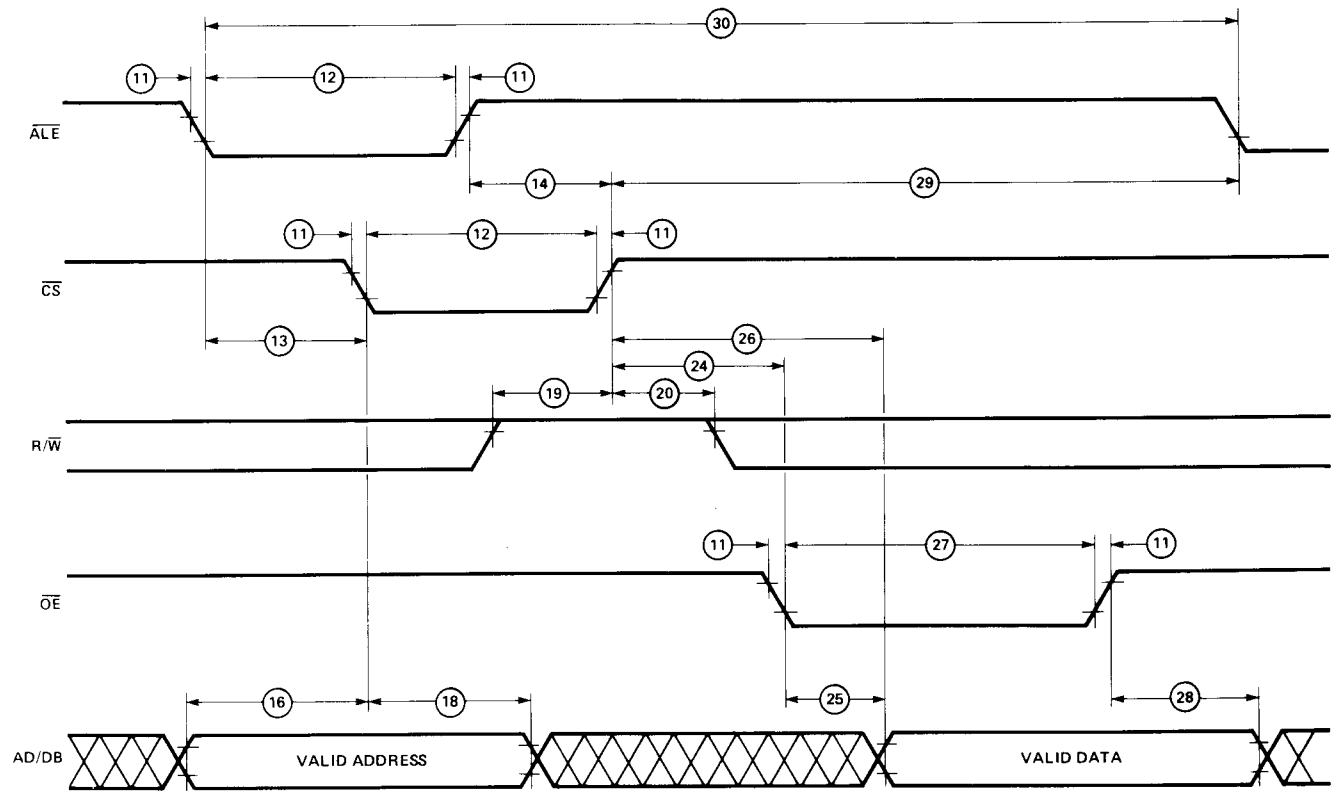
HCTL-1000 I/O Timing Diagrams

II. $\overline{ALE}/\overline{CS}$ OVERLAPPED

A. Write Cycle



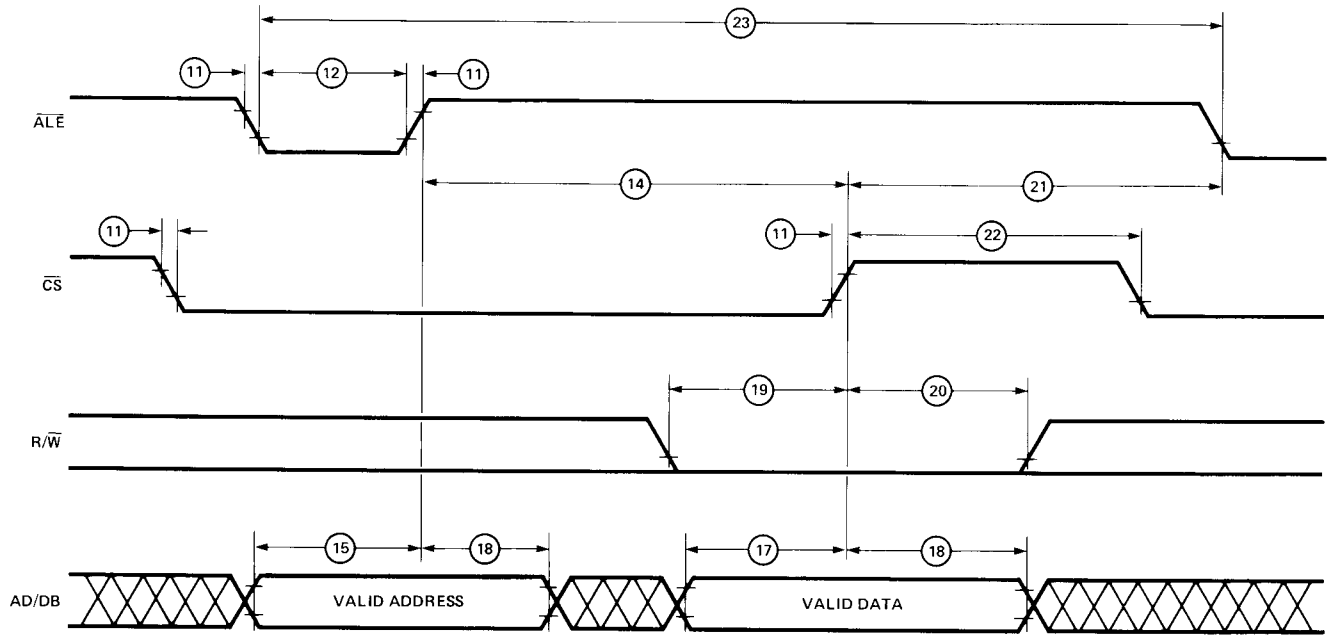
B. Read Cycle



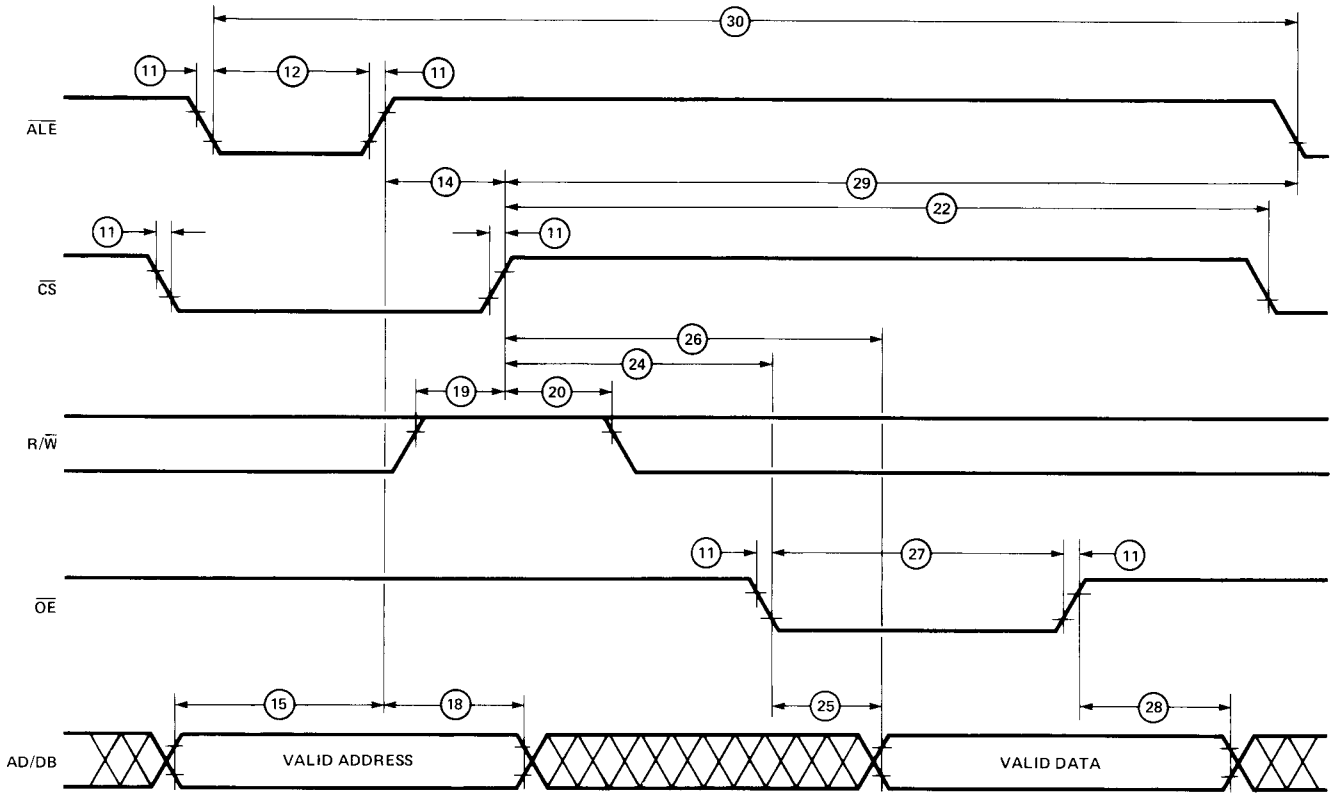
HCTL-1000 I/O Timing Diagrams

III. $\overline{ALE}$ WITHIN $\overline{CS}$

A. Write Cycle



B. Read Cycle



Functional Pin Description

INPUT/OUTPUT SIGNALS

Symbol	Pin Number	Description
AD0/DB0 — AD5/DB5	2 - 7	Address/Data bus — Low 6 bits of 8 bit I/O port which are multiplexed between address and data.
D6,D7	8, 9	Data bus — Upper 2 bits of 8 bit I/O port used for data only.

INPUT SIGNALS

Symbol	Pin Number	Description
CHA/CHB	31, 30	Channel A,B — input pins for position feedback from an incremental shaft encoder. Two channels, A and B, 90 degrees out of phase are required.
$\overline{\text{Index}}$	33	Index Pulse — input from the reference or index pulse of an incremental encoder. Used only in conjunction with the Commutator. Either a low or high true signal can be used with the Index pin. See Timing Diagrams and Encoder Interface section for more detail.
R/$\overline{\text{W}}$	37	Read/Write — determines direction of data exchange for the I/O port.
$\overline{\text{ALE}}$	38	Address Latch Enable — enables low 6 bits of external data bus into internal address latch.
$\overline{\text{CS}}$	39	Chip Select — performs I/O operation dependent on status of R/W line. For a Write, the external bus data is written into the internal addressed location. For Read, data is read from an internal location into an internal output latch.
$\overline{\text{OE}}$	40	Output Enable — enables the data in the internal output latch onto the external data bus to complete a Read operation.
$\overline{\text{Limit}}$	14	Limit Switch — an internal flag which when externally set, triggers an unconditional branch to the Initialization/Idle mode before the next control sample is executed. Motor Command is set to zero. Status of the Limit Flag is monitored in the Status Register.
$\overline{\text{Stop}}$	15	Stop Flag — an internal flag that is externally set. When flag is set during Integral Velocity control mode, the Motor Command is decelerated to a stop.
$\overline{\text{Reset}}$	36	Reset — a hard reset of internal circuitry and a branch to Reset mode.
ExtClk	34	External Clock
V_{CC}	11, 35	Voltage Supply — Both V_{CC} pins must be connected to a 5.0 volt supply.
V_{SS}	10, 32	Circuit Ground
NC	1	Not Connected — this pin should be left floating.

OUTPUT SIGNALS

Symbol	Pin Number	Description
MC0-MC7	18 - 25	Motor Command Port — 8 bit output port which contains the digital motor command adjusted for easy bipolar DAC interfacing. MC7 is the most significant bit (MSB).
Pulse	16	Pulse — Pulse Width Modulated signal whose duty cycle is proportional to the Motor Command magnitude. The frequency of the signal is External Clock/100 and pulse width is resolved into 100 external clocks.
Sign	17	Sign — gives the sign/direction of the pulse signal.
PHA-PHD	26 - 29	Phase A, B, C, D — phase enable outputs of the commutator.
Prof	12	Profile Flag — status flag which indicates that the controller is executing a profiled position move in the Trapezoidal Profile Control Mode.
Init	13	Initialization/Idle Flag — status flag which indicates that the controller is in the Initialization/Idle mode.

How to Operate the HCTL-1000 User Accessible Registers

The HCTL-1000 operation is controlled by a bank of 64 8-bit registers, 32 of which are user accessible. These registers contain command and configuration information necessary to properly run the controller chip. The 32 user accessible registers are listed in Table I. The register number is also the address. A functional block diagram of the HCTL-1000 which shows the role of the user accessible registers is also included in Figure 3. The other 32 registers are used by the internal CPU as scratch registers and should not be accessed by the user.

There are several registers which the user must configure to his application. These configuration registers are discussed in more detail below.

PROGRAM COUNTER (R05H)

The program counter, which is a write only register, executes the preprogrammed functions of the controller. The program counter is used along with the control flags F0, F3, and F5 in the Flag Register (R00H) to change control modes. The user can write any of the following four commands to the program counter.

00H — Software Reset
01H — Initialization/Idle mode
02H — Align mode
03H — Control modes; flags F0, F3, and F5 in the Flag Register (R00H) specify which control mode will be executed.

The commands written to the program counter are discussed in more detail in the section called Operating Modes and are shown in flowchart form in Figure 4.

FLAG REGISTER (R00H)

The flag register contains flags F0 thru F5. This register is also a *write only register.* Each flag is set and cleared by writing an 8-bit data word to R00H. The upper four bits are ignored by the HCTL-1000. The bottom three bits specify the flag address and the fourth bit specifies whether to set (bit=1) or clear (bit=0) the addressed flag.

Bit number	7-4	3	2	1	0
Function	Don't care	set/clear	AD2	AD1	AD0

F0 — Trapezoidal Profile Flag — set by the user to execute trapezoidal profile control. The flag is reset by the controller when the move is completed. The status of F0 can be monitored at the Profile pin (12) and in status register R07H bit 4.

F1 — Initialization/Idle Flag — set/cleared by the HCTL-1000 to indicate execution of the Initialization/Idle mode. The status of F1 can be monitored at the Initialization/Idle pin (13) and in bit 5 of the Status register (R07H). The user should never attempt to set or clear F1.

F2 — Unipolar flag — set/cleared by the user to specify bipolar (clear) or unipolar (set) mode for the Motor Command Port.

F3 — Proportional Velocity Control Flag — set by the user to specify proportional velocity control.

F4 — Hold Commutator Flag — set/cleared by the user or automatically by the Align mode. When set, this flag inhibits the internal commutator counters to allow open loop stepping of a motor by using the commutator.

F5 — Integral Velocity Control — set by the user to specify integral velocity control.

STATUS REGISTER (R07H)

The Status Register indicates the status of the HCTL-1000. Each bit decodes into one signal. All 8 bits are user readable and are decoded as shown below. Only the lower 4 bits can be written to by the user to configure the HCTL-1000. To set or clear any of the lower 4 bits, the user writes an 8-bit word to R07H. The upper 4 bits are ignored. Each of the lower 4 bits directly sets/clears the corresponding bit of the status register as shown below. For example, writing XXXX0101 to R07H sets the PWM Sign Reversal Inhibit, sets the Commutator Phase Configuration to "3 Phase", and sets the Commutator Count Configuration to "full".

Status Bit	Function	Note
0	PWM Sign Reversal Inhibit 0 = off 1 = on	Discussed in Amplifier Interface section under PWM Port.
1	Commutator Phase Configuration 0 = 3 phase 1 = 4 phase	Discussed in Commutator section
2	Commutator Count Configuration 0 = quadrature 1 = full	Discussed in Commutator section
3	Should always be set to 0	
4	Trapezoidal Profile Flag F0 1 = in Profile Control	Discussed in Operating Mode section under Trapezoidal Profile Control
5	Initialization/Idle Flag F1 1 = in Initialization/Idle Mode	Discussed in Operating Mode section under Initialization/Idle Mode
6	Stop Flag 0 = set (Stop triggered) 1 = cleared (no Stop)	Discussed in Emergency Flags Section
7	Limit Flag 0 = set (Limit triggered) 1 = cleared (no Limit)	Discussed in Emergency Flags Section

TABLE I: REGISTER REFERENCE TABLE

Register (Hex)	Function	Mode Used	Data Type	User Access
R00H	Flag Register	All	-----	w
R05H	Program Counter	All	scalar	w
R07H	Status Register	All	-----	r/w[1]
R08H	8 bit Motor Command Port	All	2's complement+80H	r/w
R09H	PWM Motor Command Port	All	2's complement	r/w
R0CH	Command Position (MSB)	Position Control	2's complement	r/w[2]
R0DH	Command Position	Position Control	2's complement	r/w[2]
R0EH	Command Position (LSB)	Position Control	2's complement	r/w[2]
R0FH	Sample Timer	All	scalar	w
R12H	Actual Position (MSB)	Position Control	2's complement	r[3]
R13H	Actual Position	Position Control	2's complement	r[3]/w[4]
R14H	Actual Position (LSB)	Position Control	2's complement	r[3]
R18H	Commutator Ring	All	scalar[5]	r/w[6]
R19H	Commutator Velocity Timer	All	scalar	w
R1AH	X	All	scalar[5]	r/w
R1BH	Y Phase Overlap	All	scalar[5]	r/w
R1CH	Offset	All	2's complement	r/w[6]
R1FH	Maximum Phase Advance	All	scalar[5]	r/w[6]
R20H	Filter Zero, A	All except Proportional Velocity	scalar	r/w
R21H	Filter Pole, B	All except Proportional Velocity	scalar	r/w
R22H	Gain, K	All	scalar	r/w
R23H	Command Velocity (LSB)	Proportional Velocity	2's complement	r/w
R24H	Command Velocity (MSB)	Proportional Velocity	2's complement	r/w
R26H	Acceleration (LSB)	Integral Velocity and Trapezoidal Profile	scalar[5]	r/w
R27H	Acceleration (MSB)	Integral Velocity and Trapezoidal Profile	scalar[5]	r/w
R28H	Maximum Velocity	Trapezoidal Profile	scalar[5]	r/w
R29H	Final Position (LSB)	Trapezoidal Profile	2's complement	r/w
R2AH	Final Position	Trapezoidal Profile	2's complement	r/w
R2BH	Final Position (MSB)	Trapezoidal Profile	2's complement	r/w
R34H	Actual Velocity (LSB)	Proportional Velocity	2's complement	r
R35H	Actual Velocity (MSB)	Proportional Velocity	2's complement	r
R3CH	Command Velocity	Integral Velocity	2's complement	r/w

Notes:

1. Upper 4 bits are read only.
2. Writing to R0EH (LSB) latches all 24 bits.
3. Reading R14H (LSB) latches data into R12H and R13H.
4. Writing to R13H clears Actual Position Counter to zero.
5. The scalar data is limited to positive numbers (00H to 7FH).
6. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.

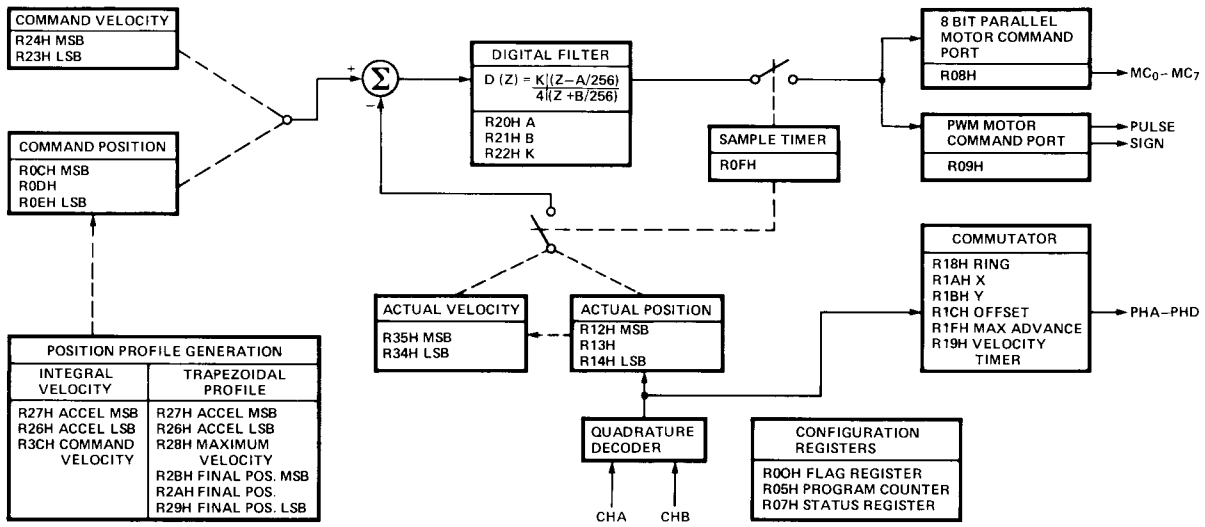


Figure 3. Register Block Diagram

EMERGENCY FLAGS — STOP AND LIMIT

Stop and Limit Flags are hardware set flags that signify the occurrence of an emergency condition and cause the controller to immediately take special action.

The Stop Flag affects the HCTL-1000 only in the Integral Velocity Mode. When the Stop Flag is set, the system will come to a decelerated stop and stay in this mode with a command velocity of zero until the Stop Flag is cleared and a new command velocity is specified.

The Limit Flag, when set in any control mode, causes the HCTL-1000 to go into the Initialization/Idle Mode, clearing the Motor Command and causing an immediate motor shutdown.

Stop and Limit Flags are set by a low level input at their respective pins (15, 14). The flags can only be cleared when the input to the corresponding pin goes high, signifying that the emergency condition has been corrected, AND a write to the Status Register (R07H) is executed. That is, after the emergency pin has been set and cleared, the flag also must be cleared by writing to R07H. Any word that is written to R07H after the emergency pin is set and cleared will clear the emergency flag, but the lower 4 bits of that word will also reconfigure the Status Register.

DIGITAL FILTER (R22H, R20H, R21H)

All control modes use some part of the programmable digital filter D(z) to compensate for closed loop system stability. The compensation D(z) has the form:

$$D(z) = \frac{K\,(z - A/256)}{4\,(z + B/256)}$$

where z = the digital domain operator

K = gain (R22H)
A = zero (R20H)
B = pole (R21H)

The compensation is a first order lead filter which in combination with the sample timer T (R0FH) affects the dynamic step response and stability of the control system. The sample timer, T, determines the rate at which the control algorithm gets executed. All parameters, A, B, K, and T, are 8-bit scalars that can be changed by the user any time.

The digital filter uses previously sampled data to calculate D(z). This old internally sampled data is cleared when the Initialization/Idle Mode is executed.

SAMPLE TIMER REGISTER (R0FH)

The contents of this register set the sampling period of the HCTL-1000. The sampling period is

$$t = 16\,(R0FH + 1)\,(1/\text{frequency of the external clock})$$

The sample timer has a limit on the minimum allowable sample time depending on the control mode being executed. The limits are given below:

	R0FH Contents Minimum Limit
Position Control	7
Proportional Velocity Control	7
Trapezoidal Profile Control	15
Integral Velocity Control	15

The maximum value of R0FH is FFH (255 decimal). For example, with a 2MHz clock, the sample time can vary from 64 μsec to 2048 μsec.

Operating Modes

The HCTL-1000 executes any one of 3 set up routines or 4 control modes selected by the user. The 3 set up routines include:

— Reset
— Initialization/Idle
— Align.

The four control modes available to the user include:

— Position Control
— Proportional Velocity Control
— Trapezoidal Profile Control
— Integral Velocity Control

The HCTL-1000 switches from one mode to another as a result of one of the following three mechanisms:

1. The user writes to the Program Counter.
2. The user sets/clears flags F0, F3, or F5 by writing to the Flag Register (R00H).
3. The controller switches automatically when certain initial conditions are provided by the user.

This section describes the function of each set up routine and control mode and the initial conditions which must be provided by the user to switch from one mode to another. Figure 4 shows a flowchart of the set up routines and control modes, and shows the commands required to switch from one mode to another.

SET UP ROUTINES

1. Reset

The Reset mode is entered under all conditions by either executing a hard reset (Reset Pin goes low) or a soft reset (write 00H to the Program Counter, R05H).

When a hard reset is executed, the following conditions occur:

— All output signal pins are held low except Sign (17), Databus (2-9), and Motor Command (18-25).

— All flags (F0 to F5) are cleared.

— The PWM port (R09H) is preset to FFH.

— The Motor Command Port (R08H) is preset to 80H.

— The Commutator logic is cleared.

— The I/O control logic is cleared.

— A soft reset is automatically executed.

When a soft reset is executed, the following conditions occur:

— The digital filter parameters are preset to

A (R20H) = E5H
B (R21H) = K (R22H) = 40H

— The sample timer (R0FH) is preset to 40H.

— The status register (R07H) is cleared.

— The Position counters (R12H, R13H and R14H) are cleared to 0.

From Reset mode, the HCTL-1000 goes automatically to Initialization/Idle mode.

2. Initialization/Idle

The Initialization/Idle mode is entered either automatically from Reset or by writing 01H to the Program Counter (R05H) under any conditions.

In the Initialization/Idle mode, the following conditions occur:

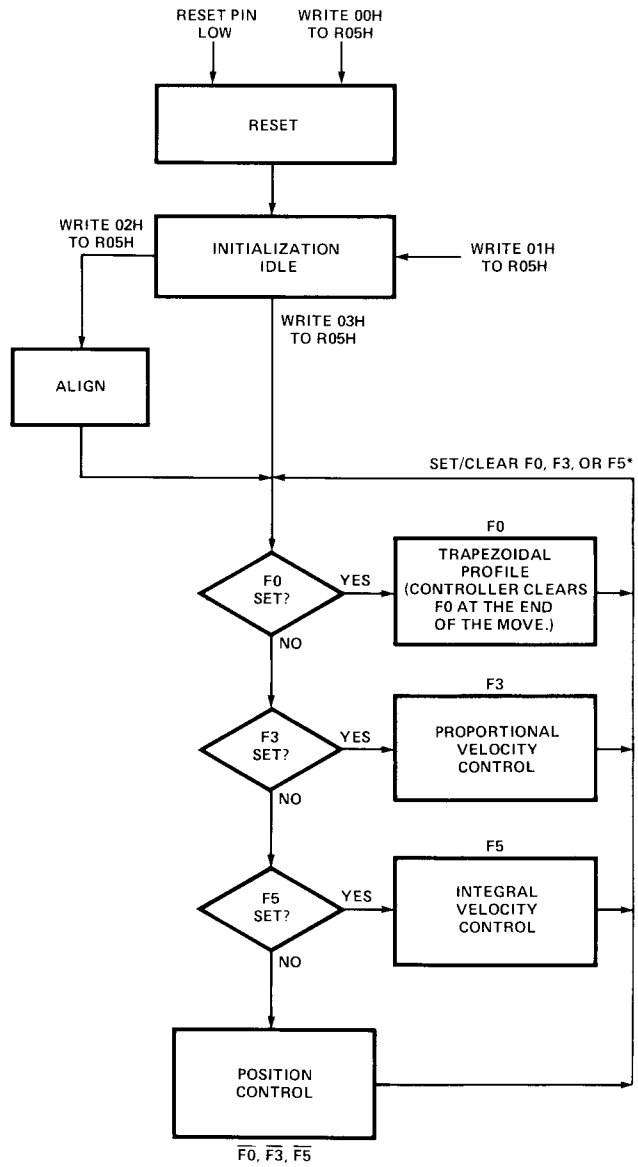
— The Initialization/Idle Flag (F1) is set.

— The PWM port (R09H) is set to 00H.

— The Motor Command port (R08H) is set to 80H.

— Previously sampled data stored in the digital filter is cleared.

It is at this point that the user should pre-program all the necessary registers needed to execute the desired control mode. The HCTL-1000 stays in this mode (idling) until a new mode command is given.



***Only one flag can be set at a time.**

Figure 4. Operating Mode Flowchart

3. **Align**

The Align mode can be entered only from the Initialization/Idle mode by writing 02H to the Program Counter (R05H). This mode automatically aligns multiphase motors to the Commutator. Align mode is executed only when using the commutator feature of the HCTL-1000 and before any control modes are used.

The Align mode assumes that, during encoder/motor assembly, the encoder index pulse has been physically aligned to the last motor phase, the Commutator parameters have been correctly preprogrammed (see the section called *The Commutator* for details), and a hard reset has been executed while the motor is stationary.

The Align mode first disables the commutator and with open loop control enables the first phase (PHA) and then the last phase (PHC or PHD) to orient the motor on the last phase torque detent. Each phase is energized for 2048 system sampling periods. For proper operation, the motor must come to a complete stop during the last phase enable. Once the last phase torque detent is found, the Commutator is enabled and commutation is closed loop.

The HCTL-1000 then switches automatically from Align to the Control Modes.

CONTROL MODES

Control flags F0, F3, and F5 in the Flag Register (R00H) determine which control mode is executed. *Only one control flag can be set at a time.* After one of these control flags is set, the control modes are entered either automatically from Align or from the Initialization/Idle mode by writing 03H to the Program Counter (R05H).

1. **Position Control**

F0, F3, F5 cleared

Position Control performs point to point position moves with no velocity profiling. The user specifies a 24-bit position command, which the controller compares to the 24-bit actual position. The position error is calculated, the full digital lead compensation is applied and the motor command is output.

The controller will remain position locked at a destination until a new position command is given.

The actual and command position data is 24-bit two's complement data stored in six 8-bit registers. Position is measured in encoder quadrature counts.

The command position resides in R0CH (MSB), R0DH, R0EH (LSB). Writing to R0EH latches all 24-bits at once for the control algorithm. Therefore, the command position is written in the sequence R0CH, R0DH and R0EH. The command registers can be read in any desired order.

The actual position resides in R12H (MSB), R13H, and R14H (LSB). Reading R14H latches the upper two bytes into an internal buffer. Therefore, actual position registers are read in the order of R14H, R13H, and R12H for correct instantaneous position data. The position registers cannot be written to, but they can all be cleared to 0 by a write to R13H.

2. **Proportional Velocity Control**

F3 set

Proportional Velocity Control performs control of motor speed using only the gain factor, K, for compensation. The dynamic pole and zero lead compensation are not used.

The algorithm takes a user command velocity, calculates the actual velocity, and computes the velocity error. The velocity error is multiplied by K/4 and output as motor command.

The command and actual velocity are 16-bit two's complement words. The units of velocity are encoder quadrature counts/sample time. In addition, the command velocity is internally divided by 16 to produce fractional resolution. The 16-bit command is interpreted as 12-bits of integer and 4-bits of fraction.

R24H	R23H
IIII IIII	IIII.FFFF

COMMAND VELOCITY FORMAT

The command velocity resides in unlatched R24H (MSB) and R23H (LSB). The registers can be read or written to in any order.

The actual velocity is computed only in this algorithm and stored in scratch registers R35H (MSB) and R34H (LSB). There is no fractional component in the actual velocity registers and they can be read in any order.

The controller tracks the command velocity continuously until new mode command is given. The system behavior after a new velocity command is governed only by the system dynamics, until a steady state velocity is reached.

3. **Integral Velocity Control**

F5 set

Integral Velocity Control performs continuous velocity profiling which is specified by a command velocity and command acceleration. Figure 5 shows the capability of this control algorithm.

The user can change velocity and acceleration any time to continuously profile velocity in time. Once the specified velocity is reached, the HCTL-1000 will maintain that velocity until a new command is specified. Changes between actual velocities occur at the presently specified linear acceleration.

The command velocity is an 8-bit two's complement word stored in R3CH. The units of velocity are quadrature counts/sample time.

While the overall range of the velocity command is 8-bits, two's complement, the difference between any two sequential commands cannot be greater than 7-bits in magnitude (i.e., 127 decimal). For example, when the HCTL-1000 is executing a command velocity of 40H (+64D), the next velocity command must fall in the range of 7FH (+127D), the maximum command range, to C1H (−63D).

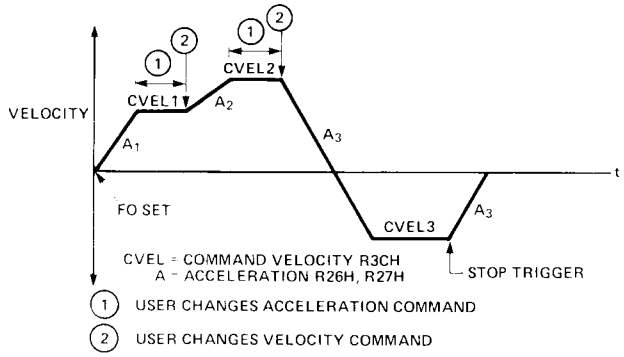


Figure 5. Integral Velocity Mode

The command acceleration is a 16-bit scalar word stored in R27H and R26H. The upper byte (R27H) is the integer part and the lower byte (R26H) is the fractional part provided for resolution. The integer part has a range of 00H to 7FH. The contents of R26H are internally divided by 256 to produce the fractional resolution.

R27H	R26H
0IIIIIII .	FFFFFFFF/256

COMMAND ACCELERATION FORMAT

The units of acceleration are quadrature counts/sample time squared.

Internally, the controller performs velocity profiling through position control. From the user specified command velocity and acceleration, the controller internally generates position profiles. In control theory terms, integral compensation has been added and therefore, this system has zero steady state velocity error.

The advantage that this mode has over Proportional Velocity modes is that the system has zero steady state velocity error. However, the drawback which comes along with this advantage is that loop stability compensation is more difficult to achieve. In the Integral Velocity Mode, the system is actually a position control system and therefore the complete dynamic compensation D(z) is used in this control mode.

If the external STOP flag F6 is set during this mode signaling an emergency situation, the controller automatically decelerates to zero velocity at the presently specified acceleration factor and stays in this condition until the flag is cleared. The user then can specify new velocity profiling data.

4. Trapezoidal Profile Control
F0 set

Trapezoidal Profile Control performs point to point position moves and profiles the velocity trajectory to a trapezoid or triangle. The user specifies only the desired final position, acceleration and maximum velocity. The controller computes the necessary profile to conform to the command data. If maximum velocity is reached before the distance halfway point, the profile will be trapezoidal, otherwise the profile will be triangular. Figure 6 shows the possible trajectories with Trapezoidal Profile control.

The command data for this control mode is a 24-bit two's complement final position written to R2BH (MSB), R2AH, and R29H (LSB). The acceleration resides in R27H (MSB) and R26H (LSB). It is the same integer and fraction

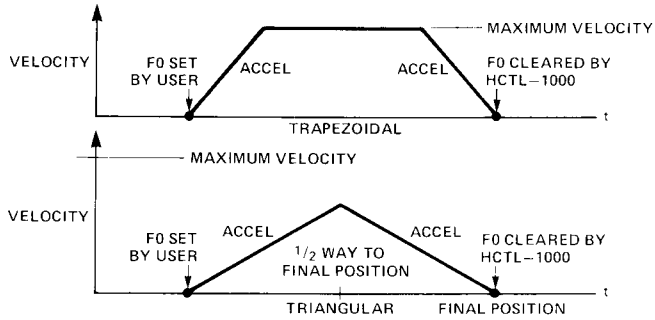


Figure 6. Trapezoidal Profile Mode

format as discussed under Integral Velocity Control. The maximum velocity is a 7-bit scalar (range is 00H to 7FH) written to R28H with units of quadrature counts/sample. The command data registers can be written/read in any order.

Once desired data is entered, flag F0 is set in the Flag Register (R00H) to commence motion (if already in Position Control). When the Trapezoidal Profile move is finished, the controller clears F0 and Position Control locks on the final position. The status of the Profile flag can be monitored in the Status Register (R07H) and at the external Profile pin. During Trapezoidal Profile move no new command data should be sent to the controller.

The internal profile generator produces a position profile using the present command position (R0CH-R0EH) as the starting point and the final position (R29H-R2BH) as the end point. The controller actually performs position control while the profile generator loads profile data into the Command Position registers. The full digital filter is applied for compensation.

Commutator

The commutator is a digital state machine that is configured by the user to properly select the phase sequence for electronic commutation of multiphase motors. The Commutator is designed to work with 2, 3, and 4 phase motors of various winding configurations and with various encoder counts.

Besides the correct phase enable sequence, the Commutator provides programmable phase overlap and phase advance. Phase overlap is used for better torque ripple control. It can also be used to generate unique state sequences which can be further decoded externally to drive more complex amplifiers and motors.

Phase advance allows the user to compensate for the frequency characteristics of the motor/amplifier combination. By advancing the phase enable command (in position), the delay in reaction of the motor/amplifier combination can be offset and higher performance can be achieved.

The ouput of the Commutator is on PHA (26) to PHD (29). The inputs to the Commutator are the three encoder signals, Channel A, Channel B, and Index, and the configuration data stored in registers.

The Commutator uses both channels and the index pulse of an incremental encoder. The index pulse of the encoder must be physically aligned to a known torque curve location because it is used as the reference point of the rotor position with respect to the Commutator phase enables.

The index pulse should be permanently aligned during motor encoder assembly to the last motor phase. This is done by energizing the last phase of the motor during assembly and permanently attaching the encoder codewheel to the motor shaft such that the index pulse is active. Fine tuning of alignment for commutation purposes is done electronically by the Offset Register (R1CH) once the complete control system is set up.

1. Commutator Configuration Registers

The Commutator is programmed by the data in the following registers. Figure 7 shows an example of the relationship between all the parameters.

Status Register (R07H)

Bit #1 — 0 = 3 phase configuration, PHA, PHB, and PHC are active outputs.
1 = 4 phase configuration, PHA - PHD are active outputs.

Bit #2 — 0 = rotor position measured in quadrature counts.
1 = rotor position measured in full counts.

RING REGISTER (R18H)

The ring register is scalar and determines the length of the electrical cycle measured in full or quadrature counts as set by bit #1 in R07H. The magnitude of Ring is limited to 7FH.

X REGISTER (R1AH)

Scalar data which sets the interval during which a phase is the only one active.

Y REGISTER (R1BH)

Scalar data which sets the interval during which two sequential phases are both active. Y is phase overlap.

X and Y must be such that:

X + Y = Ring/(# of phases)

These three parameters define the basic electrical commutation cycle.

OFFSET REGISTER (R1CH)

The offset is two's complement data which determines the relative start of the electrical cycle with respect to the index pulse. Since the index pulse must be physically referenced to the rotor, offset performs fine alignment between the electrical and mechanical torque cycles.

PHASE ADVANCE REGISTERS (R19H, R1FH)

The phase advance feature performs the function of linearly incrementing the phase advance according to measured speed of rotation up to a set maximum.

VELOCITY TIMER REGISTER (R19H)

This register contains scalar data which determines the amount of phase advance at a given velocity. The phase advance is interpreted in the units set for the Ring counter by bit #1 in R07H. The velocity is measured in revolutions/second.

$$\text{Advance} = Nv\Delta t$$

$$\text{where } \Delta t = \frac{16\,(R19H+1)}{\text{f external clk}}$$

N = encoder counts/revolution
v = velocity (revolutions/second)

3 PHASE
FULL COUNTS
RING: 9

ENCODER: 90 COUNTS/REVOLUTION

CASE	1	2	3	4
X	3	2	2	2
Y	0	1	1	1
OFFSET	0	0	2	2
ADVANCE	0	0	0	1

INDEX PULSE OCCURS AT THE ORIGIN

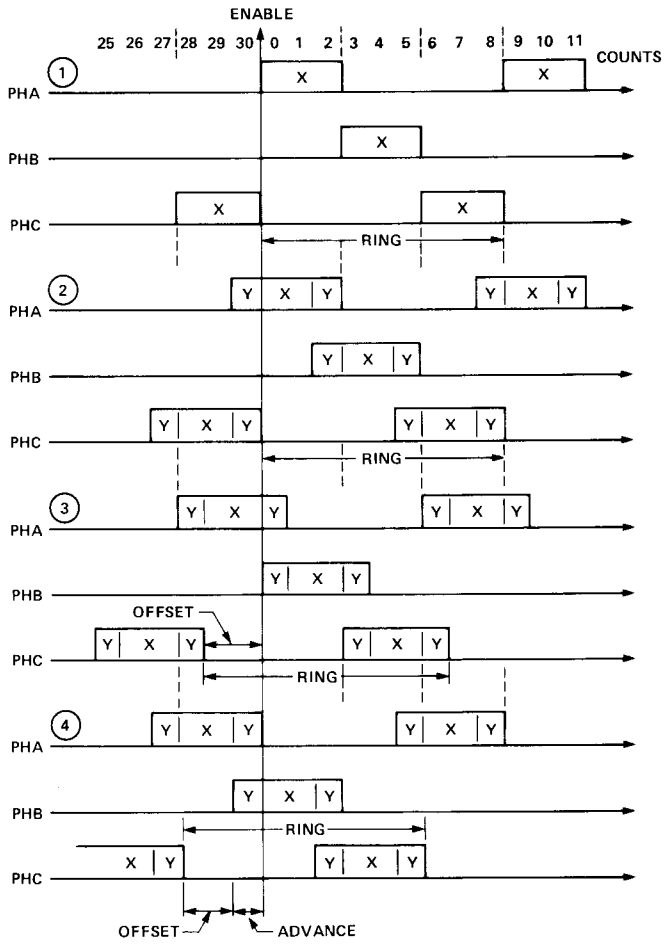


Figure 7. Commutator Configuration

MAXIMUM ADVANCE REGISTER (R1FH)

The scalar data sets the upper limit for phase advance regardless of rotor speed.

Figure 8 shows the relationship between the phase advance registers. Note: If the phase advance feature is not used, set both R19H and R1FH to 0.

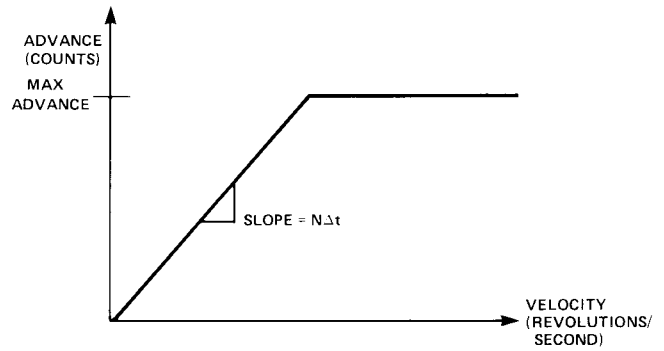


Figure 8. Phase Advance vs. Motor Velocity.

COMMUTATOR CONSTRAINTS

There are several numerical constraints the user should be aware of to use the Commutator.

The parameters of *Ring*, *X*, *Y*, and *Max Advance* must be positive numbers (00H to 7FH). Additionally, the following equation must be satisfied:

$$80H \leq \frac{3}{2}\text{Ring} + \text{Offset} \pm \text{Max Advance} \leq 7FH \quad (1)$$

In order to utilize the greatest flexibility of the Commutator, it must be realized that the Commutator works on a circular ring counter principle, whose range is defined by the Ring Register (R18H). This means that for a ring of 96 counts and a needed offset of 10D, numerically the Offset Register can be programmed as 0AH (10D) or D0H (−80D), the latter satisfying Equation 1.

Example: Suppose you want to commutate a 3 phase 15 deg/step Variable Reluctance Motor attached to a 192 count encoder.

1. Select 3 phase and quadrature mode for commutator by writing 0 to R07H.
2. With a 3 phase 15 degree/step Variable Reluctance Motor the torque cycle repeats every 45 degrees or 360 deg/45 deg/revolution.
3. $$\text{Ring Register} = \frac{(4)\,(192)\ \text{counts/revolution}}{8/\text{revolution}}$$
   $$= 96 \text{ quadrature counts}$$
4. By measuring the motor torque curve in both directions, it is determined that an offset of 3 degrees, and a phase overlap of 2 degrees is needed.

   $$\text{Offset} = 3° \quad \frac{(4)\,(192)}{360°} \simeq 6 \text{ quadrature counts}$$

   To numerically satisfy the commutator write A6H (−90D) to Offset Register (R1CH).

   $$y = \text{overlap} = \frac{(2°)\,(4)\,(192)}{360°} \simeq 4$$

   $$\frac{x + y}{3} = 96$$

   Therefore, $x = 28$
   $y = 4$

   For the purposes of this example, the Velocity Timer and Maximum Advance are set to 0.

How to Interface to the HCTL-1000

I/O INTERFACE

The HCTL-1000 looks to the user like a bank of 8-bit registers which the user can read/write. The data in these registers control the operation of the HCTL-1000. The user communicates with these registers over an 8-bit address/data multiplexed bidirectional bus. The four I/O control lines, $\overline{ALE}$, $\overline{CS}$, $\overline{OE}$ and $\overline{R/W}$, execute the data transfers.

There are three different timing configurations which can be used to give the user greater flexibility to interface the HCTL-1000 to most microprocessors (see Timing diagrams). They are differentiated from one another by the arrangement of the $\overline{ALE}$ signal with respect to the $\overline{CS}$ signal. The three timing configurations are listed below.

1. $\overline{ALE}$, $\overline{CS}$ non-overlapped
2. $\overline{ALE}$, $\overline{CS}$ overlapped
3. $\overline{ALE}$ within $\overline{CS}$

Any I/O operation starts by asserting the $\overline{ALE}$ signal which starts sampling the external bus into an internal address latch. Rising $\overline{ALE}$ or falling $\overline{CS}$ during $\overline{ALE}$ stops the sampling into the address latch.

$\overline{CS}$ low after rising $\overline{ALE}$ samples the external bus into the data latch. Rising $\overline{CS}$ stops the sampling into the data latch, and starts the internal synchronous process.

In the case of a write, the data in the data latch is written into the addressed location. In the case of a read, the addressed location is written into an internal output latch. $\overline{OE}$ low enables the internal output latch onto the external bus. The $\overline{OE}$ signal and the internal output latch allow the I/O port to be flexible and avoid bus conflicts during read operations.

The I/O Port is designed to work with most microprocessor systems and is easily fitted in as part of addressable RAM.

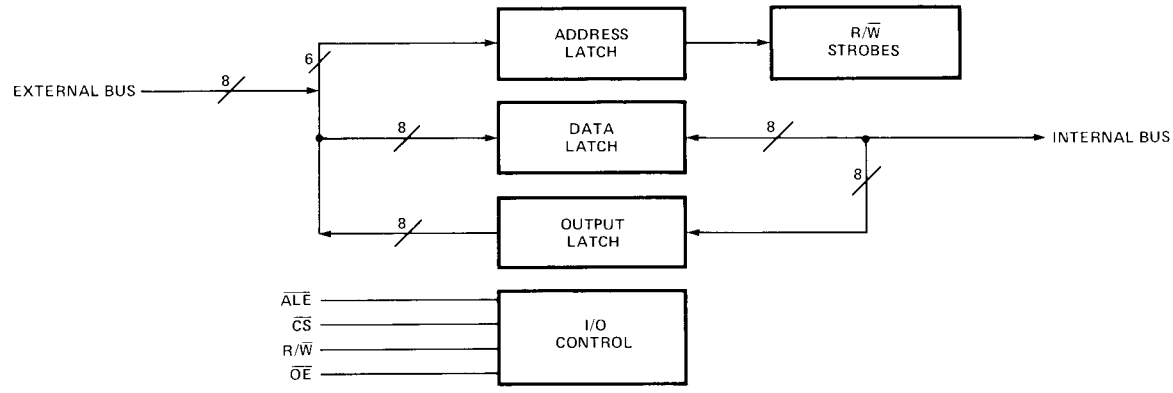


Figure 9. I/O Port Block Diagram

ENCODER INTERFACE

The HCTL-1000 accepts TTL compatible outputs from 2 or 3 channel incremental shaft encoders such as the HEDS-5000 and 6000 series. Channels A and B are internally decoded into quadrature counts which increment or decrement the 24-bit position counter. For example, a 500 count encoder is decoded into 2000 quadrature counts per revolution. The position counter will be incremented when Channel B leads Channel A. The Index channel is used only for the Commutator and its function is to serve as a reference point for the internal Ring Counter.

The inputs to the quadrature decoder from Channel A and B, have a 3-bit state delay filter to filter out unwanted noise spikes on the encoder input lines. Any transition on the input pins must be stable during 3 consecutive external clock edges before it is qualified internally as a legitimate transition. This 3-bit state delay filter, together with the quadrature decoder, impose a limit on the encoder frequency.

The AC specifications give the delay requirements between encoder signal edges. When calculating the encoder frequency limit, the user must take into consideration the external clock frequency and the encoder state width error.

The index signal of an encoder is used in conjunction with the Commutator. It resets the internal ring counter which keeps track of the rotor position so that no cumulative errors are generated.

The Index pin of the HCTL-1000 also has a 3-bit filter on its input. The Index pin is *active low and level transition sensitive.* It detects a valid high to low transition and qualifies the low input level through the 3-bit filter. At this point, the Index signal is internally detected by the commutator logic. This type of configuration allows an Index or $\overline{\text{Index}}$ signal to be used to generate the reference mark for commutator operation as long as the AC specifications for the Index signal are met.

AMPLIFIER INTERFACE

The HCTL-1000 outputs a motor command in two forms: an 8-bit Motor Command which can be connected to a DAC to drive a linear amplifier and PULSE and SIGN output to drive a PWM amplifier.

All control algorithms internally compute an error between the desired command and actual feedback which is processed through the digital filter. The result is an internal 8-bit 2's complement motor command. Before the internal motor command is made externally available, it is additionally adjusted for different output formats and ease of interfacing to external hardware. The sections below discuss the externally available amplifier interfaces and their formats. Tables II and III summarize the amplifier interface outputs.

8-Bit Parallel Motor Command Port

The 8-bit Motor Command Port consists of register R08H whose data goes directly to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to, however, it should be written to only during Initialization/Idle mode. During any of the four Control Modes, the controller writes the motor command into R08H.

The Motor Command Port is the ideal interface to an 8-bit DAC, configured for bipolar output. The data written to the 8-bit Motor Command Port by the control algorithms is the internally computed 2's complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Figure 10 shows a typical DAC interface to the HCTL-1000. An inexpensive DAC, such as MC1408 or equivalent, has its digital inputs directly connected to the Motor Command Port. The DAC produces an output current which is converted to a voltage by an operational amplifier. R_O and R_G control the analog offset and gain. The circuit is easily adjusted for +5V to −5V operation by first writing 80H to R08H and adjusting R_O for 0V output. Then FFH is written to R08H and R_G is adjusted until the output is 5V. Note that 00H in R08H corresponds to −5V out.

The above interface is suitable to drive linear amplifiers and DC motors because of the bipolar output. When using commutated motors, the direction of rotation of the motor is governed by the order of firing the motor phases which is under commutator control. In this case, it is desirable to have the Motor Command be unipolar to specify magnitude only, not direction. The HCTL-1000 has the feature of digitally configuring the 8-bit Motor Command Port into unipolar mode. Flag F2 in the Flag Register R00H controls this function.

F2 clear — Bipolar mode
F2 set — Unipolar mode

This mode functions such that, with the same circuit in Figure 10 (or any DAC configured for similar bipolar operation) setting F2 will cause the DAC to output from 0V to 5V only and to digital data on pins MC0 to MC7 to be restricted in the control modes from 80H to FFH. Internally the commutator keeps track of the sign of the motor command for proper commutation of the motor.

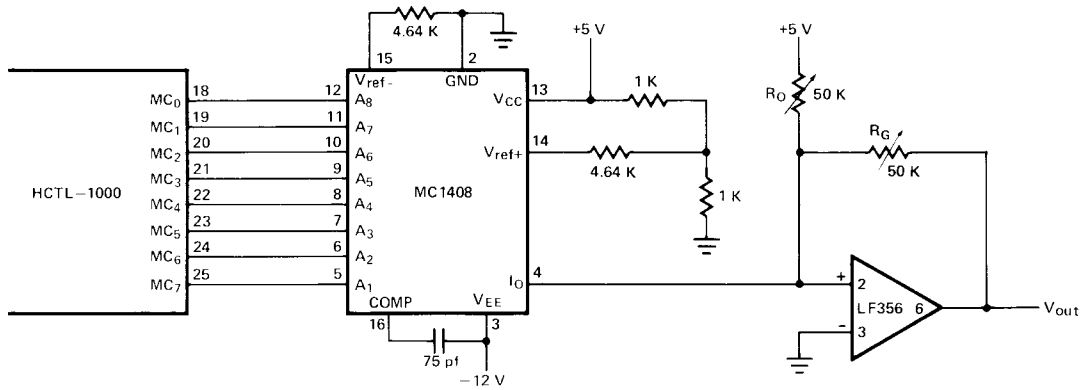


Figure 10. Linear Amplifier Interface

Internally, the HCTL-1000 operates on data of 24, 16 and 8-bit lengths to produce the 8-bit motor command, available externally. Many times the computed motor command will be greater than 8-bits. At this point, the motor command is saturated by the controller. The saturated value output by the controller is not the full scale value 00H, or FFH. The saturated value is adjusted to 0FH (negative saturation) and F0H (positive saturation). Saturation levels for the Motor Command Port are also included in Table II.

PWM Port

The PWM port outputs the motor command as a pulse width modulated signal with the correct sign of polarity. The PWM Port consists of the Pulse and Sign pins (pins 16 and 17) and R09H.

The PWM signal at the Pulse pin has a frequency of External Clock/100 and the duty cycle is resolved into the 100 clocks.

The Sign pin gives the polarity of the command. Low output on Sign pin is positive polarity.

The 2's complement contents of R09H determine the duty cycle and polarity of the PWM command. For example, D8H (−40D) gives a 40% duty cycle signal at the Pulse pin and forces the Sign pin high. Data outside the 64H (+100D) to 9CH (−100D) linear range gives 100% duty cycle. R09H can be read and written to. However, the user should only write to R09H when the controller is in the Initialization/Idle mode. Table II gives the PWM output vs the internal motor command.

When any Control Mode is being executed, the unadjusted internal 2's complement motor command is written to R09H. Because of the hardware limit on the linear range (64H to 9CH; ±100D), the PWM port saturates sooner than the 8-bit Motor Command Port (00H to FFH; +127D to −128D). When the internal Motor Command saturates above 8 bits, the PWM Port is saturated to the full ±100% duty cycle level. Table III gives the actual values inside the PWM port. Note that the unipolar Flag, F2, does *not* affect the PWM port.

TABLE II. MOTOR COMMAND PORT OUTPUTS

Functional Condition During Control Modes	Internal Motor Command 2's Complement	Motor Command Port R08H, MC0-MC7		DAC Output	
		Bipolar F2 = 0	Unipolar F2 = 1	Biploar F2 = 0	Unipolar F2 = 1
Minimum Motor Command	80H	00H	FFH	−5.0 V	5.0 V
Negative Internal Motor Command Saturation	< 80H	0FH	F0H	−4.4 V	4.4 V
Zero Motor Command	00H	80H	80H	0 V	0 V
Position Internal Motor Command Saturation	> 7FH	F0H	F0H	4.4 V	4.4 V
Maximum Motor Command	7FH	FFH	FFH	5.0 V	5.0 V

TABLE III. PWM PORT OUTPUTS

Functional Condition During Control Modes	Internal Motor Command	PWM Port		
		R09H	Pulse Duty Cycle	Sign
Minimum Motor Command	80H	80H	100%	High
Negative Internal Motor Command Saturation	< 80H	8FH	100%	High
Minimum PWM Linear Range	9CH	9CH	100%	High
Zero Motor Command	00H	00H	0%	Low
Positive Internal Motor Command Saturation	> 7FH	70H	100%	Low
Maximum PWM Linear Range	64H	64H	100%	Low
Maximum Motor Command	7FH	7FH	100%	Low

The PWM port has an option that can be used with H bridge type amplifiers. The option is Sign Reversal Inhibit, which inhibits the Pulse output for one PWM period after a sign polarity reversal. This allows one pair of transistors to turn off before others are turned on and thereby avoids a short across the power supply. Bit 0 in the Status Register (R07H) controls the sign reversal inhibit option. Figure 11 shows the output of the PWM port when Bit 0 is set.

Figure 12 shows an example of how to interface the HCTL-1000 to an H bridge amplifier (amplifier schematic is simplified). An H bridge amplifier works such that either Q1 and Q4 conduct or Q2 and Q3 conduct. This allows for bipolar motor operation with a unipolar power supply. The Sign Reversal Inhibit feature prevents all transistors from being on at the same time when the direction of motion is reversed.

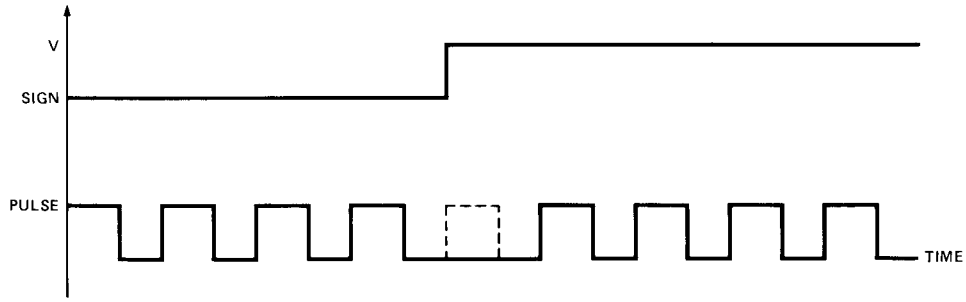


Figure 11. Sign Reversal Inhibit

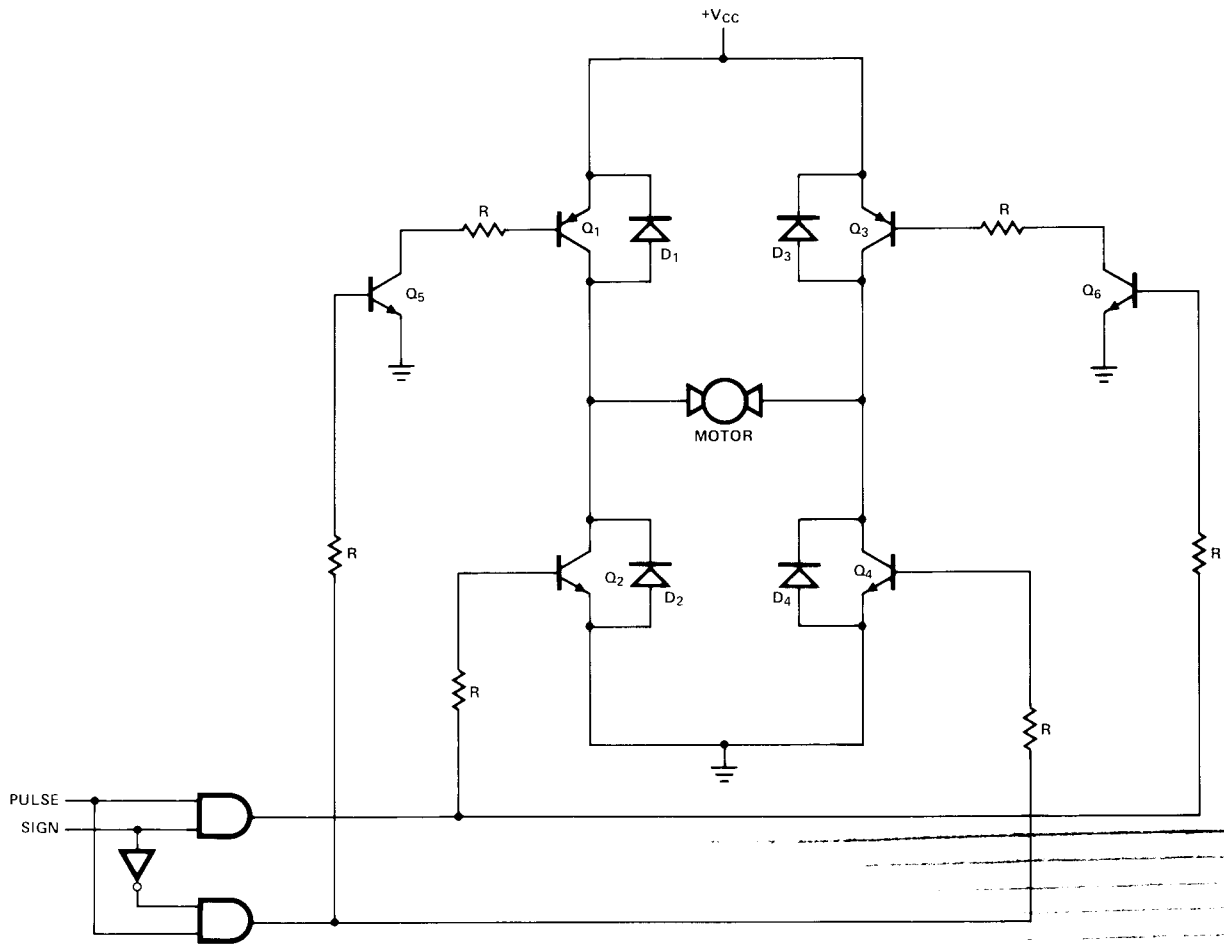
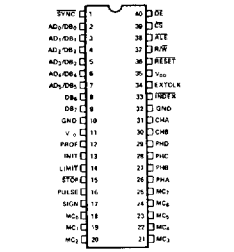
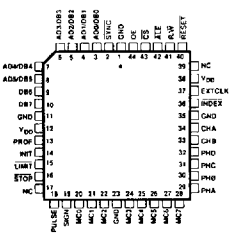
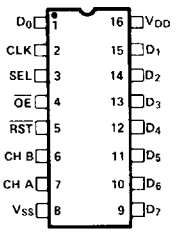
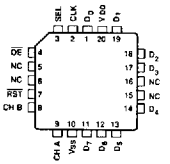
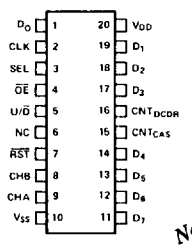
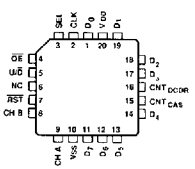


Figure 12. H-Bridge Amplifier Interface

UNRES

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61