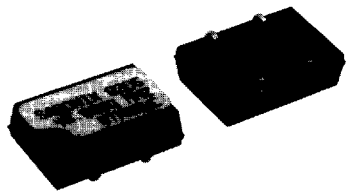
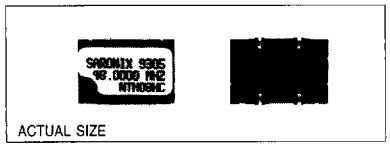
SaRonix

Crystal Clock Oscillator HCMOS, TTL, Tri-State, SMD

Technical Data NTH / NTT Series, Type H





ACTUAL SIZE

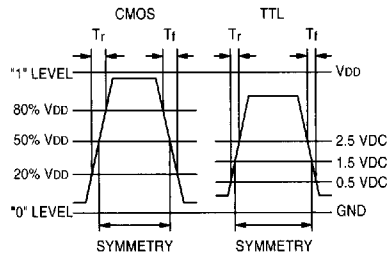
Description

A crystal controlled, low current oscillator providing rise and fall times to drive HCMOS and NMOS microprocessors. The plastic-molded surface mountable package is ideal for today's automated assembly environments. J-leads are compatible with EIA standard footprints. The HCMOS device is capable of driving both CMOS and TTL loads.

Applications & Features

- Compact, plastic-molded, surface mountable package
- TTL and CMOS compatible
- Tri-State output
- Matches EIA standard SO-J-20 footprint
- Ideally suited for use with contemporary MPU's and custom ASIC's.

Output Waveform



Frequency Range:	1 MHz to 70 MHz
Frequency Stability:	±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.
Temperature Range:	
Operating:	0°C to +70°C
Storage:	-55°C to +125°C
Supply Voltage:	
Recommended Operating:	+5 VDC ±10%
Absolute Maximum:	+7 VDC
Supply Current:	
1 MHz to 26 MHz:	15mA
26 MHz to 50 MHz:	30mA
Above 50 MHz:	38mA
Output Drive:	
HCMOS	
Symmetry:	50% ±10% @ 50% VDD
Rise & Fall Times:	20% to 80% VDD: T_r = 8ns max, T_f = 8ns max
Logic 0:	10% VDD max
Logic 1:	90% VDD min
Output Load:	50 pF max to 50 MHz, 30 pF > 50 MHz
TTL	
Symmetry:	50% ±10% @ 1.5V level
Rise & Fall Times:	0.5 to 2.5V: T_r = 8ns max, T_f = 8ns max
Logic 0:	0.5V max
Logic 1:	2.5V min
Output Load:	10 TTL to 50 MHz, 5 TTL > 50 MHz
Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-202, Method 211, Conditions A and C
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition B
Environmental:	
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

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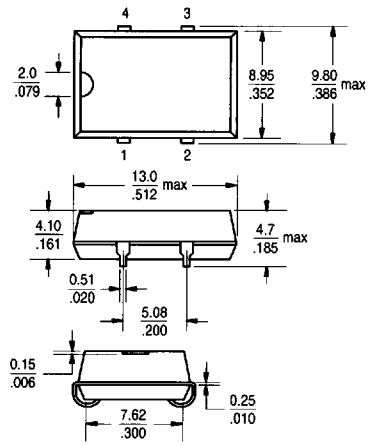
Tri-State Logic Table

Pin 1 Input	Pin 3 Output
Logic "1" or NC	Oscillation
Logic "0" or GND	High Impedance

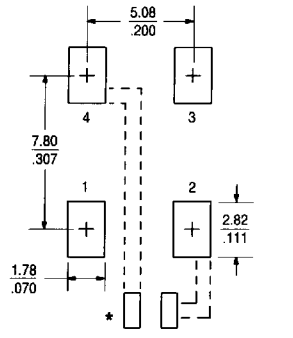
Required Input Levels on Pin 1:
Logic "1" = 2.0V min
Logic "0" = 0.8V max

Package Details, Type H



Pin Function:
Pin 1: Tri-State Control
Pin 2: GND
Pin 3: Output
Pin 4: +5 VDC

Recommended Land Pattern



Tolerance: $\frac{\pm.13}{\pm.005}$

* External high frequency power supply decoupling required.

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

NTH 06 H C - 4.0000

Series
NTH = CMOS - compatible
NTT = TTL - compatible

Frequency Range
03 = 1.0 to 3.9 MHz
06 = 4.0 to 23.9 MHz
08 = 24.0 to 70.0 MHz

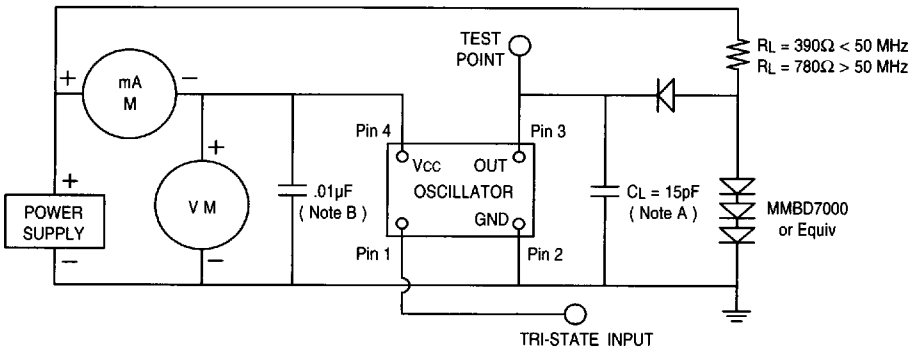
Package Type H

Stability Tolerance
C = ±100 ppm (0.010%)
B = ±50 ppm (0.005%)

Frequency

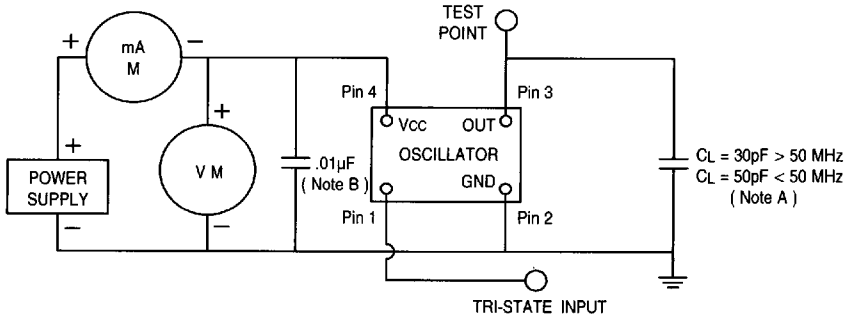
Example PN: NTH08HC - 36.0000

Test Circuits



NOTE: A. C_L includes probe and fixture capacitance.
NOTE: B. An external .01µF bypass capacitor close to package ground and V_{CC} pin is recommended

FIGURE 1 - TTL TEST CIRCUIT



NOTE: A. C_L includes probe and fixture capacitance.
NOTE: B. An external .01µF bypass capacitor close to package ground and V_{CC} pin is recommended

FIGURE 2 - HCMOS TEST CIRCUIT

All specifications are subject to change without notice.

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