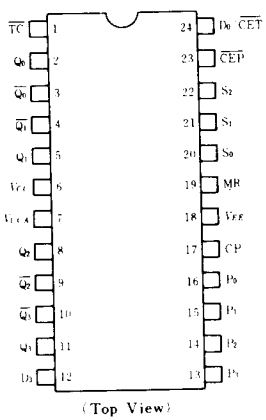
4-stage Counter /Shift Register

The HD100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (Sn) inputs determine the mode of operation, as shown in the mode select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multi-stage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (Do) input for shift-up operation.

For shift-down operation D_3 is the Serial Data input. In counting operation the Terminal Count ($\overline{TC}$) output goes low when the counter reaches 15 in the count/up mode or 0 in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the Do/$\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multi-stage counting or shift-up operation. The individual Preset (Pn) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A high signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, asynchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

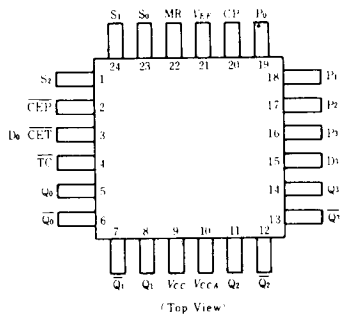
■ PIN ARRANGEMENT

● HD100136



(Top View)

● HD100136F



(Top View)

■ FUNCTION SELECT TABLE

S_0	S_1	S_2	Function
L	L	L	Load
L	H	L	Shift down
H	H	L	Shift up
L	L	H	Count down
L	H	H	Count up
H	H	H	Hold
H	L	L	Complement
H	L	H	Clear

H = High level
L = Low level

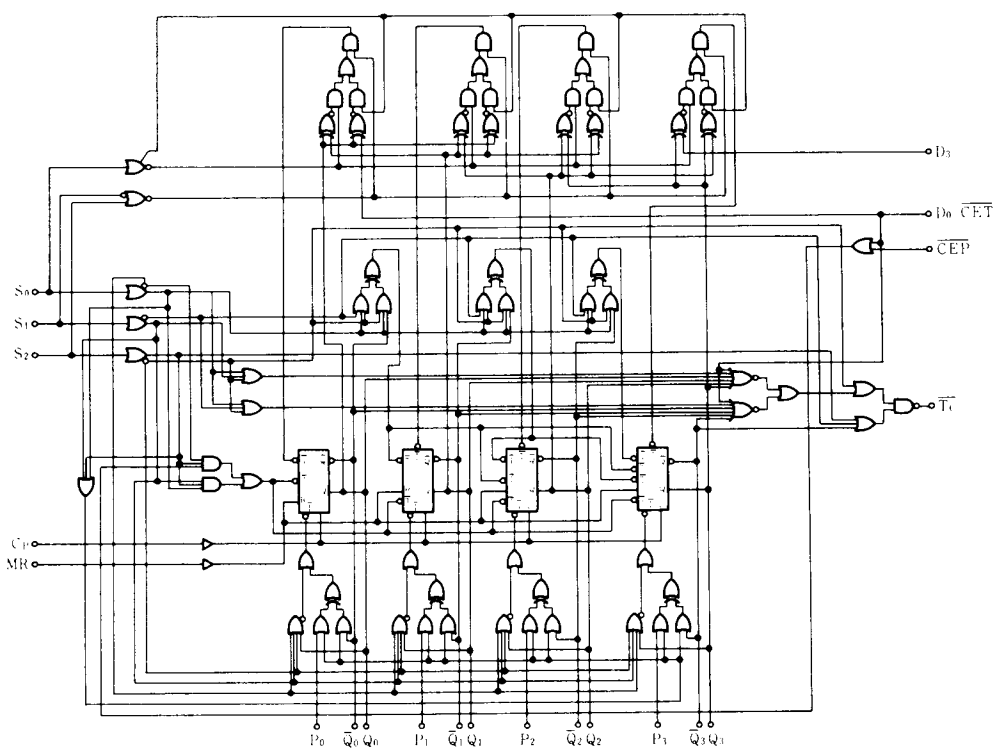
■TRUTH TABLE

Inputs								Outputs					
MR	S_0	S_1	S_2	$\overline{CEP}$	D_0 $\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	⎍	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	L	L	X	⎍	(Q_{0-3}) minus 1				①	Count Down
L	L	L	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ not active
L	L	L	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ not active
L	L	H	L	X	X	X	⎍	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	L	L	X	⎍	(Q_{0-3}) plus 1				②	Count Up
L	L	H	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ not active
L	L	H	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ not active
L	H	L	L	X	X	X	⎍	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	H	L	H	X	X	X	⎍	L	L	L	L	H	Clear
L	H	H	L	X	X	X	⎍	D_0	Q_0	Q_1	Q_2	Q_3	Shift Right
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	
H	L	L	H	X	L	X	X	L	L	L	L	L	
H	L	L	H	X	H	X	X	L	L	L	L	H	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	H	Asynchronous Master Reset
H	H	L	L	X	X	X	X	L	L	L	L	L	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = Lif $Q_0 - Q_3$ = LLLL Hif $Q_0 - Q_3$ = LLLL ② = Lif Q_0 Q_3 = HHHH Hif $Q_0 - Q_3$ = HHHH

H = HIGH Voltage Level L = Low Voltage Level X = Don't Care ⎍ = Low-to-HIGH Transition

■LOGIC DIAGRAM



HITACHI

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		136	195	283	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	P_n, S_n input	—	—	180	μA
			$\overline{CEP}$ input	—	—	200	
			MR input	—	—	240	
			D_3 input	—	—	280	
			CP input	—	—	390	
			$D_0/\overline{CEP}$ input	—	—	530	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100136

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Toggle Frequency	f_{TOG}			300	—	300	—	—	300	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See tes circuit and waveform	CP→Q	0.80	2.10	0.90	1.25	2.10	0.90	2.10	ns
			CP→$\overline{TC}$	1.60	4.50	1.70	3.10	4.50	1.70	4.50	
			MR→Q	1.30	2.65	1.35	1.85	2.65	1.35	2.65	
			MR→$\overline{TC}$	2.30	4.80	2.40	3.50	4.80	2.40	4.80	
			D_0/CET→$\overline{TC}$	1.40	2.80	**1.40**	1.90	2.80	**1.40**	2.80	
			S_n→$\overline{TC}$	1.20	3.30	1.30	2.25	3.30	1.30	3.30	
Transition Time	t_{TLH}, t_{THL}			0.40	1.70	0.40	0.95	1.70	0.40	1.70	ns
Setup Time	t_{SU}		D_n	1.10	—	1.20	—	—	1.20	—	ns
			P_n	1.50	—	1.60	—	—	1.60	—	
			D_0/CET, $\overline{CEP}$	1.35	—	1.45	—	—	1.45	—	
			S_n	3.10	—	3.20	—	—	3.20	—	
			MR (Release Time)	2.50	—	2.60	—	—	2.60	—	
Hold Time	t_h		D_n	−0.10	—	−0.10	—	—	−0.20	—	ns
			P_n	−0.25	—	−0.25	—	—	−0.35	—	
			D_0/CET, $\overline{CEP}$	**0.20**	—	**0.20**	—	—	**0.20**	—	
			S_n	−0.85	—	−0.85	—	—	−0.95	—	
Pulse Width	t_W		CP (H)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

● HD100136F

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Toggle Frequency	f_{TOG}			300	--	300	—	--	300	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	CP→Q	0.90	1.90	0.95	1.25	1.90	0.95	1.90	ns
			CP→$\overline{TC}$	1.75	4.35	1.75	3.10	4.35	1.75	4.50	
			MR→Q	1.30	2.65	1.40	2.00	2.65	1.40	2.65	
			MR→$\overline{TC}$	2.20	4.60	2.20	3.50	4.60	2.20	5.20	
			D_0/CET→$\overline{TC}$	1.30	3.00	1.40	1.70	3.00	1.40	3.30	
			S_n→$\overline{TC}$	1.20	3.60	1.20	2.25	3.60	1.20	4.10	
Transition Time	t_{TLH}, t_{THL}			0.40	1.70	0.40	0.80	1.70	0.50	1.70	ns
Setup Time	t_{SU}		D_n	0.90	--	0.90	—	--	1.00	—	ns
			P_n	1.50	-	1.50	--	—	1.60	--	
			D_n/CET, $\overline{CEP}$	1.50	-	1.50	-	—	1.60	-	
			S_n	3.20	-	3.20	-	--	3.50		
			MR (Release Time)	2.50		2.50	--		2.50	--	
Hold Time	t_h		D_n	−0.10	-	−0.20	--	—	−0.20		ns
			P_n	−0.40		−0.45		—	−0.45	--	
			D_n/CET, $\overline{CEP}$	−0.05	--	−0.10	-	--	−0.10	--	
			S_n	−0.85	-	−0.85	--	--	−0.85	-	
Pulse Width	t_W		CP (H)	2.00	-	2.00	-	—	2.00	-	ns
			MR (H)	2.00		2.00		—	2.00	--	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m s (500 linear fpm) is maintained.

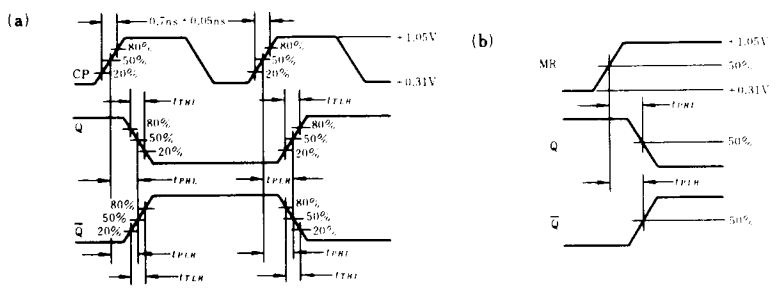


Fig.1 Propagation Delay Time

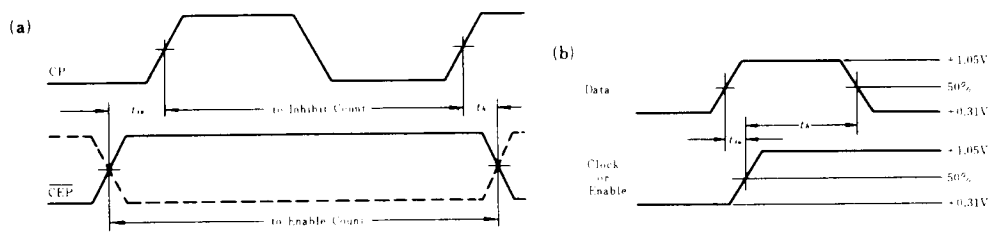


Fig.2 Set-up and Hold Time