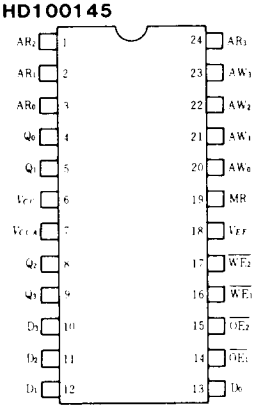
16×4 Read/Write Register File

The HD100145 is a 64-bit Register File organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting-up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the WRITE mode and the latches are in a HOLD mode. When either $\overline{WE}$ input is HIGH, the circuit is in the READ mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches and forces the outputs LOW.

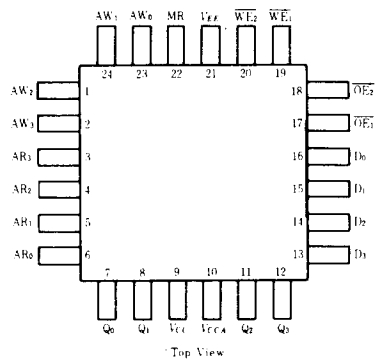
■ PIN ARRANGEMENT

●HD100145



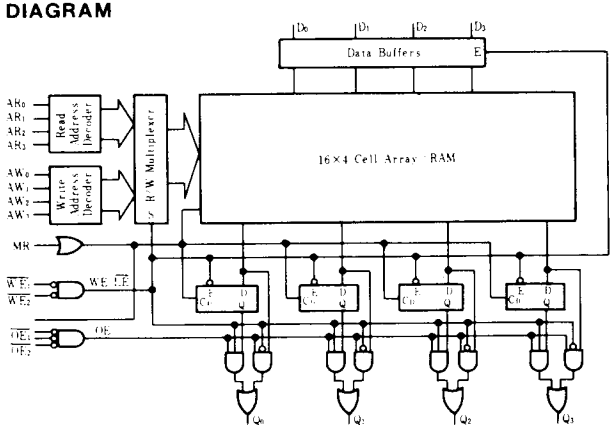
(Top View)

●HD100145F



(Top View)

■ LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	119	170	247	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$ WE $\overline{LE}$ input		–	270	μA
		All input except WE $\overline{LE}$			220	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100145

Item		Symbol	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Access Recovery Timing	Address Access	t_{AA}	2.00	7.40	2.00	5.50	7.40	2.00	7.40	ns
	Output Recovery	t_{OR}	0.80	3.10	0.80	2.20	3.10	0.80	3.30	
	Output Disable	t_{OD}	0.80	3.10	0.80	2.20	3.10	0.80	3.30	
Read Timing	Address Setup	t_{RSA1}	3.20	–	3.20	2.00	–	3.20	–	
	Output Delay	t_{WEQ}	2.00	6.10	2.00	4.50	6.10	2.00	6.60	
Outpul Latch Timing	Address Setup	t_{RSA2}	8.50	–	8.50	5.50	–	8.50	–	
	Address Hold	t_{RHA}	0.20		0.20	−2.00	–	0.20	–	
Write Timing	Address Setup	t_{WSA}	3.20	–	3.20	2.00	–	3.20	–	
	Address Hold	t_{WHA}	0.20		0.20	−1.30	–	0.20	–	
	Data Setup	t_{WSD}	9.20		9.20	6.00	–	9.20	–	
	Data Hold	t_{WHD}	0.20		0.20	−1.20	–	0.20		
	Min. Write Pulse Width	t_W	6.20	–	6.20	4.00	–	6.20	–	
	WE to $\overline{WE}$ Setup	t_{SW}	0.70	–	0.70	–	–	0.70	–	
	$\overline{WE}$ to $\overline{WE}$ Hold	t_{HW}	0.20	–	0.20	–	–	0.20	–	
Master Reset Timing	Min. Reset Pulse Width	t_M	4.50	–	4.50	–	–	4.50	–	
	$\overline{WE}$ Hold to Write	t_{MHW}	9.20	–	9.20	–	–	10.60		
	Output Disable	t_{MQ}	3.70		3.70	2.70	–	3.70		

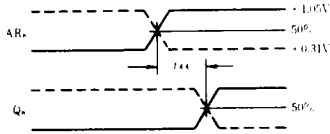
● HD100145F

Item		Symbol	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Access Recovery Timing	Address Access	t_{AA}	2.00	7.20	2.00	5.50	7.20	2.00	7.20	ns
	Output Recovery	t_{OR}	1.00	2.90	1.00	2.20	2.90	1.00	3.20	
	Output Disable	t_{OD}	1.00	2.90	1.00	2.20	2.90	1.00	3.20	
Read Timing	Address Setup	t_{RSA1}	3.00	–	3.00	2.00	–	3.00		
	Output Delay	t_{WEQ}	2.00	5.90	2.00	4.50	5.90	2.00	6.40	
Output Latch Timing	Address Setup	t_{RSA2}	8.30		8.30	5.50	–	8.30		
	Address Hold	t_{RHA}	0.00		0.00	−2.00	–	0.00		
Write Timing	Address Setup	t_{WSA}	3.00		3.00	2.00		3.00		
	Address Hold	t_{WHA}	0.00		0.00	−1.30	–	0.00		
	Data Setup	t_{WSD}	9.00	–	9.00	6.00		9.00		
	Data Hold	t_{WHD}	0.00		0.00	−1.20	–	0.00		
	Min. Write Pulse Width	t_W	6.00		6.00	4.00	–	6.50		
	WE to $\overline{WE}$ Setup	t_{SW}	0.50		0.50			0.50		
	$\overline{WE}$ to $\overline{WE}$ Hold	t_{HW}	0.00		0.00		–	0.00		
Master Reset Timing	Min. Reset Pulse Width	t_M	4.30		4.30			4.30		
	$\overline{WE}$ Hold to Write	t_{MHW}	9.00		9.00			10.40		
	Output Disable	t_{MQ}	3.50		3.50			3.50		

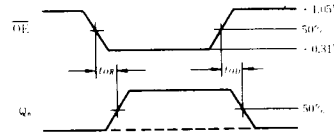
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■ TIMING RELATIONSHIPS

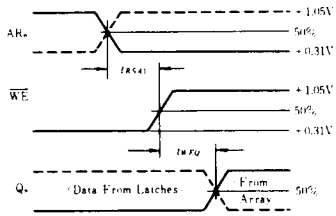
(a) Address Access Time
($\overline{WE}_1$, or $\overline{WE}_2$ = High ; $\overline{OE}_1 = \overline{OE}_2$ = Low)



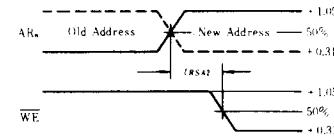
(b) Output Recovery/Disable Time
(unpulsed $\overline{OE}$ = Low)



(c) Read Timing, Address Set-up Time
(unpulsed $\overline{WE}$, $\overline{OE}_1$, $\overline{OE}_2$ = Low)



(d) Output Latch Timing, Address Set-up Time
(unpulsed $\overline{WE}$ = Low)



(e) Output Latch Timing, Address Hold Time
(unpulsed $\overline{WE}$ = Low)

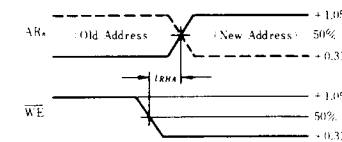
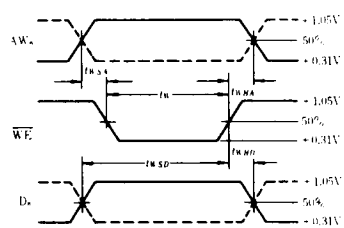


Fig.1 Read Timing

(a) Address and Data Set-up Time and Hold Time, Write Pulse Width (unpulsed $\overline{WE}$ = Low)



(b) $\overline{WE}$ Set-up and hold times, write with other $\overline{WE}$

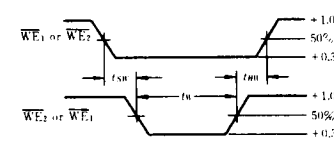
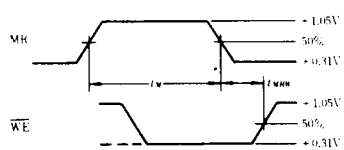


Fig.2 Write Timing

(a) Reset pulse width, $\overline{WE}$ hold time for subsequent writing (address already set-up, unpulsed $\overline{WE}$ = Low)



(b) Output reset delay, MR to Q$_n$

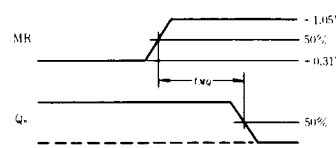


Fig.3 Master Reset Timing