NTP12N50

Preferred Device

Product Preview

TMOS 7 E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well–suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS 7

- Ultra Low On–Resistance Provides Higher Efficiency
- Reduced Gate Charge

Features Common to TMOS 7 and TMOS E–FETS

- Avalanche Energy Specified
- Diode Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	 V_{GS} V_{GSM}	 ±20 ±40	Vdc
Drain — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 12 10 42	Adc
Total Power Dissipation Derate above 25°C	P_D	202 1.61	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 V, V_{GS} = 10 Vdc, I_L = 12 A, L = 10 mH, R_G = 25 Ω)	E_{AS}	720	mJ
Thermal Resistance — Junction–to–Case — Junction–to–Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.62 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

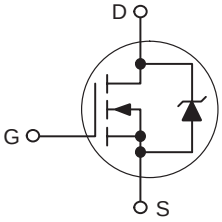
This document contains information on a new product. Specifications and information herein are subject to change without notice.

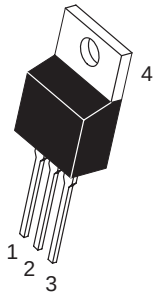
ON Semiconductor

http://onsemi.com

TMOS POWER FET
12 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.41 Ω

N–Channel





TO–220AB
CASE 221A
STYLE 5

PIN ASSIGNMENT	
1	Gate
2	Drain
3	Source
4	Drain

ORDERING INFORMATION

Device	Package	Shipping
NTP12N50	TO220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

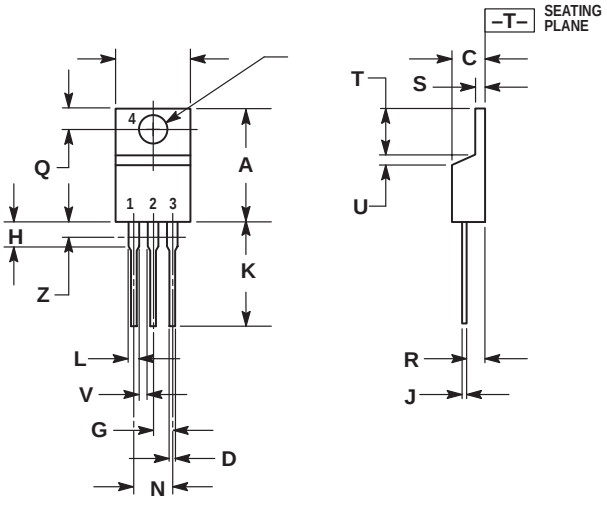
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	500 —	— 583	— —	Vdc mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J =125°C)	I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)	$I_{GSS(f)}$ $I_{GSS(r)}$	— —	— —	100 100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage I_D = 0.25 mA, V_{DS} = V_{GS} Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	2.5 6.7	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)	$R_{DS(on)}$	—	0.38	0.41	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 12 Adc) (V_{GS} = 10 Vdc, I_D = 6 Adc, T_J = 125°C)	$V_{DS(on)}$	— —	— —	5.9 5.2	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 6 Adc)	g_{FS}	8.0	11	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1800	2520	pF
Output Capacitance		C_{oss}	—	620	870	
Transfer Capacitance		C_{rss}	—	40	80	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	20	ns
Rise Time		t_r	—	27	50	
Turn–Off Delay Time		$t_{d(off)}$	—	52	100	
Fall Time		t_f	—	35	70	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc)	Q_T	—	37	50	nC
		Q_1	—	8.0	—	
		Q_2	—	12	—	
		Q_3	—	20	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage(1)	(I_S = 12 Adc, V_{GS} = 0 Vdc) (I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.90 0.80	1.0 —	Vdc
Reverse Recovery Time	(I_S = 12 Adc, V_{GS} = 0 Vdc, di_S/dt = 100 A/μs)	t_{rr}	—	380	—	ns
		t_a	—	165	—	
		t_b	—	215	—	
Reverse Recovery Stored Charge		Q_{RR}	—	3.9	—	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

TO–220AB
CASE 221A–09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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Literature Distribution Center for ON Semiconductor
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CENTRAL/SOUTH AMERICA:
Spanish Phone: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
Email: ONlit–spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5740–2745
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.