

# NTP12N50

Preferred Device

## Product Preview

### TMOS 7 E-FET™

## Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

This advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well-suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

#### New Features of TMOS 7

- Ultra Low On-Resistance Provides Higher Efficiency
- Reduced Gate Charge

#### Features Common to TMOS 7 and TMOS E-FETS

- Avalanche Energy Specified
- Diode Characterized for Use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature

#### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	500	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0\text{ M}\Omega$ )	$V_{DGR}$	500	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ( $t_p \leq 10\text{ ms}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 40$	Vdc
Drain — Continuous — Continuous @ $100^\circ\text{C}$ — Single Pulse ( $t_p \leq 10\text{ }\mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	12 10 42	Adc
Total Power Dissipation Derate above $25^\circ\text{C}$	$P_D$	202 1.61	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 100\text{ V}$ , $V_{GS} = 10\text{ Vdc}$ , $I_L = 12\text{ A}$ , $L = 10\text{ mH}$ , $R_G = 25\text{ }\Omega$ )	$E_{AS}$	720	mJ
Thermal Resistance — Junction-to-Case — Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.62 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

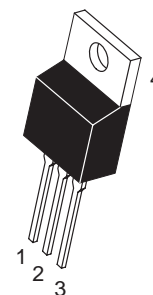
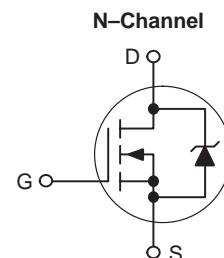
This document contains information on a new product. Specifications and information herein are subject to change without notice.



ON Semiconductor

<http://onsemi.com>

**TMOS POWER FET**  
**12 AMPERES**  
**500 VOLTS**  
 **$R_{DS(on)} = 0.41\text{ }\Omega$**



**TO-220AB**  
**CASE 221A**  
**STYLE 5**

#### PIN ASSIGNMENT

1	Gate
2	Drain
3	Source
4	Drain

#### ORDERING INFORMATION

Device	Package	Shipping
NTP12N50	TO220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

# NTP12N50

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	500 —	— 583	— —	Vdc mV/°C
Zero Gate Voltage Collector Current (V <sub>DS</sub> = 500 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 500 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS(f)</sub> I <sub>GSS(r)</sub>	— —	— —	100 100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage I <sub>D</sub> = 0.25 mA, V <sub>DS</sub> = V <sub>GS</sub> Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 —	2.5 6.7	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 6 Adc)	R <sub>DS(on)</sub>	—	0.38	0.41	Ohm
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 12 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 6 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	— —	5.9 5.2	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 6 Adc)	g <sub>FS</sub>	8.0	11	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	1800	2520	pF
Output Capacitance		C <sub>oss</sub>	—	620	870	
Transfer Capacitance		C <sub>rss</sub>	—	40	80	

### SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V <sub>DD</sub> = 250 Vdc, I <sub>D</sub> = 12 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	12	20	ns
Rise Time		t <sub>r</sub>	—	27	50	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	52	100	
Fall Time		t <sub>f</sub>	—	35	70	
Gate Charge	(V <sub>DS</sub> = 400 Vdc, I <sub>D</sub> = 12 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	37	50	nC
		Q <sub>1</sub>	—	8.0	—	
		Q <sub>2</sub>	—	12	—	
		Q <sub>3</sub>	—	20	—	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage <sup>(1)</sup>	(I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	— —	0.90 0.80	1.0 —	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	380	—	ns
		t <sub>a</sub>	—	165	—	
		t <sub>b</sub>	—	215	—	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	3.9	—	μC

### INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—	

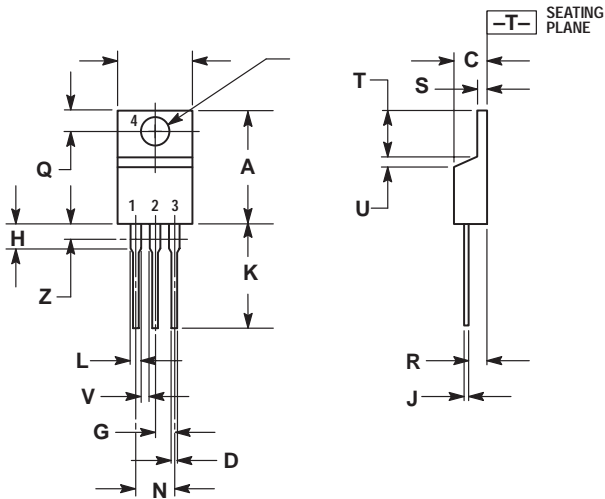
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

# NTP12N50

## PACKAGE DIMENSIONS

TO-220AB  
CASE 221A-09  
ISSUE Z




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

E-FET is a trademark of Semiconductor Components Industries, LLC.  
TMOS is a registered trademark of Semiconductor Components Industries, LLC.

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### **NORTH AMERICA Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, England, Ireland

### **CENTRAL/SOUTH AMERICA:**

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
**Phone:** 81-3-5740-2745

**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.