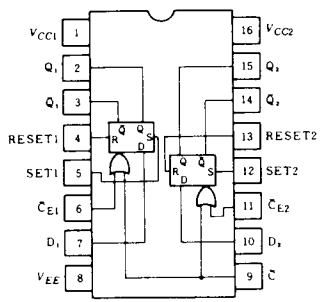
Dual D-type Latches

The HD10130 is a clocked dual D-type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode the enable inputs perform the function of controlling the common clock($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information. The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■PIN ARRANGEMENT



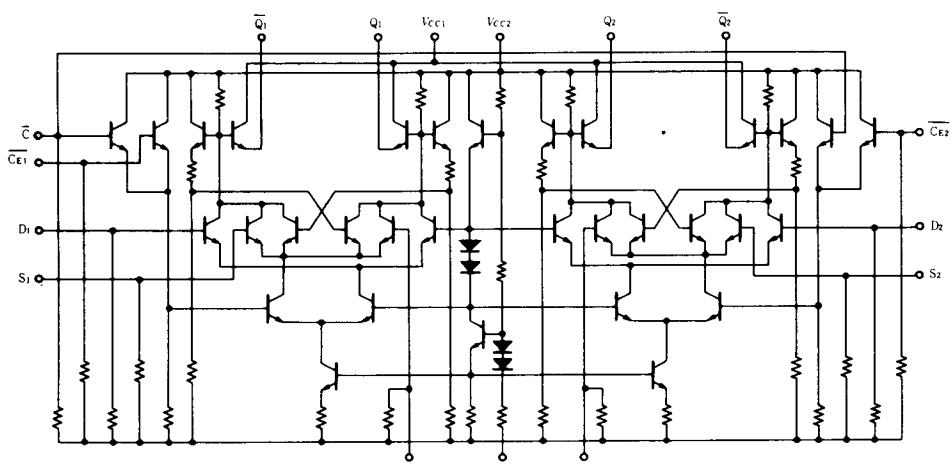
(Top View)

■FUNCTION TABLE

D	$\overline{C}$	$\overline{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× : Don't care.

■CIRCUIT SCHEMATIC



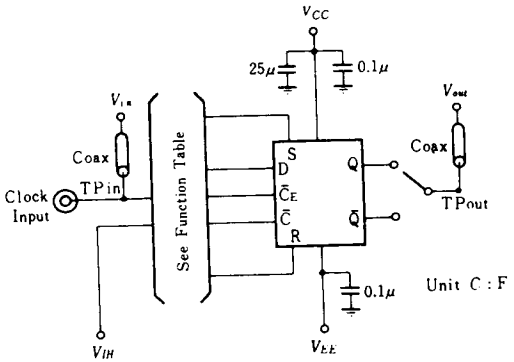
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

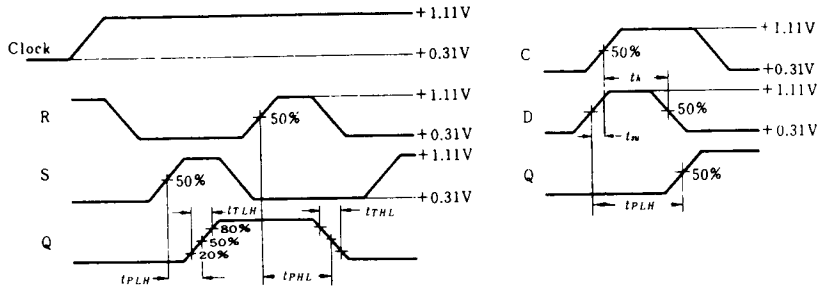
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	30	35	mA
Input Current	I_{IH}	$V_{IN}=-0.810V$	$\overline{C_E}$	25°C	—	—	220	μA
			$\overline{C}$		—	—	265	
			R, S, $\overline{C}$		—	—	285	
		$V_{IH}=-0.810V$, $\overline{C}=-1.850V$	D, S		—	—	285	
	I_{IL}	$V_{IL}=-1.850V$		25°C	—	—	0.5	μA
Output Voltage	V_{OH}	S=−0.890V		−30°C	−1.060	—	−0.890	V
		S=−0.810V		25°C	−0.960	—	−0.810	
		S=−0.700V		85°C	−0.890	—	−0.700	
	V_{OL}	R=−0.890V		−30°C	−1.890	—	−1.675	V
		R=−0.810V		25°C	−1.850	—	−1.650	
		R=−0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$\overline{C}=-1.890V$, D=−1.205V		−30°C	−1.080	—	—	V
		$\overline{C}=-1.850V$, D=−1.105V		25°C	−0.980	—	—	
		$\overline{C}=-1.825V$, D=−1.035V		85°C	−0.910	—	—	
	V_{OLA}	$\overline{C}=-1.890V$		−30°C	—	—	−1.655	V
		$\overline{C}=-1.850V$		25°C	—	—	−1.630	
		$\overline{C}=-1.825V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	$R_L=50\Omega$	−30°C	1.0	—	3.6	ns
					25°C	1.0	2.5	3.5	
					85°C	1.0	—	3.8	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	2.5	3.5	
					85°C	1.0	—	3.8	
	t_{PLH}	S, R	Q, $\overline{Q}$		−30°C	1.0	—	3.6	ns
					25°C	1.0	2.7	3.5	
					85°C	1.1	—	3.9	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	2.7	3.5	
					85°C	1.1	—	3.9	
	t_{PLH}	$\overline{C_E}$	Q, $\overline{Q}$		−30°C	1.0	—	4.3	ns
					25°C	1.0	—	4.0	
					85°C	1.0	—	4.1	
	t_{PHL}				−30°C	1.0	—	4.3	ns
					25°C	1.0	—	4.0	
					85°C	1.0	—	4.1	
Rise/Fall Time	t_{TLH}	D	Q, $\overline{Q}$		−30°C	1.0	—	3.6	ns
					25°C	1.1	2.7	3.5	
					85°C	1.1	—	3.8	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	2.7	3.5	
					85°C	1.1	—	3.8	
Setup Time	t_{su}	$\overline{C_E}$, D	Q, $\overline{Q}$		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns

■TEST CIRCUIT





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.