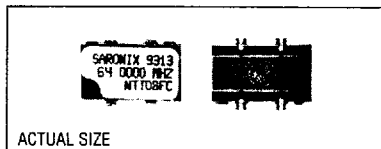
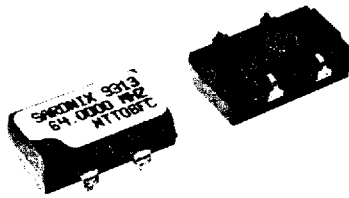


Technical Data

NTH / NTT Series, Type F



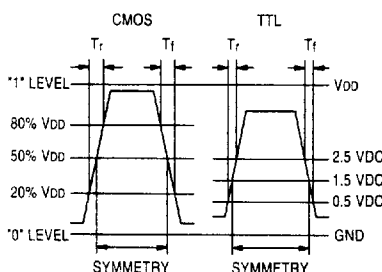
Description

A crystal controlled, low current oscillator providing rise and fall times to drive HCMOS and NMOS microprocessors. The plastic-molded surface mountable package is ideal for today's automated assembly environments. J-leads are compatible with EIA standard footprints. The HCMOS device is capable of driving both CMOS and TTL loads.

Applications & Features

- Compact, plastic-molded, surface mountable package
- TTL and CMOS compatible
- Tri-State output
- Ideally suited for use with contemporary MPU's i386, i486, 68040, custom ASIC's.

Output Waveform



Frequency Range: 1 MHz to 70 MHz

Frequency Stability: ± 50 or ± 100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.

Temperature Range:

Operating: 0°C to $+70^{\circ}\text{C}$
Storage: -55°C to $+125^{\circ}\text{C}$

Supply Voltage:

Recommended Operating: $+5\text{ VDC} \pm 10\%$
Absolute Maximum: $+7\text{ VDC}$

Supply Current:

1 MHz to 24 MHz: 10mA typical, 15mA max @ 25°C
20mA max over operating temperature range
Above 24 MHz: 20mA typical, 30mA max @ 25°C
35mA max over temperature range

Output Drive:

HCMOS

Symmetry: $50\% \pm 10\%$ @ $50\% V_{DD}$
 $50\% \pm 5\%$ to 50 MHz @ $50\% V_{DD}$ (Available)
Rise & Fall Times: 20% to 80% V_{DD} : $T_r = 8\text{ns max}$, $T_f = 8\text{ns max}$
Logic 0: 10% V_{DD} max
Logic 1: 90% V_{DD} min
Output Load: 50 pF max to 50 MHz, 30 pF > 50 MHz

TTL

Symmetry: $50\% \pm 10\%$ @ 1.5V
 $50\% \pm 5\%$ to 50 MHz @ 1.5V (Available)
Rise & Fall Times: 0.5 to 2.5V: $T_r = 8\text{ns max}$, $T_f = 8\text{ns max}$
Logic 0: 0.5V max
Logic 1: 2.5V min
Output Load: 10 TTL

Mechanical:

Shock: MIL-STD-883, Method 2002, Condition B
Solderability: MIL-STD-883, Method 2003
Terminal Strength: MIL-STD-202, Method 211, Conditions A and C
Vibration: MIL-STD-883, Method 2007, Condition A
Solvent Resistance: MIL-STD-202, Method 215
Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition B

Environmental:

Thermal Shock: MIL-STD-883, Method 1011, Condition A
Moisture Resistance: MIL-STD-883, Method 1004

Technical Data

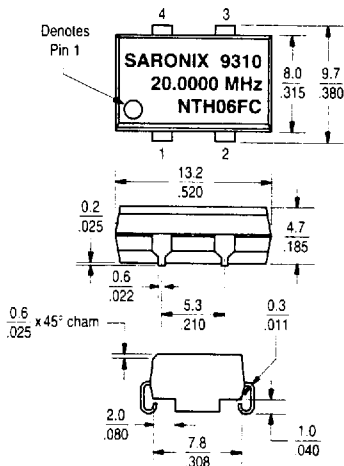
NTH / NTT Series, Type F

Tri-State Logic Table

Pin 1 Input	Pin 3 Output
Logic "1" or NC	Oscillation
Logic "0" or GND	High Impedance

Required Input Levels on Pin 1:
 Logic "1" = 3.0V min
 Logic "0" = 0.5V max

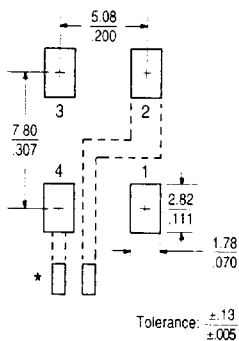
Package Details, Type F



Pin Function:

Pin 1: Tri-State Control
 Pin 2: GND
 Pin 3: Output
 Pin 4: +5 VDC

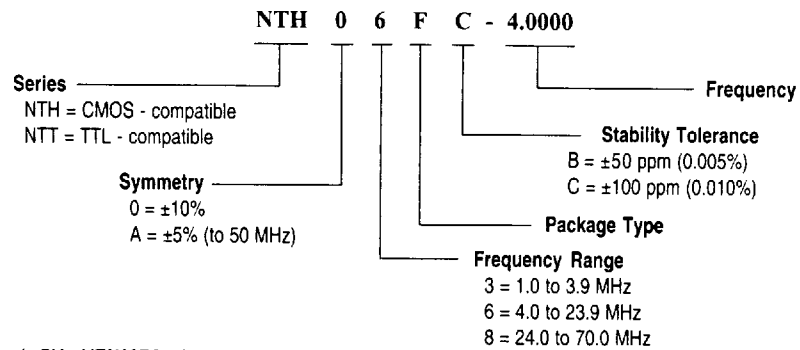
Recommended Land Pattern



* External high frequency power supply decoupling required.

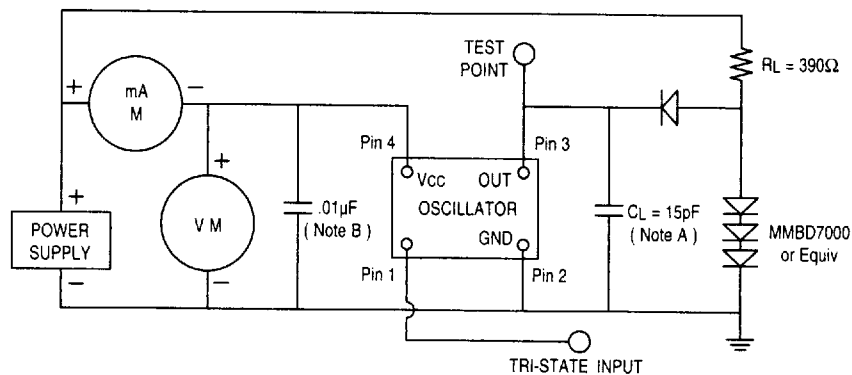
Scale: None (Dimensions in mm / inches)

Part Numbering Guide



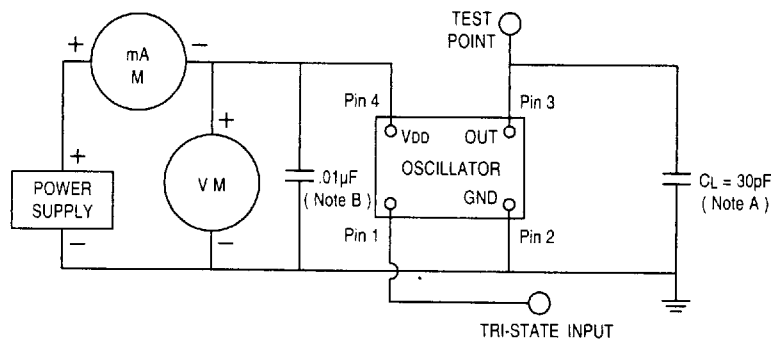
Example PN: NTH08FC - 36.0000

Test Circuits



NOTE: A. CL includes probe and fixture capacitance.
 NOTE: B. An external .01µF bypass capacitor close to package ground and VCC pin is recommended

FIGURE 1 - TTL TEST CIRCUIT



NOTE: A. CL includes probe and fixture capacitance.
 NOTE: B. An external .01µF bypass capacitor close to package ground and VDD pin is recommended

FIGURE 2 - HCMOS TEST CIRCUIT

All specifications are subject to change without notice.

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