HD404678 Series

Description

The HD404678 Series is a 4-bit single-chip HMCS400 series microcomputer for telephone applications designed to increase program productivity. It features a high-precision dual-tone multi-frequency (DTMF) receiver that is especially suitable for answering machines.

The HD404678 Series includes three chips: the HD404676 with 6-kword ROM; the HD404678 with 8-kword ROM; and the HD4074678 with 8-kword PROM (ZTAT™ version).

The HD4074678 is a PROM version (ZTAT™) microcomputer. A program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™ version is 27256-compatible.)

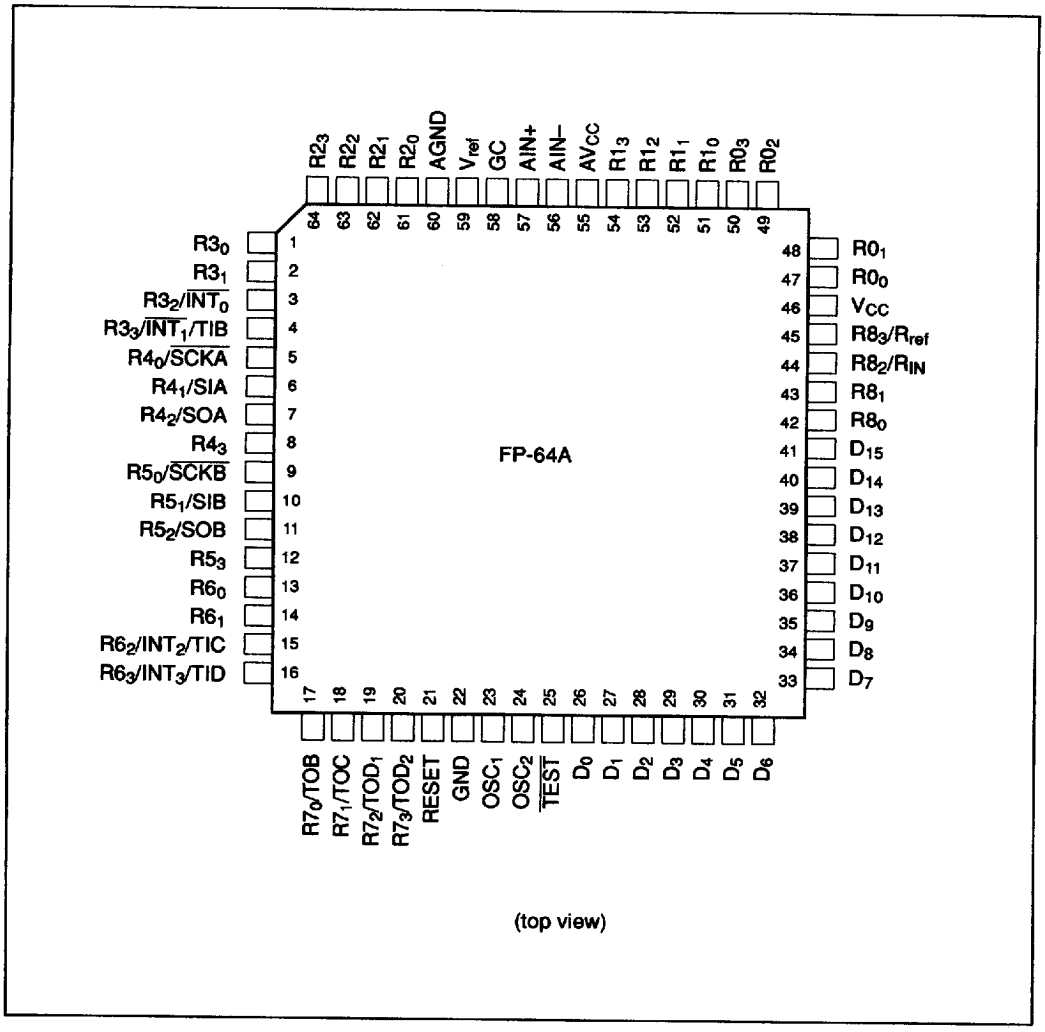
Features

- 6,144-word × 10-bit ROM (HD404676)
- 8,192-word × 10-bit ROM (HD404678, HD4074678)
- 512-digit × 4-bit RAM
- 48 I/O pins and four dedicated input pins
  - — 16 high-current output pins: Ten 15-mA sinks (a maximum of 7 pins can be used at the same time) and six 10-mA sources
- Four timer/counters
  - — One 8-bit free-running timer
  - — Three 8-bit auto-reload timer/counter output circuits
- Two-channel clock-synchronous 8-bit serial interface
- Built-in DTMF receiver
- Reset voltage variable function
- 11 interrupt sources
  - — Four by external sources
  - — Four by timer/counters sources
  - — Two by serial interface sources
  - — One by DTMF receiver source
- Subroutine stack up to 16 levels, including interrupts
- Instruction cycle time: 2 µs
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- Package
  - — 64-pin flat plastic package (FP-64A)
- Operation modes
  - — MCU mode
  - — PROM mode (HD4074678)

Ordering Information

Type	Product Name	Model Name	ROM (Words)	Package
Mask ROM	HD404676	HD404676H	6,144	FP-64A
	HD404678	HD404678H	8,192	FP-64A
ZTAT™	HD4074678	HD4074678H	8,192	FP-64A

Pin Arrangement



(top view)

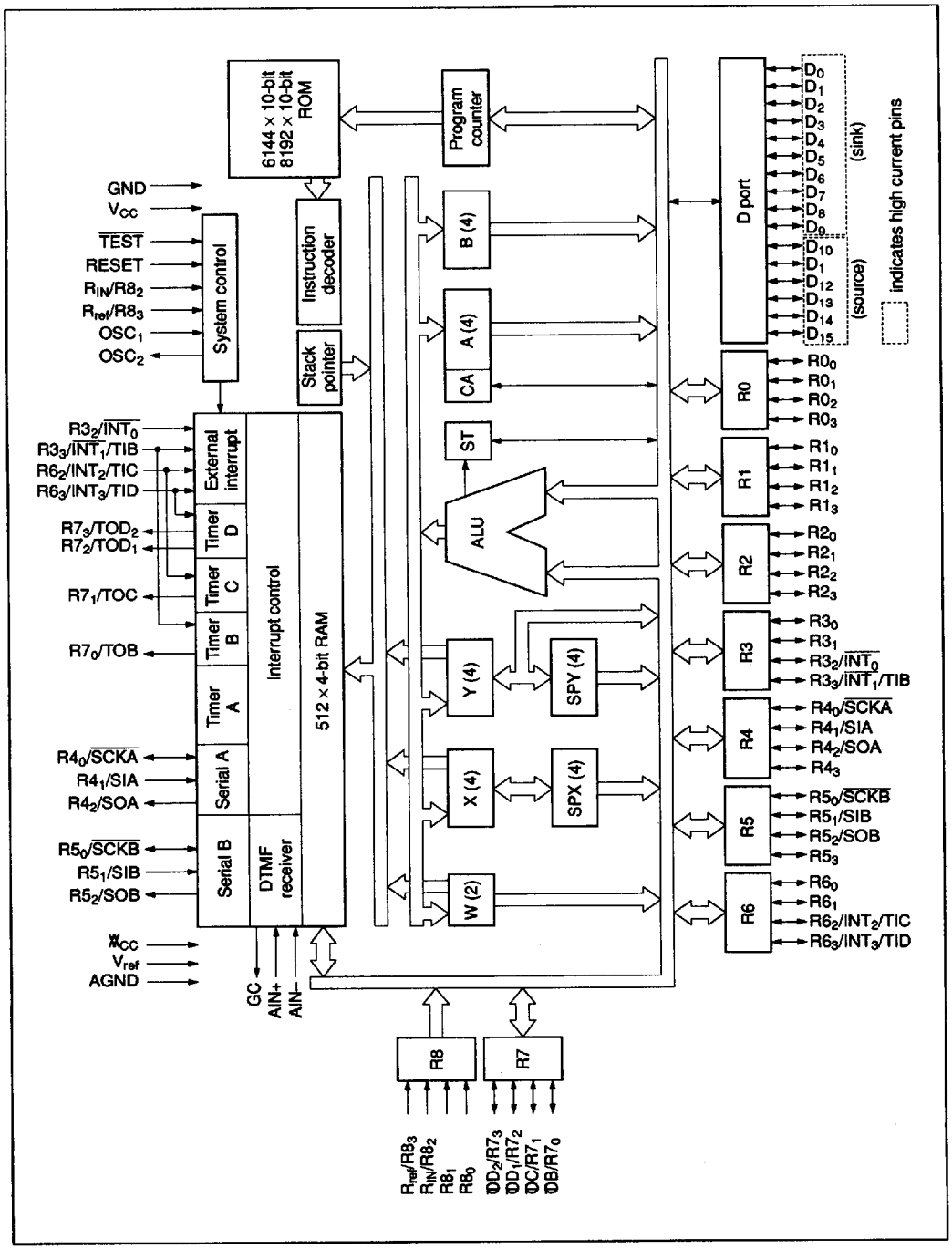
Pin Description

Function	Symbol	Pin No.	I/O	Description
Power	V_{CC}	46		Power supply voltage (5 V ± 10%).
	GND	22		Connected to ground.
Test	$\overline{TEST}$	25		Used for factory tests. Connected to V_{CC}.
Reset	RESET	21	I	Resets the MCU.
Oscillator	OSC_1	23	I	Input or output pins for the internal oscillator circuit. Connected to the crystal oscillator or external oscillation circuit.
	OSC_2	24	O	External oscillation circuit can be connected to OSC_1.
Port	D_0–D_9	26–35	I/O	Input/output ports. All bits can be accessed separately. Port pins are large current sink pins with pull-up MOS.
	D_{10}–D_{15}	36–41	I/O	Input/output ports. All bits can be accessed separately. Port pins are large current source pins with pull-down MOS.
	$R0_0$–$R7_3$	1–20, 47–54, 61–64	I/O	Input/output ports accessed with 4-bit-wide digits. Pins $R0_0$–$R5_3$ are standard pins with pull-up MOS while $R6_0$–$R7_3$ each has pull-down MOS.
	$R8_0$–$R8_3$	42–45	I	An input port accessed with 4-bit-wide digits. Port pins are standard pins with pull-down MOS.
Interrupt	$\overline{INT_0}$, $\overline{INT_1}$ INT_2, INT_3	3, 4 15, 16	I	External interrupts. These pins are multiplexed with $R3_2$, $R3_3$/TIB, $R6_2$/TIC, and $R6_3$/TID, respectively.
Serial interface	$\overline{SCKA}$, $\overline{SCKB}$	5, 9	I/O	Transmit clock input/output pins for serial interface A and serial interface B.
	SIA, SIB	6, 10	I	Receive data input pins for serial interface A and serial interface B.
	SOA, SOB	7, 11	O	Transmit data output pins for serial interface A and serial interface B.
Timer	TIB, TIC, TID	4, 15, 16	I	External clock input pins for timers B, C, and D. These pins are multiplexed with $R3_3/\overline{INT_1}$, $R6_2/INT_2$, and $R6_3/INT_3$, respectively.
	TOB, TOC, TOD_1, TOD_2	17–20	O	Timer output pins for timers B, C, and D. These pins are multiplexed with $R7_0$, $R7_1$, $R7_2$, and $R7_3$, respectively.
DTMF receiver	AV_{CC}	55		Power supply pin for the DTMF receiver analog block. Connect it as close as possible to the power supply to set AV_{CC} at the same potential as V_{CC}. Stabilized power supply must be applied.

Pin Description (cont)

Function	Symbol	Pin No.	I/O	
DTMF receiver (cont)	AGND	60		Power supply pin for the DTMF receiver analog block. Connect it as close as possible to the power supply to put AGND to the same potential as GND.
	R_{ref}	59		DTMF receiver analog block reference voltage. A stabilized voltage $AV_{CC}/2$ must be applied.
	AIN+, AIN–	57, 56	I	DTMF signal input pins for the DTMF receiver.
	GC	58	O	DTMF receiver gain control pin.
Reset voltage variable circuit	R_{ref}	45	I	A reference voltage input pin for threshold voltage of the reset voltage, variable circuitry. R_{ref} is multiplexed with $R8_3$.
	R_{IN}	44	I	An analog input pin of the reset voltage variable circuit. R_{IN} is multiplexed with $R8_2$.

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1, and the ROM is described in detail below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After an MCU reset or interrupt execution, the program starts from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to the subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Reserved for ROM data that can be referenced as a pattern by the P instruction.

Program area ($0000–$17FF (HD404676), $0000–$1FFF (HD404678, HD4074678)): Used for program code.

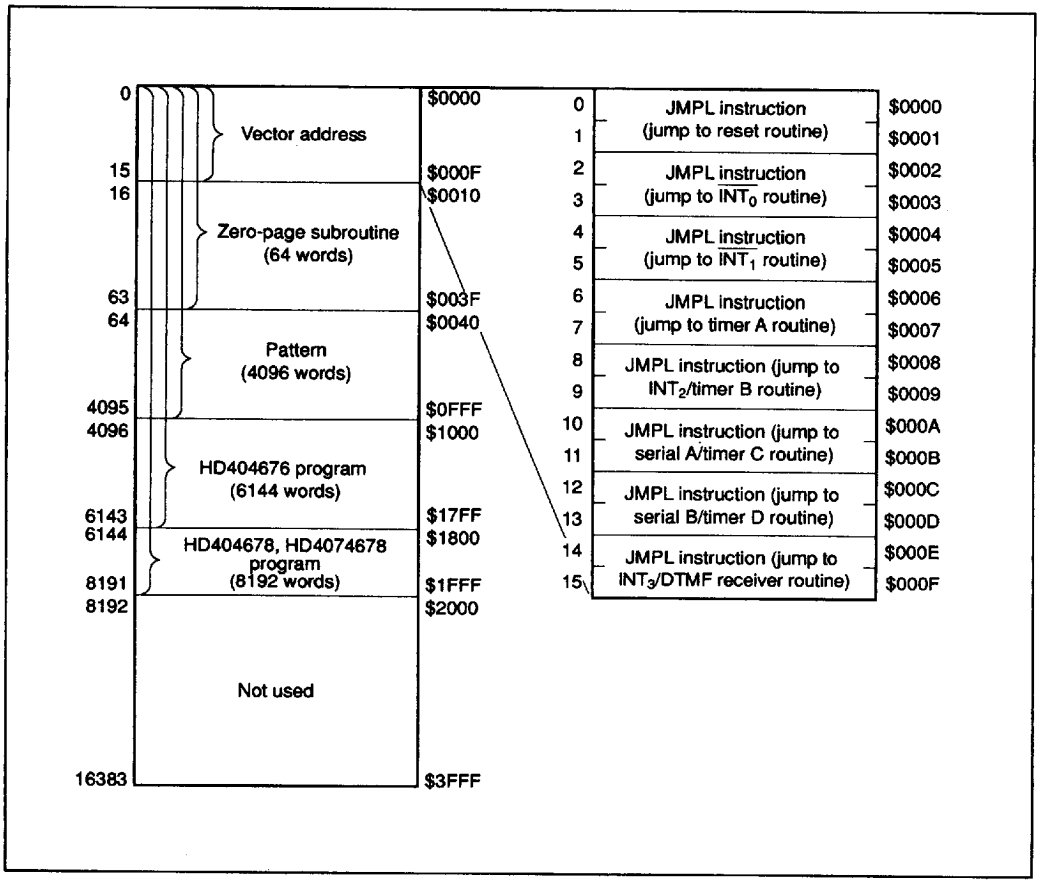


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 512-digit × 4-bit RAM area for data and stack areas. In addition, interrupt control bits, special function registers, and a display data RAM area are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and the RAM area is described in detail below.

Interrupt Control Bit Area ($000–$003, $022–$023): Used for interrupt control (figure 3). It can be accessed only by RAM bit manipulation instructions. However, note that the interrupt request flag cannot be set by software, and the RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004–$01F, $024–$03F): Used as mode registers for external interrupts, the serial interface, the timer, and as data control registers and data registers for I/O ports. As shown in figure 2, there are three types of registers: read-only, write-only, and read/write (table 1). DTMF receiver related registers ($024–$02C) are shown in table 29.

Register Flag Area ($020–$021): Used for the WDON flag which is accessed by RAM bit manipulation instructions. The WDON flag can only be set by the SEM and SEMD instructions. This flag is shown in figure 4.

Data Area ($040–$04F, $070–$21F): The memory register (MR), which is 16 digits ($040–$04F) long, can also be accessed by the LAMR and XMRA instructions (figure 5).

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine calls (CAL, CALL) and interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The stack area and data to be saved in it are shown in figure 5.

The program counter is popped from the stack by the RTN and RTNI instructions, but the status and carry flags can only be popped from the stack by the RTNI instruction. Any unused area is available for data storage.

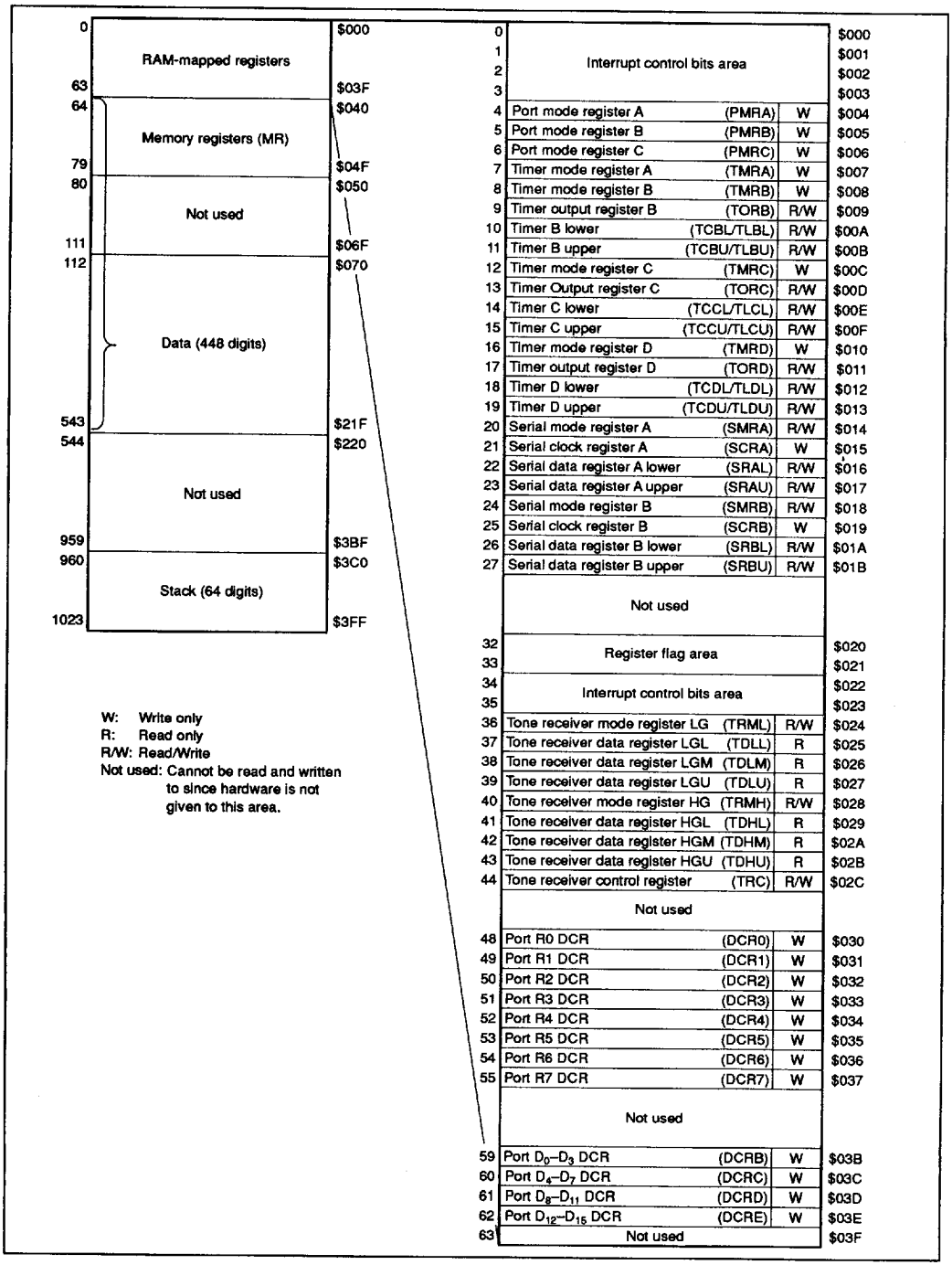


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset stack pointer bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMSA (IM of serial A)	IFSA (IF of serial A)	IM2 (IM of INT_2)	IF2 (IF of INT_2)	$002
3	IM3 (IM of INT_3)	IF3 (IF of INT_3)	IMSB (IM of serial B)	IFSB (IF of serial B)	$003
34	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$022
35	IMTR (IM of tone receiver)	IFTR (IF of tone receiver)	IMTD (IM of timer D)	IFTD (IF of timer D)	$023

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, is reset by the REM/REMD instruction, and is tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction.
The value of the status flag becomes invalid when the unused bits and RSP bit are tested by the TM/TMD instruction.

Figure 3 Configuration of Interrupt Control Bits Area

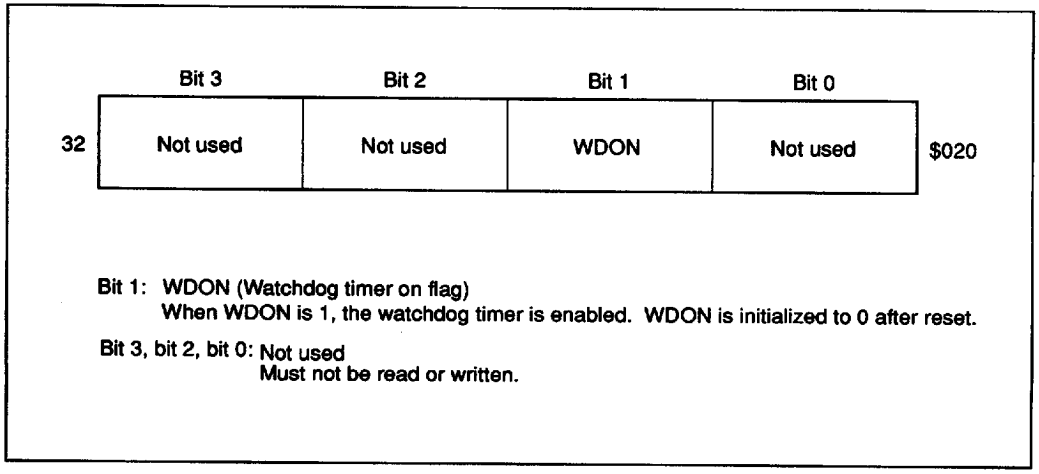


Figure 4 Configuration of Register Flag Area

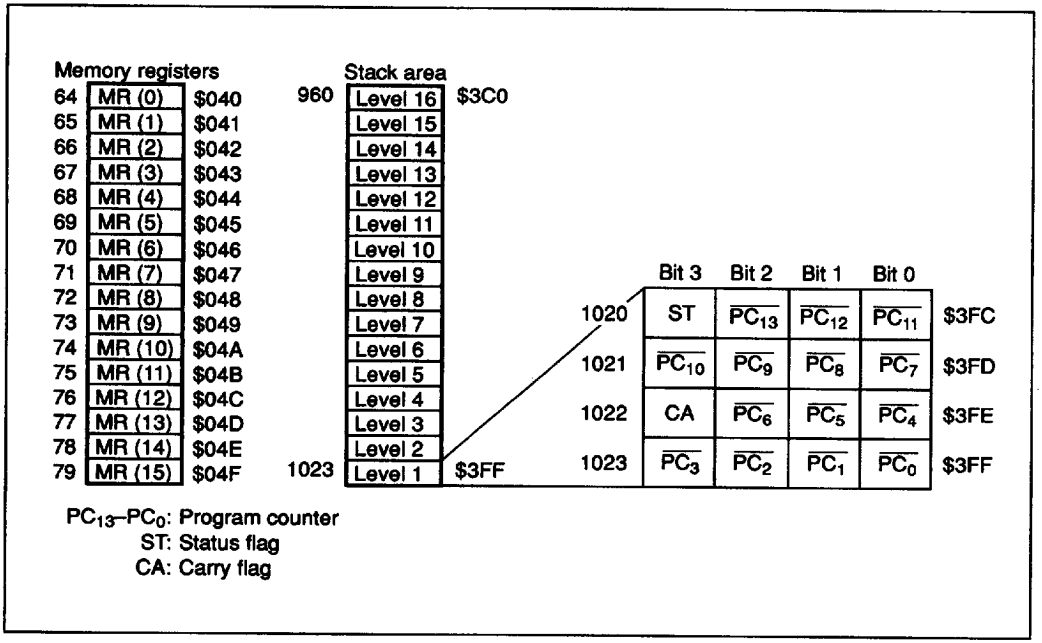


Figure 5 Configuration of Memory Register, Stack Area, and Stack Position

Table 1 Special Registers

Name	Address	Bit	Function
PMRA	$004	0	Selects $R3_2/\overline{INT_0}$ pin mode
		1	Selects $R3_3/\overline{INT_1}$ pin mode
		2	Selects $R6_2/INT_2$ pin mode
		3	Selects $R6_3/INT_3$ pin mode
PMRB	$005	0	Selects $R4_2$ pin circuit type (CMOS/NMOS open drain)
		1	Selects $R5_2$ pin circuit type (CMOS/NMOS open drain)
		2	Selects $R8_2/R_{IN}$ and $R8_3/R_{ref}$ pin modes
		3	Disables input fix resistor MOS
PMRC	$006	0	Selects $R7_0$/TOB pin mode
		1	Selects $R7_1$/TOC pin mode
		2	Selects $R7_2/TOD_1$ pin mode
		3	Selects $R7_3/TOD_2$ pin mode
TMRA	$007	0–2	Selects timer A input clock
		3	Resets timer A
TMRB	$008	0–2	Selects timer B input clock
		3	Enables auto-reload function
TORB	$009	0, 1	Selects timer B output mode
		2	Selects PWM operation (pulse width modulation)
		3	Not used
TCBL/ TLBL	$00A	0–3	Lower digit of timer counter/timer load register (timer B)
TCBU/ TLBU	$00B	0–3	Upper digit of timer counter/timer load register (timer B)
TMRC	$00C	0–2	Selects timer C input clock
		3	Enables auto-reload function
TORC	$00D	0, 1	Selects timer C output mode
		2	Selects PWM operation
		3	Not used
TCCL/ TLCL	$00E	0–3	Lower digit of timer counter/timer load register (timer C)
TCCU/ TLCU	$00F	0–3	Upper digit of timer counter/timer load register (timer C)
TMRD	$010	0–2	Selects timer D input clock
		3	Enables auto-reload function
TORD	$011	0, 1	Selects timer D output mode
		2	Selects PWM operation
		3	Not used

Table 1 Special Registers (cont)

Name	Address	Bit	Function
TCDL/ TLDL	$012	0–3	Lower digit of timer counter/timer load register (timer D)
TCDU/ TLDU	$013	0–3	Upper digit of timer counter/timer load register (timer D)
SMRA	$014	0	Selects $R4_2$/SOA pin mode
		1	Selects $R4_1$/SIA pin mode
		2	Selects $R4_0$/$\overline{SCKA}$ pin mode
		3	Enables STS for serial interface A
SCRA	$015	0–2	Selects transmit clock source (serial interface A)
		3	Not used
SRAL	$016	0–3	Serial data register A lower digit
SRAU	$017	0–3	Serial data register A upper digit
SMRB	$018	0	Selects $R5_2$/SOB pin mode
		1	Selects $R5_1$/SIB pin mode
		2	Selects $R5_0$/$\overline{SCKB}$ pin mode
		3	Enables STS for serial interface B
SCRB	$019	0–2	Selects transmit clock source (serial interface B)
		3	Not used
SRBL	$01A	0–3	Serial data register B lower digit
SRBU	$01B	0–3	Serial data register B upper digit
DCR0	$030	0–3	R0 port data control register
DCR1	$031	0–3	R1 port data control register
DCR2	$032	0–3	R2 port data control register
DCR3	$033	0–3	R3 port data control register
DCR4	$034	0–3	R4 port data control register
DCR5	$035	0–3	R5 port data control register
DCR6	$036	0–3	R6 port data control register
DCR7	$037	0–3	R7 port data control register
DCRB	$03B	0–3	D_0–D_3 port data control register
DCRC	$03C	0–3	D_4–D_7 port data control register
DCRD	$03D	0–3	D_8–D_{11} port data control register
DCRE	$03E	0–3	D_{12}–D_{15} port data control register

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 6 and described below.

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and to transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): A one-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

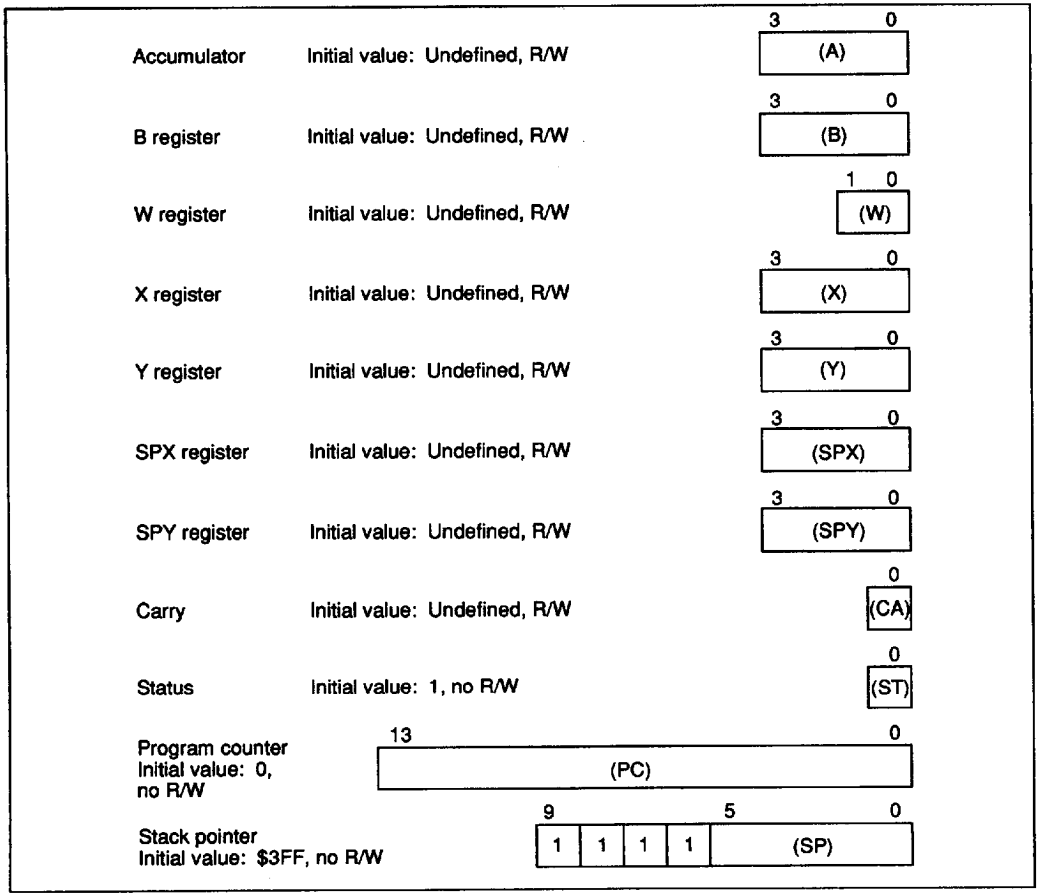


Figure 6 Registers and Flags

Status Flag (ST): A one-bit flag that indicates an ALU overflow or ALU non-zero generated during an arithmetic or compare instruction, or the result of a bit test instruction. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is fetched, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): A 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): A 10-bit pointer that contains the address of the stack area to be used as the next level. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top 4 bits of the SP are fixed to 1111, a stack of up to 16 levels can be used.

The SP is initialized to $3FF in two ways: by MCU reset or by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by setting the RESET pin high. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. In other cases, the RESET input for two instruction cycles resets the MCU.

Initial values of the registers and counters after MCU reset are listed in table 2.

Note that the reset signal is not acknowledged by the MCU from power-on until the oscillation stabilizes (t_{RC}), so the statuses within the MCU and at the I/O pins are not defined.

Table 2 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/ mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	With pull-up MOS ports $R0_0$–$R5_3$ and D_0–D_9	(PDR)	1	Pulled up with input state
	With pull-down MOS ports $R6_0$–$R8_3$ and D_{10}–D_{15}	(PDR)	0	Pulled down with input state (R8 port is a dedicated input port)
	Port mode registers A and C	(PMRA, PMRC)	0000	Refer to descriptions of port mode registers A and C
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Data control register	(DCR0–7, DCRB–D)	0000	Refer to Data Control Register section

Table 2 Initial Values After MCU Reset (cont)

Item			Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer mode registers B–D		(TMRB –TMRD)	0000	Refer to description of timer mode registers B–D
	Timer output registers B–D		(TORB –TORD)	0000	Refer to description of timer output registers B–D
	Timer mode register A		(TMRA)	0000	Refer to description of timer mode register A
	Serial mode registers A and B		(SMRA, SMRB)	0000	Refer to description of serial mode register
	Serial clock registers A and B		(SCRA, SCRB)	000	Refer to description of serial clock register
	Prescaler			$000	—
	Timer counter A		(TCA)	$00	—
	Timer/event counters B–D		(TCB –TCD)	$00	—
	Timer load registers B–D		(TLRB –TLRD)	$00	—
	Octal counter			000	—
DTMF receiver	Tone receiver control register		(TRC)	$0000	—
	Low-group	Tone receiver mode register	(TRML)	$0000	—
		Tone receiver data register	(TDLL, TDLM, TDLU)	$0000	—
	High-group	Tone receiver mode register	(TRMH)	$0000	—
		Tone receiver data register	(TDHL, TDHM, TDHU)	$0000	—

Note: The status of other registers and flags after MCU reset are shown on page 16.

Item	Abbr.	Status After Cancellation of Stop Mode by MCU Reset	After All Other MCU Reset
Carry flag	(CA)	Pre-MCU-reset value are not guaranteed: values must be initialized by software.	Pre-MCU-reset values are not guaranteed: values must be initialized by software.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data registers A, B	(SRA, SRB)		
RAM		Pre-MCU-reset (pre-STOP-instruction) are retained.	

Interrupts

The MCU has eleven interrupt sources: four external signals ($\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3) and seven internal requests (timer A, timer B, timer C, timer D, serial A, serial B, DTMFR). For each source, an interrupt request flag (IF) and an interrupt mask (IM) are provided to control and maintain the interrupt requests. To control total interrupt operations, the interrupt enable flag (IE) is provided.

Since the vector addresses are shared between timer B and INT_2, between serial A and timer C, between serial B and timer D, and between INT_3 and DTMFR, determining which request occurs must be done by software.

Interrupt Control Bits and Interrupt Processing: Locations $000 through $003 and $022 through $023 in RAM are reserved for the interrupt control bits which can only be accessed by RAM bit manipulation instructions. The interrupt request flags (IFs) can only be set by signals from interrupt sources. MCU reset initializes the interrupt enable flag (IE) and interrupt request flags (IFs) to 0 and the interrupt masks (IMs) to 1.

A block diagram of the interrupt control circuit is shown in figure 7, interrupt priorities and vector addresses are listed in table 3, and the interrupt processing conditions for the eleven interrupt sources are listed in table 4. An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, interrupt processing begins. A priority control logic generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 8, and an interrupt processing flowchart is shown in figure 9. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt routine, and reset the IF by a software instruction within the interrupt routine.

Table 3 Interrupt Function Table

Interrupt Source	Interrupt Generation	Priority	Interrupt Vector Address	Interrupt Control Bit Address					
				Interrupt Request Flag			Interrupt Mask		
				Symbol	Address	Bit	Symbol	Address	Bit
RESET	RESET pin = H Variable voltage reset mode ($R_{IN} > R_{ref}$) Timer A (WDT) overflow	Note	$0000						
$\overline{INT_0}$	$\overline{INT_0}$ pin falling edge detection	1	$0002	IF0	$000	2	IM0	$000	3
$\overline{INT_1}$	$\overline{INT_1}$ pin falling edge detection	2	$0004	IF1	$001	0	IM1	$001	1
Timer A	Timer A overflow	3	$0006	IFTA	$001	2	IMTA	$001	3
INT_2/ timer B	INT_2 pin rising edge detection	4	$0008	IF2	$002	0	IM2	$002	1
	Timer B overflow			IFTB	$022	0	IMTB	$022	1
Serial A/ timer C	Serial A transmit end Serial A transmit suspended	5	$000A	IFSA	$002	2	IMSA	$002	3
	Timer C overflow			IFTC	$022	2	IMTC	$022	3
Serial B/ timer D	Serial B transmit end Serial B transmit suspended	6	$000C	IFSB	$003	0	IMSB	$003	1
	Timer D overflow			IFTD	$023	0	IMTD	$023	1
INT_3/ DTMFR	INT_3 pin rising edge detection	7	$000E	IF3	$003	2	IM3	$003	3
	DTMF signal cycle measurement end			IFTR	$023	2	IMTR	$023	3

Note: Highest priority
- High input to the RESET pin
- Reset by watchdog timer mode
- Reset by variable voltage reset mode

Table 4 Conditions of Interrupt Processing

Interrupt Control Bit	Interrupt Source						
	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	INT_2/ Timer B	Serial A/ Timer C	Serial B/ Timer D	INT_3/ DTMFR
IE	1	1	1	1	1	1	1
IF0 • $\overline{IM0}$	1	0	0	0	0	0	0
IF1 • $\overline{IM1}$	*	1	0	0	0	0	0
IFTA • $\overline{IMTA}$	*	*	1	0	0	0	0
IF2 • $\overline{IM1}$	*	*	*	1/*	0	0	0
IFTB • $\overline{IMTB}$	*	*	*	*/1	0	0	0
IFSA • $\overline{IMSA}$	*	*	*	*	1/*	0	0
IFTC • $\overline{IMTC}$	*	*	*	*	*/1	0	0
IFSB • $\overline{IMSB}$	*	*	*	*	*	1/*	0
IFTD • $\overline{IMTD}$	*	*	*	*	*	*/1	0
IF3 • $\overline{IM3}$	*	*	*	*	*	*	1/*
IFTR • $\overline{IMTR}$	*	*	*	*	*	*	*/1

* Don't care.

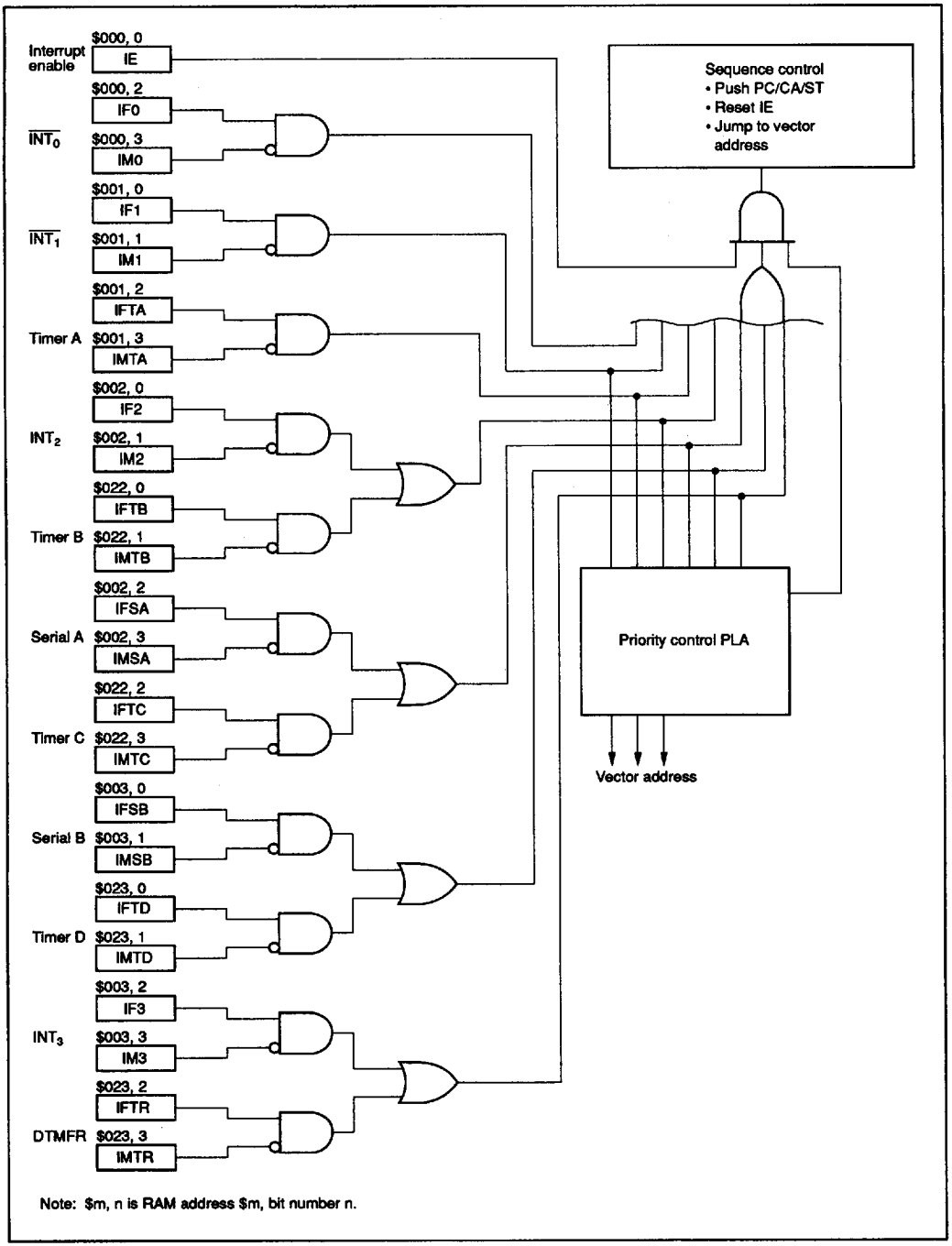


Figure 7 Interrupt Control Circuit Block Diagram

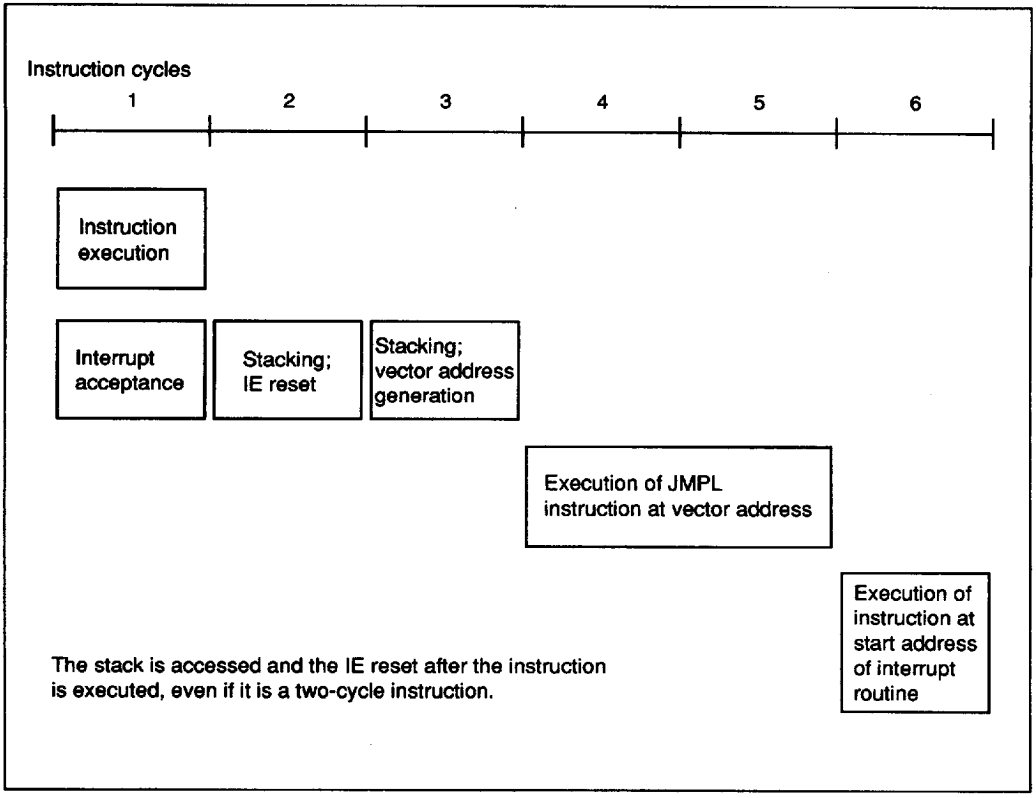


Figure 8 Interrupt Processing Sequence

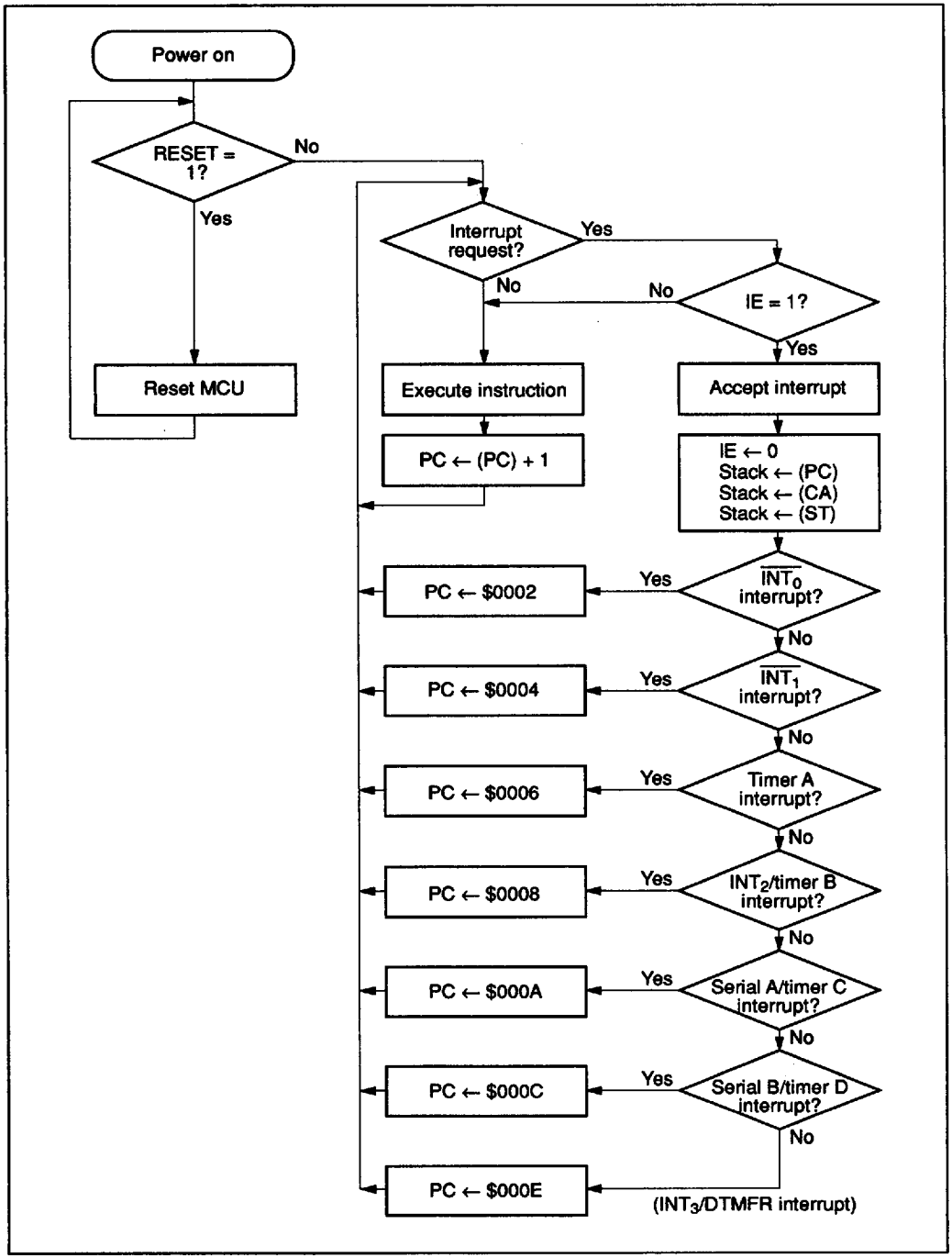


Figure 9 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): This flag controls all interrupts (table 5). IE is reset to 0 by the interrupt processing and set to 1 by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3): Four external interrupt pins are provided for the MCU. The external interrupt request flag is set at the falling edge of the INT_0 and INT_1 inputs. It is set at the rising edge of the INT_2 and INT_3 inputs.

When using $\overline{INT_0}$–INT_3, the corresponding bit of port mode register A (PMRA: $004) selects external interrupt input. If port mode register A is set, the data control register of the corresponding pin is reset automatically, and external interrupt input is enabled. If port mode register A is reset, the external interrupt request flag is not set in spite of external interrupt signal input, and interrupt processing is not performed since the external interrupt input signal is masked.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0; IF2: $002, Bit 0; IF3: 003, Bit 2): External interrupt request flags IF0 and IF1 are set at the falling edge of the INT_0 and INT_1 inputs. IF2 and IF3 are set at the rising edge of the INT_2 and INT_3 inputs (table 6).

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1; IM2: $002, Bit 1; IM3: $003, Bit 3): These masks mask interrupt requests caused by the corresponding external interrupt request flags (table 7).

Table 5 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 6 External Interrupt Request Flags

IF0, IF1, IF2, IF3	Interrupt Request
0	Disabled
1	Enabled

Table 7 External Interrupt Masks

IM0, IM1, IM2, IM3	Interrupt Request
0	Enabled
1	Disabled (Masked)

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode. The low-power dissipation mode functions are shown in table 8, and MCU operation mode relationships are shown in figure 10.

Standby Mode: The MCU enters standby mode if the SBY instruction is executed from active mode. In this mode, the oscillator remains active, and interrupts, the timer/counters, and the serial interface are enabled, but all instruction-control clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents, and maintaining the current I/O pin status. The counter of the DTMF receiver continues to operate and the receiver retains the measurement value.

Standby mode is terminated by a RESET interrupt or an interrupt request. After an interrupt request, the MCU resumes by executing the next instruction following the SBY instruction. Then, if the interrupt enable flag is 1, the interrupt is processed. If the interrupt enable flag is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 11.

Table 8 Low-Power Dissipation Mode Function

		Condition								
Low-Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Registers, Flags	Interrupt Function	RAM	Input/ Output Pins	Timer/ Counters, Serial Interface	DTMFR	Cancel Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*2	Active	Retained	RESET input, interrupt request WDT
Stop mode*1	STOP instruction	Stop	Stop	RESET	Stop	Retained	High impedance	Stop	Stop	RESET input

Notes: 1. The MCU recovers from the stop mode by RESET input. Refer to table 2 for the contents of the flags and registers.
2. If an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is the additional current to the current dissipation in standby mode.

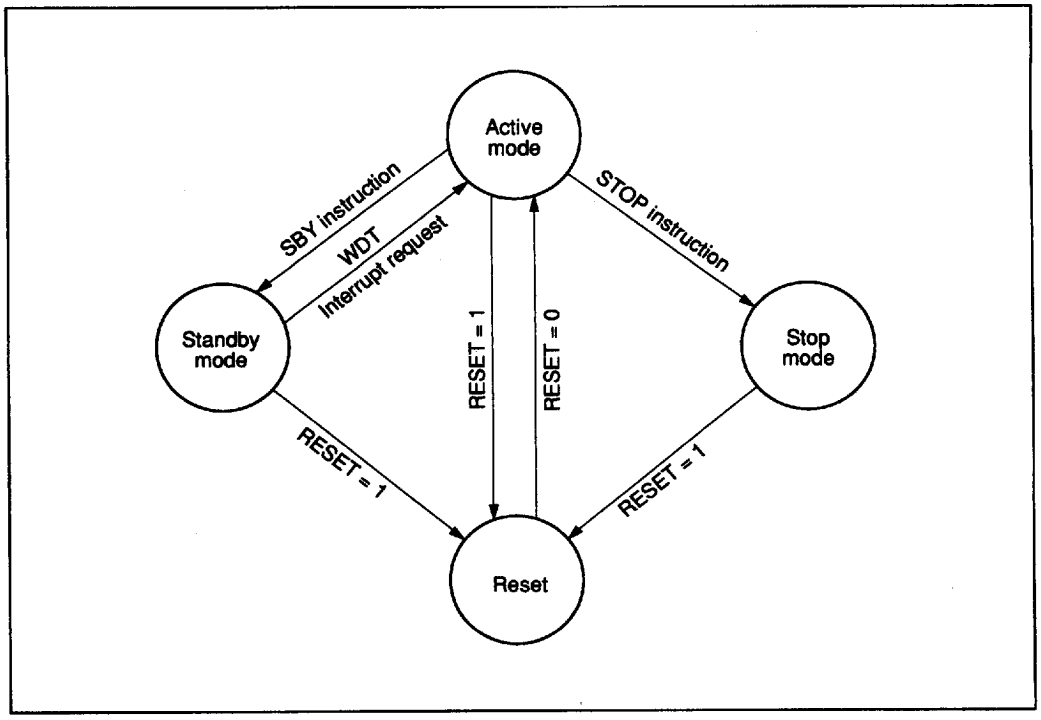


Figure 10 MCU Operation Mode Transition

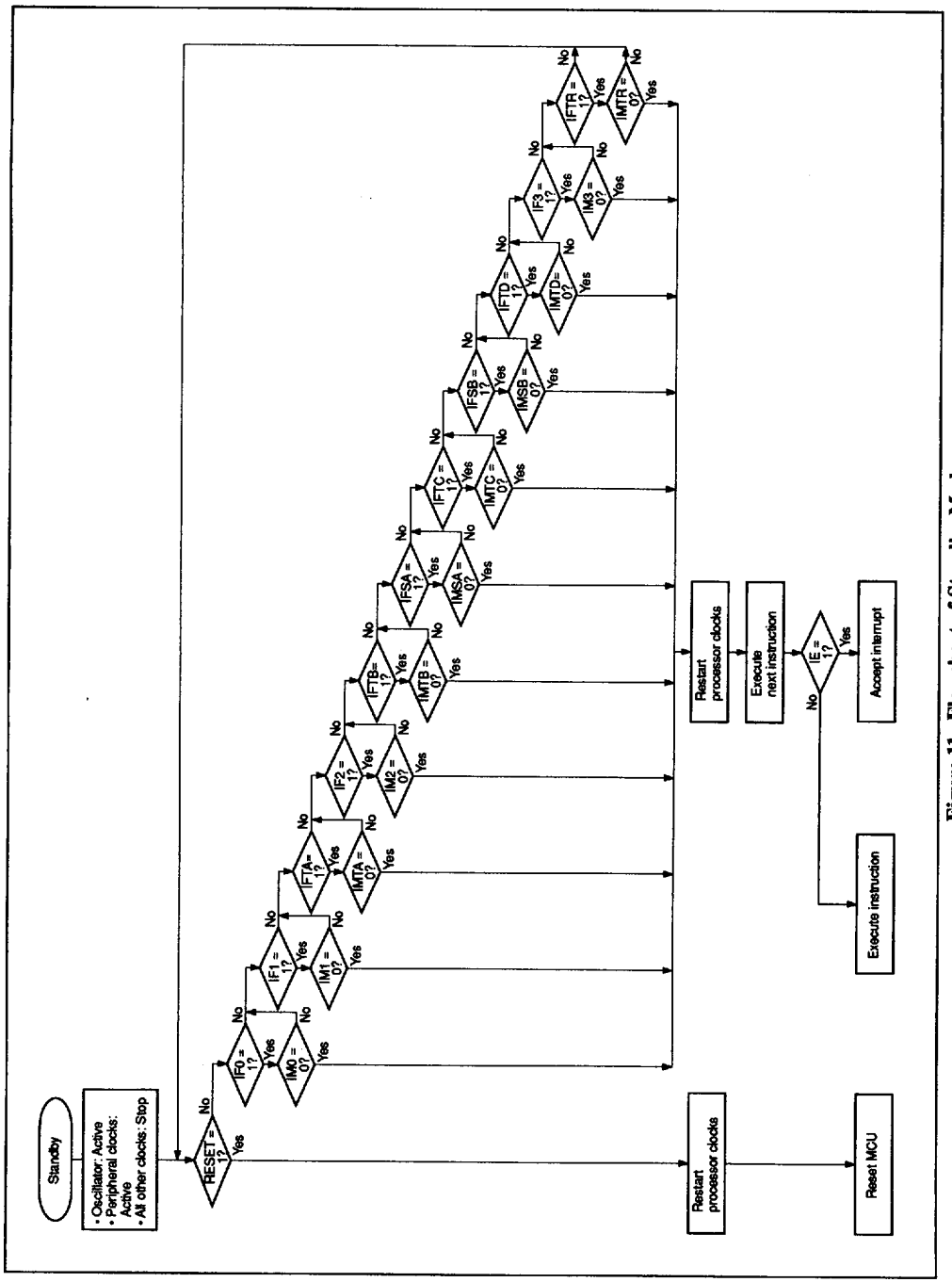


Figure 11 Flowchart of Standby Mode

Stop Mode: The MCU enters the stop mode if the STOP instruction is executed. In this mode, the oscillator stops, causing all MCU functions to also stop.

Stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one t_{RC} to stabilize oscillation. (Refer to the AC Characteristics table.) In stop mode, all RAM contents are retained. After stop mode is cancelled, the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

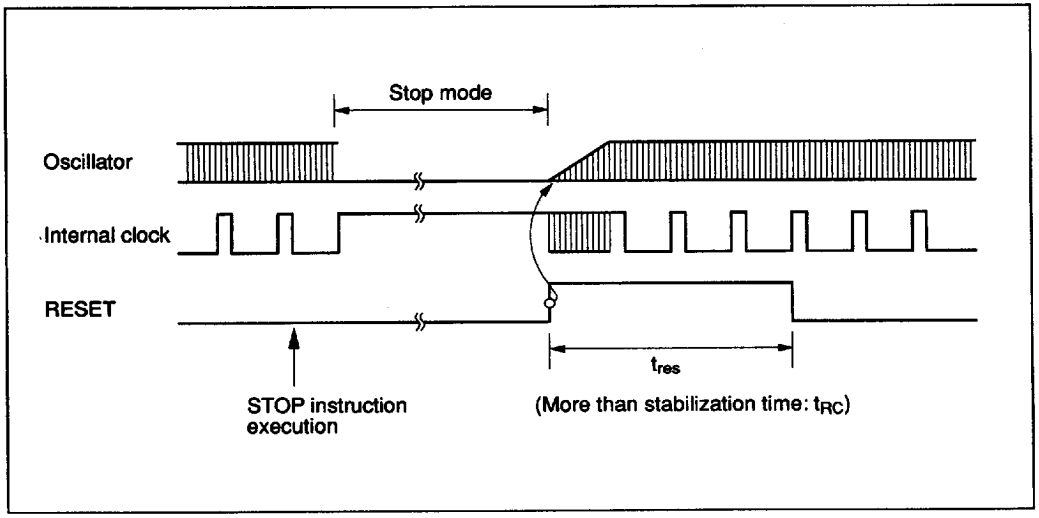


Figure 12 Timing of Stop Mode Cancellation

Low-Power Mode Operation Sequence: The low-power mode operation sequence is shown in figure 13. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

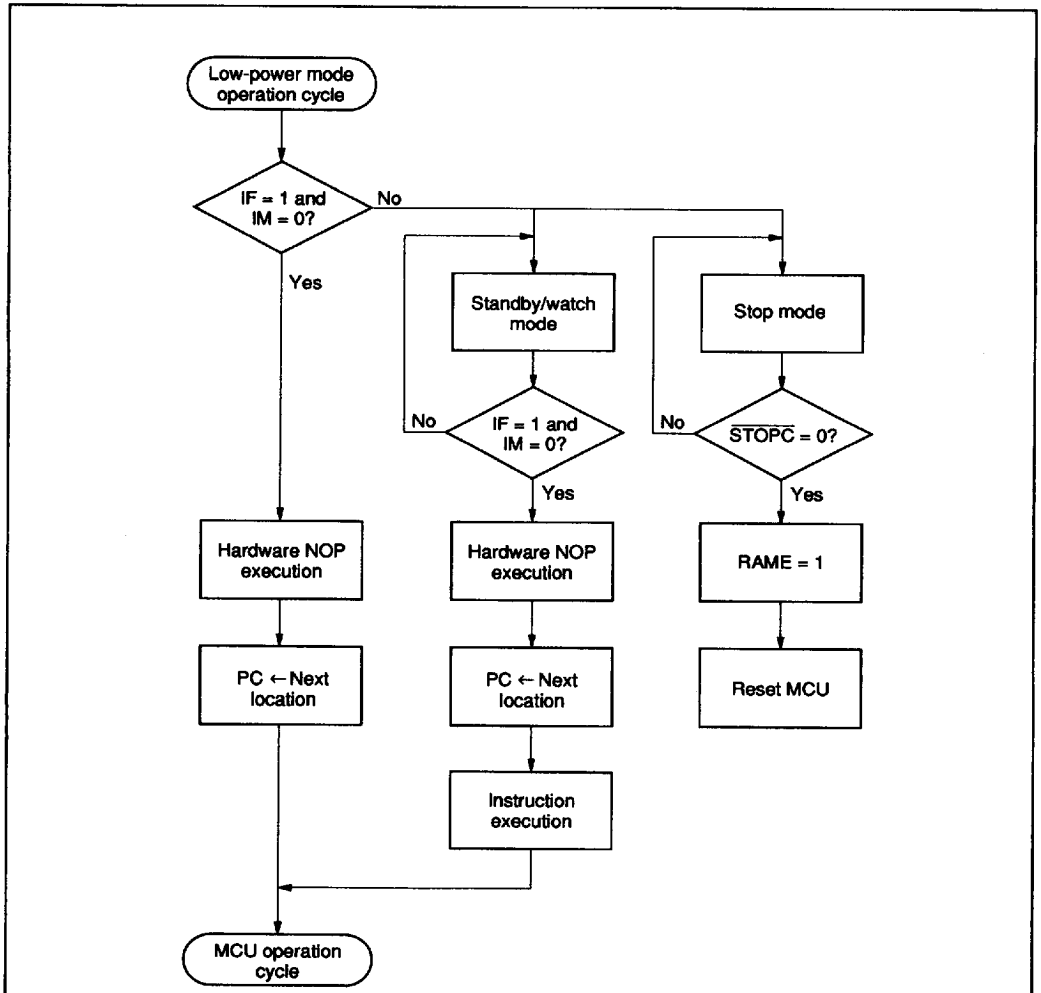


Figure 13 MCU Operating Sequence (Low-Power Mode Operation)

Internal Oscillating Circuit

A block diagram of the internal oscillator circuit is shown in figure 14. A crystal can be used as shown in table 9. An external clock operation is also available.

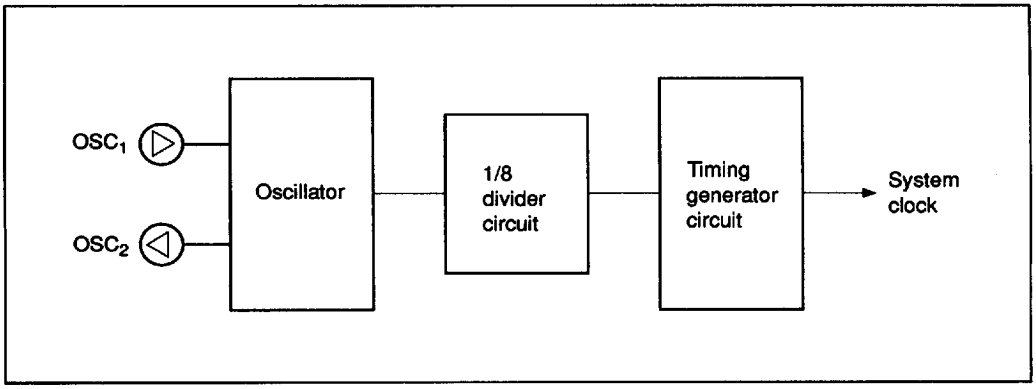


Figure 14 Internal Oscillator Circuit

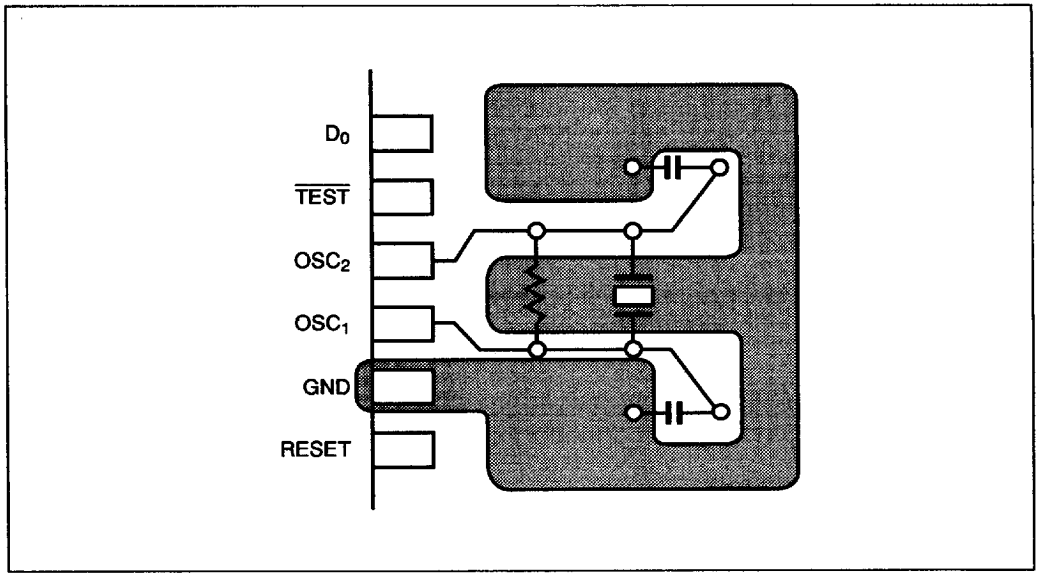
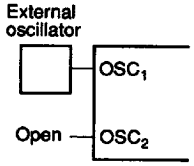
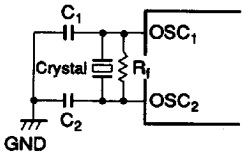
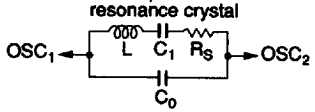


Figure 15 Layout of Crystal Oscillator

Table 9 Oscillator Circuit Examples

Circuit Configuration		Circuit Constants
External clock operation		
Crystal oscillator	 AT-cut parallel resonance crystal 	R_f : 1 MΩ ± 20% C_1 : 10–22 pF ± 20% C_2 : 10–22 pF ± 20% Crystal: Equivalent circuit shown at bottom left C_0 : 7 pF max. R_S : 100 Ω max. f : 4.0 MHz (±0.01%)

Notes: 1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, please consult the crystal manufacturer to determine the actual circuit parameters required.
2. Wiring between the OSC_1/OSC_2 pins and an element must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the crystal in figure 15.

Input/Output

The MCU has 48 input/output pins and 4 dedicated input pins. All the input/output pins except the dedicated input port R8 have data control registers (DCR) that control the data direction. All ports, however, feature either programmable pull-up MOS or pull-down MOS.

Several of the above pins are multiplexed with the input/output pins of peripheral circuits such as for the timer and serial interface. The peripheral circuit has priority on these pins. When set as a peripheral circuit's input or output, pin function and data direction for these pins are automatically selected accordingly.

I/O buffer configuration with pull-up and pull-down MOS is shown in figures 16 and 17. The software directed I/O circuit control is shown in tables 11 and 12. Several I/O types are available due to the combinations of the mode registers (PMRB, DCR, PDR) shown in these tables. I/O pin circuit types are shown in table 10.

PMRB bit 3 controls on and off of all pull-up and pull-down MOSs. DCR and PDR control that of individual pins.

D Port: The D port is an I/O port having 16 I/O pins accessible on a bit basis. A maximum current of 15 mA can flow into each of the pins D_0 to D_9, with a total maximum current of less than 105 mA. In addition, D_{10}–D_{15} can each act as a 10 mA maximum current source.

Pins D_0–D_9 and D_{10}–D_{15} incorporate program controllable pull-up MOS and pull-down MOS, respectively. Data direction is controlled by the D port data control registers (DCRB–DCRE). DCR registers are mapped to RAM.

The D port can be set/reset with the SED/RED and SEDD/REDD instructions and tested with the TD/TDD instruction.

R Port: The R port consists of 32 I/O pins and 4 dedicated input pins, and is accessible on a 4-bit basis. R0–R7 are I/O ports and R8 is an input port. R0–R5 and R6–R8 have program controllable pull-up MOS and pull-down MOS, respectively. Pull-down MOS is controlled by PDR (port data register) on a bit basis. The data direction of the I/O ports is controlled by the R port data control registers (DCR0–DCR7), which are also mapped to RAM. For the R port, the LRA/LRB instruction outputs the contents of the accumulator and B register through the port, and the LAR/LBR input instructions load port data into the accumulator and B register. Several of these pins are multiplexed with the I/O pins of peripheral circuits (table 13).

Port R8 is a 4-pin dedicated input port accessed in 4-bit units. The $R8_2$ pin operates in two modes, digital input mode and analog input mode (variable voltage reset mode). In digital input mode, $R8_2$ functions as a dedicated input pin with input characteristics the same as other I/O pins. In analog input mode, comparison between a reference voltage input through $R8_3/R_{ref}$ and $R8_2/R_{IN}$ input is performed. If the input is higher than the R_{ref} voltage, the system is reset. After a reset pulse is automatically generated synchronously with the system cycle for one cycle, the MCU proceeds to execute from a reset vector. These operation modes are set by port mode register B (PMRB).

In analog mode, an analog voltage comparator is activated. To maintain required characteristics, analog current continues to flow into the analog comparator while it is on. Consequently, current dissipation increases in analog mode. Accordingly, to reduce current dissipation, a program should be prepared which sets $R8_2$ to analog mode only during analog comparison. Note that the analog comparator retains its previous state in standby mode, although in stop mode, it is automatically turned off.

For the R8 port, the LAR/LBR instruction loads port data into the accumulator and B register. This input-only port cannot be written to.

Table 10 Circuit Configurations of I/O Pins

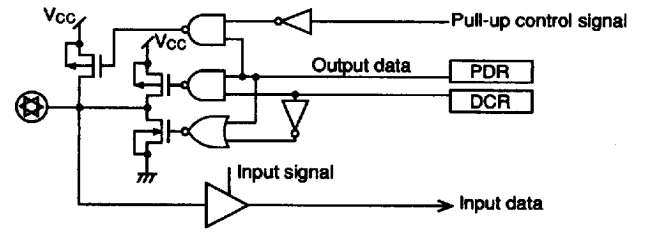
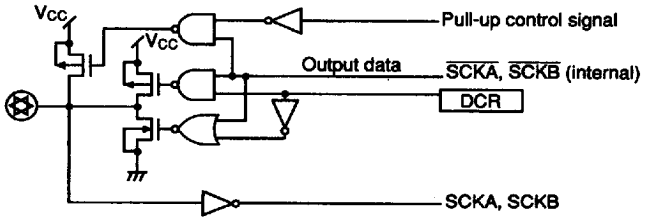
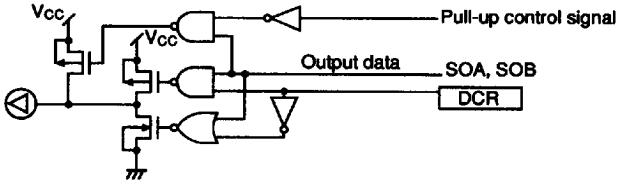
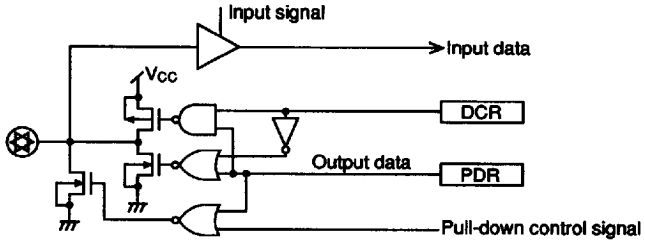
I/O Pin Type	Circuit	Applicable Pins
Common I/O pin (with pull-up MOS transistor)		D_0–D_9 $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$ $R4_0$–$R4_3$ $R5_0$–$R5_3$
		$\overline{SCKA}$ $\overline{SCKB}$
Output pin (with pull-up MOS transistor)		SOA SOB
Common I/O pin (with pull-down MOS transistor)		$R6_0$–$R6_3$ $R7_0$–$R7_3$ D_{10}–D_{15}

Table 10 Circuit Configurations of I/O Pins (cont)

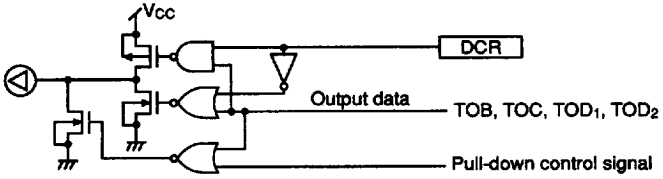
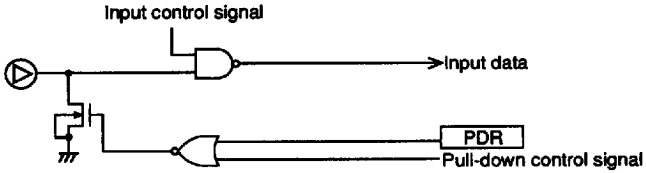
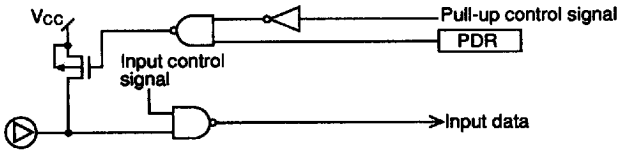
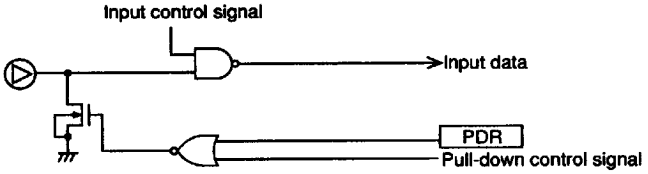
I/O Pin Type	Circuit	Applicable Pins
Output pin (with pull-down MOS transistor)		TOB TOC TOD_1 TOD_2
Input pin (with pull-down MOS transistor)		$R8_0$–$R8_3$
Input pin		$\overline{INT_0}$, $\overline{INT_1}$ SIA, SIB, TIB
		INT_2, INT_3, TIC, TID

Table 11 Programmable I/O Combination (—: Off)

PMRB Bit 3		0				1			
Control bit	DCR	0		1		0		1	
	PDR	0	1	0	1	0	1	0	1
I/O circuit condition	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
	Pull-up MOS	—	On	—	On	—	—	—	—

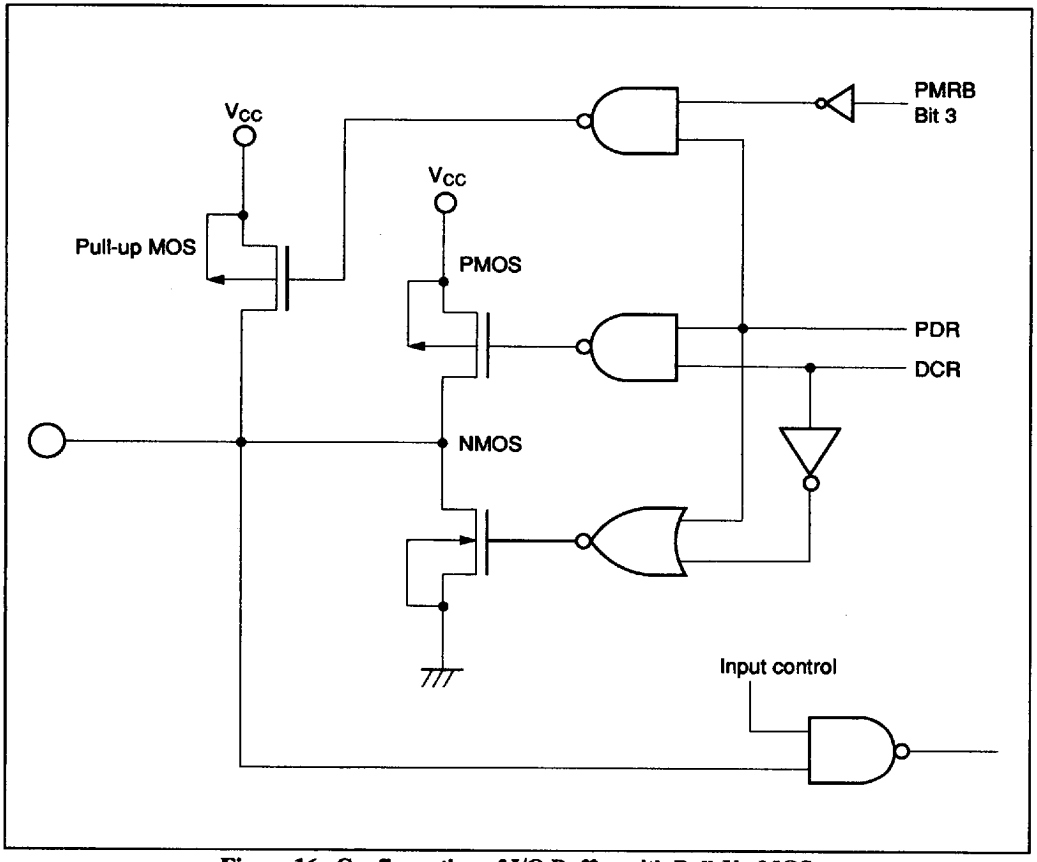


Figure 16 Configuration of I/O Buffer with Pull-Up MOS

Table 12 Programmable I/O Combination (—: Off)

PMRB Bit 3		0				1			
Control bit	DCR	0		1		0		1	
	PDR	0	1	0	1	0	1	0	1
I/O circuit condition	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
	Pull-down MOS	On	—	On	—	—	—	—	—

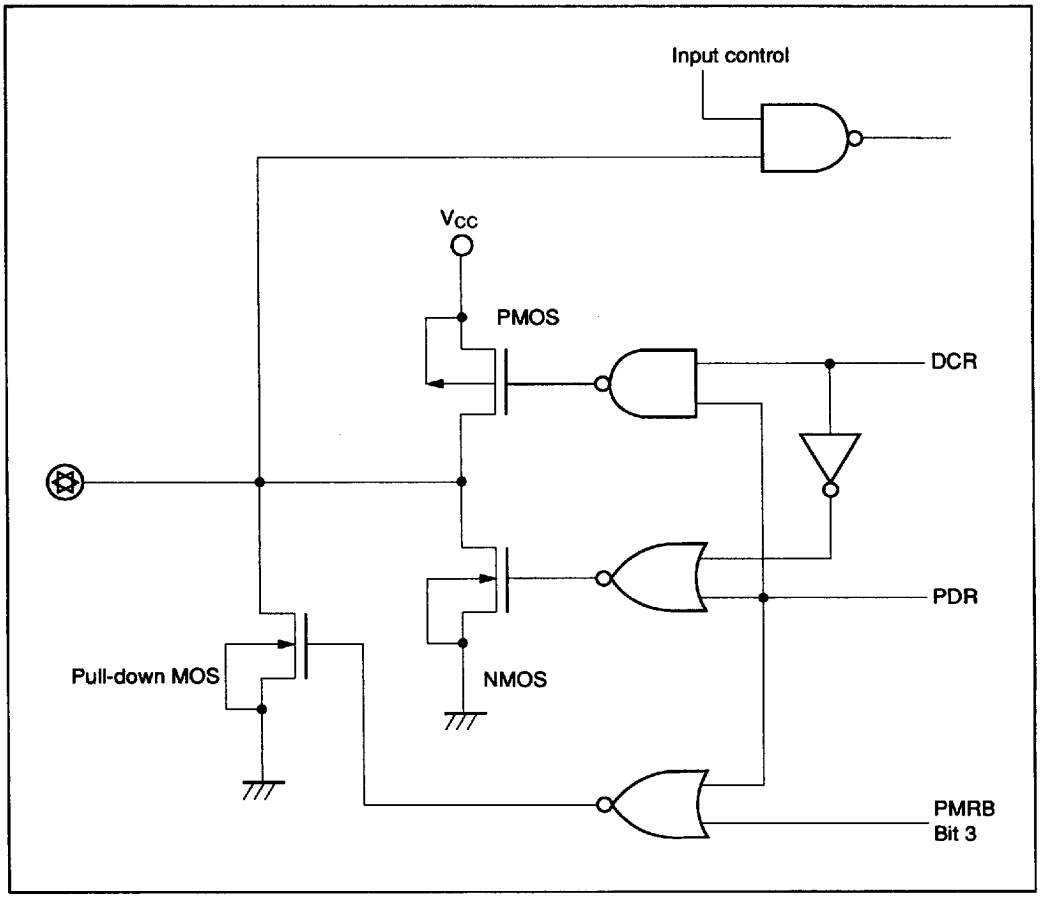


Figure 17 Configuration of I/O Buffer with Pull-Down MOS

Table 13 Multiplexed Pins of R Ports

Pin	Multiplexed Pin	Control Register
$R3_2$	$\overline{INT_0}$	PMRA
$R3_3$	$\overline{INT_1}$ (timer B input)	PMRA
$R4_0$	$\overline{SCKA}$	SMRA
$R4_1$	SIA	SMRA
$R4_2$	SOA	SMRA, PMRB
$R5_0$	$\overline{SCKB}$	SMRB
$R5_1$	SIB	SMRB
$R5_2$	SOB	SMRB, PMRB
$R6_2$	INT_2 (timer C input)	PMRA
$R6_3$	INT_3 (timer D input)	PMRA
$R7_0$	TOB	PMRC
$R7_1$	TOC	PMRC
$R7_2$	TOD_1	PMRC
$R7_3$	TOD_2	PMRC
$R8_2$	R_{IN}	PMRB
$R8_3$	R_{ref}	PMRB

Table 14 Data Control Registers and Control Pins

DCR	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	$R7_3$	$R7_2$	$R7_1$	$R7_0$
DCRB	D_3	D_2	D_1	D_0
DCRC	D_7	D_6	D_5	D_4
DCRD	D_{11}	D_{10}	D_9	D_8
DCRE	D_{15}	D_{14}	D_{13}	D_{12}

Data Control Registers ($030–$037, $03B–$03E): The data control registers (DCR) are 4-bit dedicated write registers which control the data direction of the I/O ports. DCRs are provided for the pins of the D port and R0–R7 ports as 4-bit registers to switch data direction on a bit basis (table 14).

Each port loads data from a pin or pins when functioning as an input port, and loads data from a data register when functioning as an output port. Consequently, even if output potential varies by load when a port functions as an output, output data can be read correctly.

Since DCR is reset to 0 by reset input, all ports are input immediately after reset. To use a port as an output, the corresponding DCR must be set to 1 by a program initialization routine.

Port Mode Registers A, B, C ($004–$006): The port mode registers are 4-bit dedicated write registers. PMRA, PMRB, and PMRC have the functions shown in tables 15, 16, and 17.

PMRA controls the function of $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, $R6_2/INT_2$, and $R6_3/INT_3$. These pins can be used as R-port pins when all bits of PMRA are initialized to 0.

If $R3_2/\overline{INT_0}$ or $R3_3/\overline{INT_1}$ is low when bit 0 or 1 of PMRA is set, the external interrupt request flag IF0 or IF1 is set. If $R6_2/INT_2$ or $R6_3/INT_3$ is high when bit 2 or 3 is set, the external interrupt request flag IF2 or IF3 is set.

PMRB controls $R4_2$, $R5_2$, $R8_2/R_{IN}$, $R8_3/R_{ref}$, and pull-up MOS/pull-down MOS enable/disable of all ports. When bit 2 of PMRB is set to use the reset voltage variable function, and if a voltage higher than R_{ref} is applied to R_{IN}, the MCU will be reset.

A voltage of 0 to V_{CC} – 1.2 V must be applied to R_{ref} to enable the analog comparator function.

When bit 3 of PMRB is reset, pull-up/pull-down MOS attached to all ports are enabled and when it is set, they are disabled. While they are enabled, on/off of each pull-up/pull-down MOS can be controlled by bit settings in the PDR provided for each port. When PMRB bit 3 is initialized to 0 by MCU reset, pull-up/pull-down MOS of all ports are enabled.

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

PMRC controls $R7_0$/TOB, $R7_1$/TOC, $R7_2/TOD_1$, and $R7_3/TOD_2$. These pins function as R-port pins when PMR is initialized to 0 by MCU reset.

TOD_1 and TOD_2 are timer D outputs which are actually identical signals. By controlling bit 2 and 3 of PMRC, timer D output signals can be output to either or both TOD_1 and TOD_2.

I/O Pins Unused on the User System: If unused I/O pins are left floating, the LSI may malfunction due to noise. To prevent this, unused pins should be dealt with as follows:

- Ports with pull-up MOS: Pull up to V_{CC} through an incorporated pull-up MOS or a resistor of approximately 100 kΩ.
- Ports with pull-down MOS: Pull down to GND through an incorporated pull-down MOS or a resistor of approximately 100 kΩ.
- Unused pins other than ports: Pull up to V_{CC} through a resistor of approximately 100 kΩ.

During a programmed reset, the state of unused pins must be retained. Accordingly, the data control register and any other registers related to these unused pins must not be changed.

Table 15 Port Mode Register A Function

PMRA		Bit 3	Bit 2	Bit 1	Bit 0
Pin		$R6_3/INT_3$	$R6_2/INT_2$	$R3_3/\overline{INT_1}$	$R3_2/\overline{INT_0}$
Pin function	0	$R6_3$	$R6_2$	$R3_3$	$R3_2$
	1	INT_3	INT_2	$\overline{INT_1}$	$\overline{INT_0}$

Table 16 Port Mode Register B Function

PMRB		Bit 3	Bit 2	Bit 1	Bit 0
Pin		Pull-up MOS Pull-down MOS disabled	$R8_2/R_{IN}$ $R8_3/R_{ref}$	$R5_2$ (CMOS/NMOS)	$R4_2$ (CMOS/NMOS)
Pin function	0	Resistor MOS enabled	$R8_2$, $R8_3$	CMOS	CMOS
	1	Resistor MOS disabled	R_{IN}, R_{ref}	NMOS	NMOS

Table 17 Port Mode Register C Function

PMRC		Bit 3	Bit 2	Bit 1	Bit 0
Pin		$R7_3/TOD_2$	$R7_2/TOD_1$	$R7_1$/TOC	$R7_0$/TOB
Pin function	0	$R7_3$	$R7_2$	$R7_1$	$R7_0$
	1	TOD_2	TOD_1	TOC	TOB

Timers

The MCU incorporates a prescaler and four timers.

The prescaler is an 11-bit counter to which a system clock signal is input. The prescaler divides this system clock signal into several different clock signals and outputs these signals to different timers. A prescaler output signal is also used as a transmit clock for the serial interface.

Timers B, C, and D are 8-bit versatile timers which can be respectively programmed as a free-running timer, reload timer, and PWM (duty variable pulse output). Timers B to D have I/O pins by which functions such as an event counter or frequency variable clock output can be specified.

Timer A is an 8-bit free-running timer. Timer A is allowed to function as a watchdog timer with hardware reset.

Prescaler: The prescaler is an 11-bit counter whose input is the system clock. After being initialized to $000 by MCU reset, the prescaler counts up by clock cycles. The prescaler outputs are fed to timers A to D and serial interfaces A and B. The prescaler continues counting except during MCU reset and stop mode. It cannot be read from or written to, and its divide ratio can be independently programmed.

Table 18 Timer Function

	Input		Timer Function				Output				
								Function			
Timer	Pin Name	Edge	Free-Running	Reload	PWM	Watchdog	Pin Name	Toggle	0 Output	1 Output	PWM
Timer A	No input pins		Yes	—	—	Yes	No output pins				
Timer B	TIB ($R3_3$)	↓	Yes	Yes	Yes	—	TOB ($R7_0$)	Yes	Yes	Yes	Yes
Timer C	TIC ($R6_2$)	↑	Yes	Yes	Yes	—	TOC ($R7_1$)	Yes	Yes	Yes	Yes
Timer D	TID ($R6_3$)	↑	Yes	Yes	Yes	—	TOD_1 ($R7_2$)	Yes	Yes	Yes	Yes
							TOD_2 ($R7_3$)	Yes	Yes	Yes	Yes

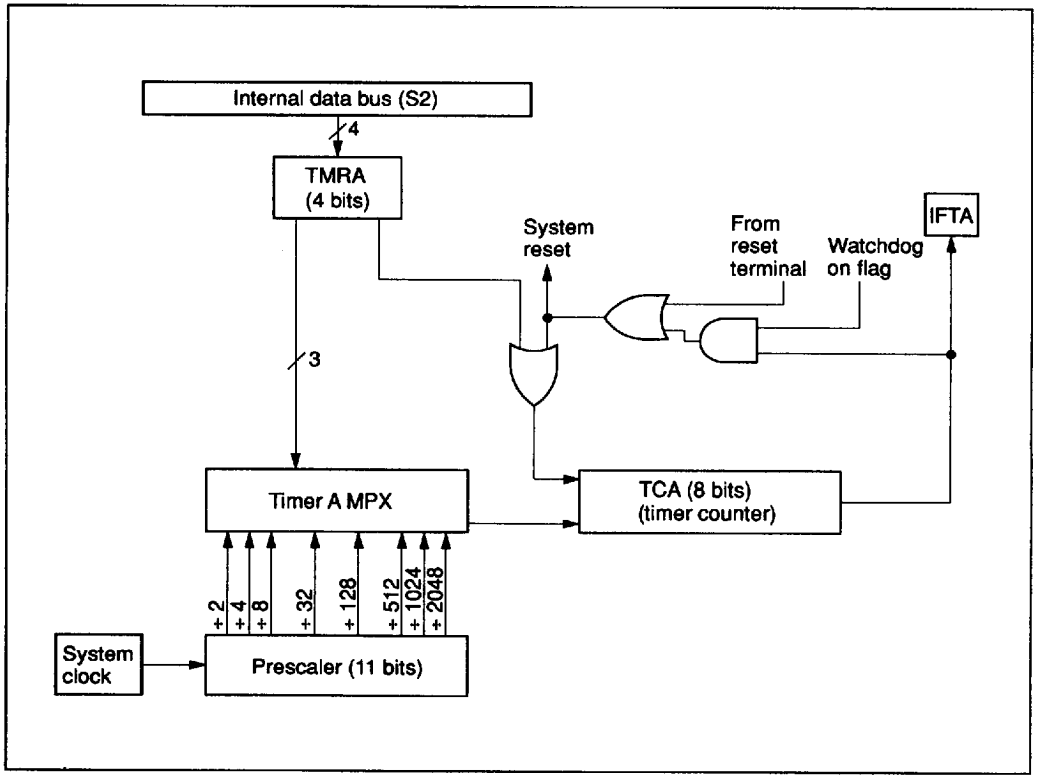


Figure 18 Timer A Block Diagram

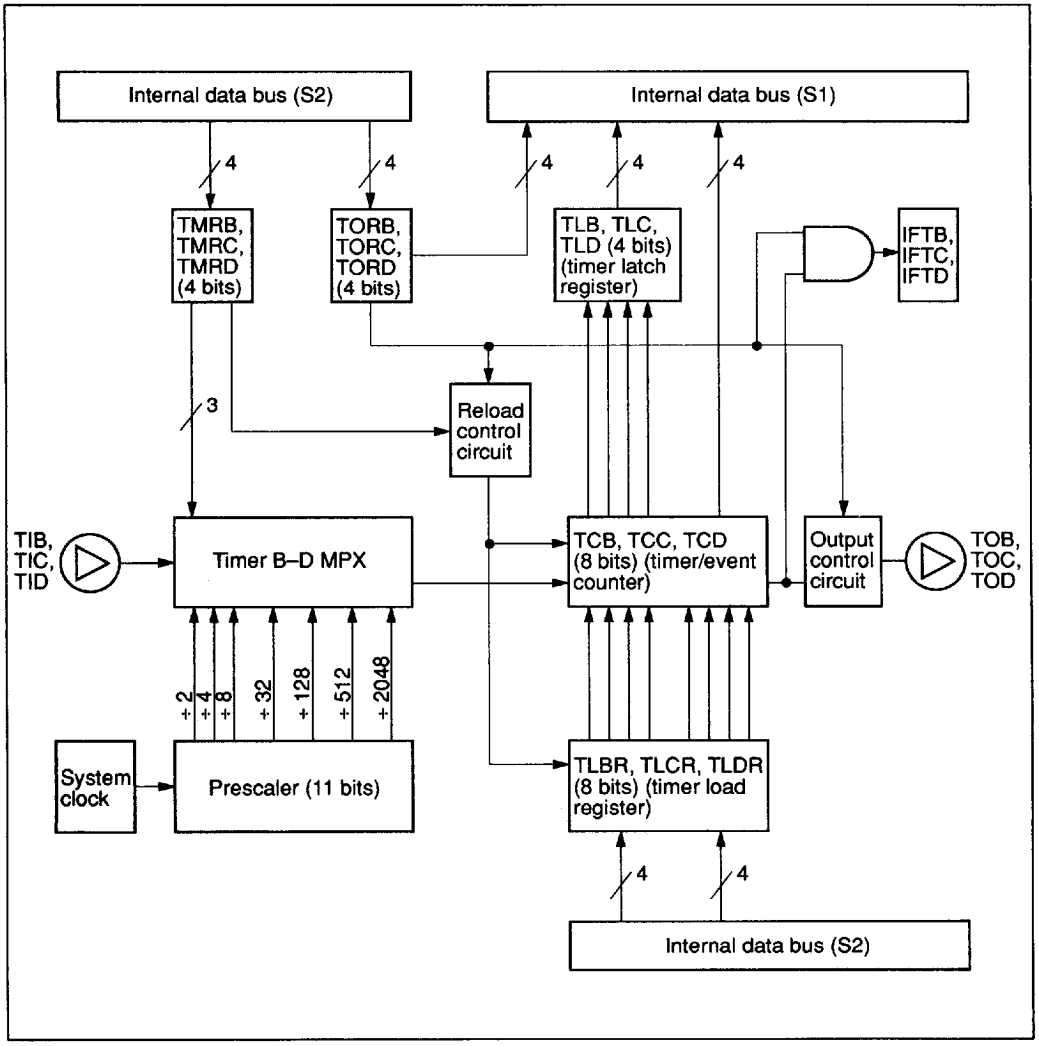


Figure 19 Timers B, C, and D Block Diagram

Operation of Timer A: Functions as a free-running timer and a watchdog timer.

- Free-running timer operation

  Timer A is an 8-bit count-up timer that increments with every input clock.

  When specified as a free-running timer, timer A's input clock is selected among the 8 clocks output by the prescaler using TCS2–TCS0 of timer mode register A.

  When timer A reaches $FF, it generates an overflow, and the timer A interrupt request flag is set. Timer A then restarts counting from $00. The timer interrupt request flag is not reset even when an interrupt is accepted; it must be reset by an instruction in an interrupt processing routine.

  Timer A (free-running timer) is used to generate an interrupt at regular intervals.

- Watchdog timer operation

  Timer A can function as a watchdog timer that increments with every input clock. When timer A overflows, an internal reset signal is generated. If WDTR of timer mode register A is set, timer A is reset and begins counting from $00.

  A watchdog timer can reset and recover the MCU when control has been lost. To enable the function, the program must be prepared so that timer A is reset within a cycle shorter than the prescaler output and the cycle counted by timer A. In such a program, an overflow is not generated during normal MCU operation, because the timer is reset by the program. However, when the MCU is out of control, timer A generates an overflow, and the MCU is reset.

  In watchdog timer mode, timer A is initialized to $00 with a reset signal via the RESET pin. When an overflow is generated, an interrupt does not occur since the MCU has already been reset. The timer can be reset but cannot be written to or read.

Operation of Timers B, C, D: Timers B to D are 8-bit multifunctional timers. Operation modes—free-running, event counter, reload, and PWM—are provided by programming the timer mode registers (TMRB, TMRC, TMRD) and timer output registers (TORB, TORC, TORD).

The timer/counters (TCB, TCC, TCD) count up with every input clock after being initialized to 00 by MCU reset. An input clock can be selected among the clocks divided by the prescaler, and an external clock is available for the event counter. When selecting an external clock input, the interrupt mask bit of each external interrupt must be set to inhibit external interrupts since external clock input pins are multiplexed with external interrupt pins.

Table 19 Timer A Function

Item	Free-Running Timer	Watchdog Timer
Prescaler divide ratio	Variable (8: ÷2 to ÷2048)	
Timer reset	Possible (write 1 to WDTR)	
Interrupt function	Provided	None
Internal system reset function	None	Provided

The timer interrupt request flags (IFTB, IFTC, IFTD) are set if an input clock is supplied after the timer/counters reach $FF. When auto-reload function is not specified, timers B to D function as free-running timer/event counters, and restart to count up from $00. When auto-reload function is specified, timers B to D function as reload timers. In the reload mode, an overflow signal causes the timer load register value to be loaded into the timer/counter, and the timer counts up from that value.

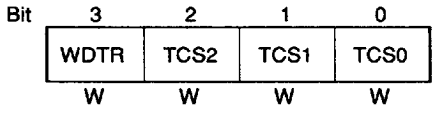
Timers B to D also function as timer input/output circuits. The timer output circuit varies output level when a clock pulse is input after the timer reades $FF. By combining this circuit and the reload timer, several different cycle clock signals can be output.

Timers B to D are set in PWM mode when the timer output register is programmed. The cycle of the pulse is 256 clocks, and the length of the high portion is the same value as that of the timer load register. A voltage level proportional to the value set in the timer load register can be obtained by combining PWM and a lowpass filter.

Timer Mode Register A (TMRA: $007): A 4-bit write-only register. The function of timer mode register A is shown in figure 20 and table 20.

Table 20 Input Clock Source Selection for Timer A

Timer Mode Register Bit			
TCS2	**TCS1**	**TCS0**	**Input Clock Source**
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2



Bit 3 (WDTR: Watchdog Timer Reset): Resets timer A when 1 is written to WDTR, after which timer A begins counting from $00.

Bits 0–2 (TCS0–TCS2: Timer Clock Select): Selects timer A input clock source. These bits are initialized to 000 after reset.

Figure 20 Timer Mode Register A

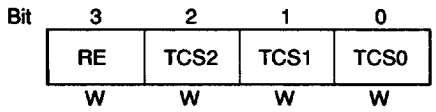
Timer Mode Registers B, C, D (TMRB: $008, TMRC: $00C, TMRD: $010): 4-bit write-only registers which control the auto-reload function, input source, and prescaler divide ratio of timers B, C, and D as shown in figure 21 and table 21. These registers are initialized to $0 by MCU reset.

The timer mode register value can be changed from the third instruction after executing the timer mode register write instruction. Timer initialization by the timer load register write instruction must be executed after the varied mode becomes valid.

Table 21 Input Clock Source Selection for Timers B, C, and D

Timer Mode Register Bit			
TCS2	**TCS1**	**TCS0**	**Input Clock Source**
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	(external event input)*

Note:* When an external event input is selected, pins $R3_3$, $R6_2$, and $R6_3$ should be set to INT input by PMRA.



Bit 3 (RE: Reload Enable): Controls auto-reload function of timers B–D. When RE is 1, timers B to D function as a reload timer. When it is 0, they function as a free-running timer. RE is initialized after reset.

Bits 0–2 (TCS0–TCS2: Timer Clock Select): Selects input clock source of timers B–D. They are initialized to 000 after reset.

Figure 21 Timer Mode Registers B, C, and D

Timer Output Registers B, C, D (TORB: $009, TORC: $00D, TORD: $011): 4-bit read/write registers which control the output mode, PWM output mode, and external interrupt multiplexed with timer input pins of timers B to D as shown in figure 22 and table 22. By combining these modes and various modes of timers B to D, several different frequencies and duty clock signals can be obtained. When setting PWM output, the timer output pin functions as a PWM output regardless of timer output mode. The timer output register value becomes valid from the third instruction after the timer output register write instruction.

Timer Counters BL, BU, CL, CU, DL, DU (TCBL: $00A, TCBU: $00B, TCCL: $00E, TCCU: $00F, TCDL: $012, TCDU: $013), Timer Load Registers BL, BU, CL, CU, DL, DU (TLBL: $00A, TLBU: $00B, TLCL: $00E, TLCU: $00F, TLDL: $012, TLDU: $013): Timers B to D are 8-bit timers comprised of read-only timer counters and write-only timer load registers at the same address. Each register is divided into lower and upper digits which are located at sequential addresses.

The high data digit is read from the timer/counter first. At the same time, the lower digit is latched into the 4-bit timer latch register. When a lower digit is read, it is read from the latched register. Therefore, it is possible to read an upper and lower digit at the same time.

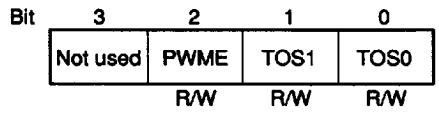
After data is written in the timer load register, it is loaded into the timer/counter and the timer begins counting from the loaded value. The lower digit must be written in the timer load register first. The timer mode register value is loaded into the timer/counter at the same time the upper digit is written to. The timer/counter and timer load register are initialized to $00 during reset.

Timers B, C, D Operation Modes: Various modes can be provided by timers B to D by programming each timer mode register and timer output register. Programmable operation modes are listed in table 23. Timer output waveform examples are shown in figure 23.

Table 22 Output Mode Selection of Timers B, C, and D

Timer Output Register Bit			
TOS1	**TOS0**	**Output Mode**	**Function**
0	0	—	Output disabled
0	1	Toggle output	Output is reversed synchronously with timer overflow
1	0	0 output	Low is output synchronously with timer overflow
1	1	1 output	High is output synchronously with timer overflow

Note: For timer output, pins $R7_0$, $R7_1$, $R7_2$, and $R7_3$ must be set to timer output mode by PMRC.



Bit 2 (PWME: Pulse Width Modulation Enable): Controls the PWM function of timers B, C, and D. When PWME is 1, timers B, C, and D are set to PWM mode. PWME is initialized to 0 after reset.

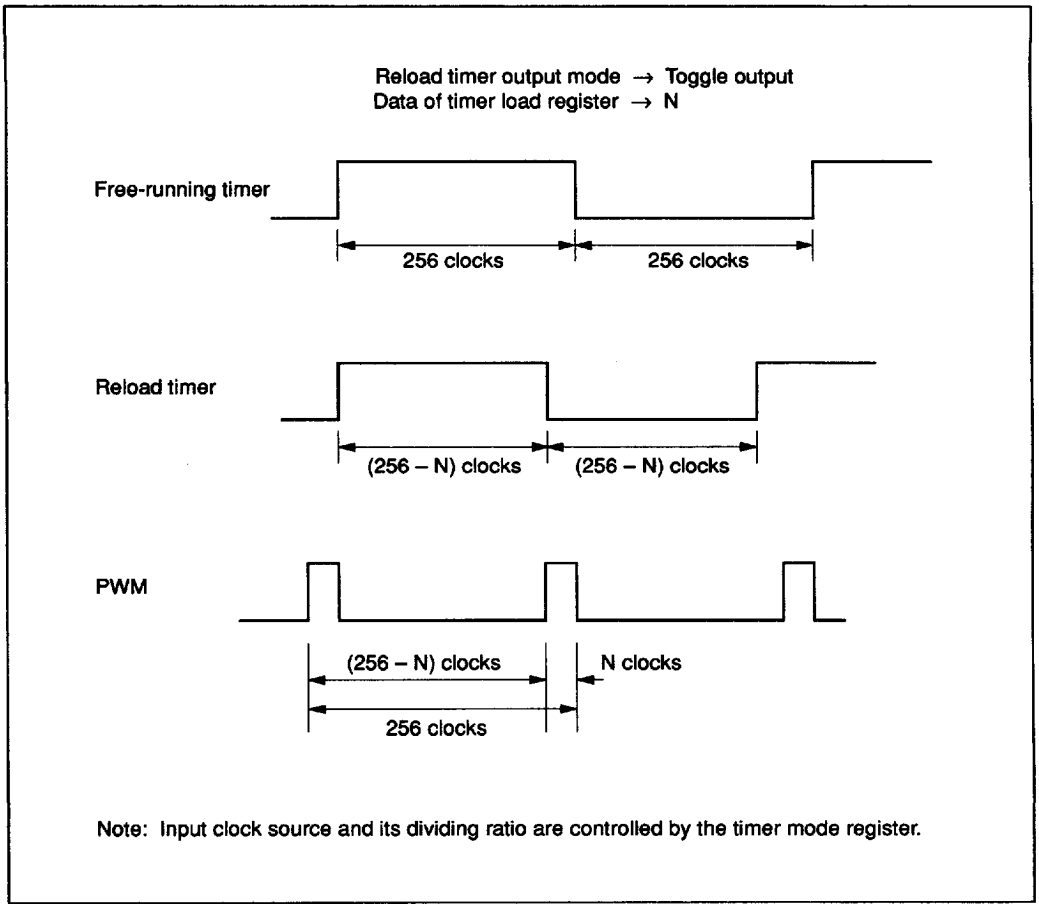
Bits 0, 1 (TOS0, TOS1: Timer Output Mode Select): Selects output pin mode of timers B, C, and D. These bits are initialized to 00 after reset.

Figure 22 Timer Output Register

Table 23 Operation Modes of Timers B, C, and D

PMRA	PMRC	TMRB, TMRC, TMRD				TORB, TORC, TORD					
Bits 1–3	Bits 0–4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	Timer Input Pin	Timer Output Pin	Timer B–D Function
1	0	0	1	1	1	0	0	0	TIB, TIC, TID	$R7_0$, $R7_1$, $R7_2$, $R7_3$	Event counter
1	1	0	1	1	1	0	*2	*2	TIB, TIC, TID	TOB, TOC, TOD_1, TOD_2	
0	0	0	*3	*3	*3	0	0	0	$R3_3$, $R6_2$, $R6_3$	$R7_0$, $R7_1$, $R7_2$, $R7_3$	Free-running timer
0	1	0	*3	*3	*3	0	*2	*2	$R3_3$, $R6_2$, $R6_3$	TOB, TOC, TOD_1, TOD_2	
1	0	0	*3	*3	*3	0	0	0	$\overline{INT_1}$, INT_2, INT_3	$R7_0$, $R7_1$, $R7_2$, $R7_3$	
1	1	0	*3	*3	*3	0	*2	*2	$\overline{INT_1}$, INT_2, INT_3	TOB, TOC, TOD_1, TOD_2	
0	0	1	*3	*3	*3	0	0	0	$R3_3$, $R6_2$, $R6_3$	$R7_0$, $R7_1$, $R7_2$, $R7_3$	Reload timer
0	1	1	*3	*3	*3	0	*2	*2	$R3_3$, $R6_2$, $R6_3$	TOB, TOC, TOD_1, TOD_2	
1	0	1	*3	*3	*3	0	0	0	$\overline{INT_1}$, INT_2, INT_3	$R7_0$, $R7_1$, $R7_2$, $R7_3$	
1	1	1	*3	*3	*3	0	*2	*2	$\overline{INT_1}$, INT_2, INT_3	TOB, TOC, TOD_1, TOD_2	
1	0	1	1	1	1	0	0	0	TIB, TIC, TID	$R7_0$, $R7_1$, $R7_2$, $R7_3$	Event counter (with reload function)
1	1	1	1	1	1	0	*2	*2	TIB, TIC, TID	TOB, TOC, TOD_1, TOD_2	
0	1	*1	*3	*3	*3	1	*1	*1	$R3_3$, $R6_2$, $R6_3$	TOB, TOC, TOD_1, TOD_2	PWM *4
1	1	*1	*3	*3	*3	1	*1	*1	$\overline{INT_1}$, INT_2, INT_3	TOB, TOC, TOD_1, TOD_2	
1	1	*1	1	1	1	1	*1	*1	TIB, TIC, TID	TOB, TOC, TOD_1, TOD_2	*4 PWM (external clock)

Notes: 1. Neither 0 nor 1 affect operation.
2. Either or both of TOR bits 0 and 1 are 1.
3. One, two, or all of TMR bits 0–2 are 0.
4. If the timer load register value is $00 when PWM output is selected, the timer functions as a free-running timer.



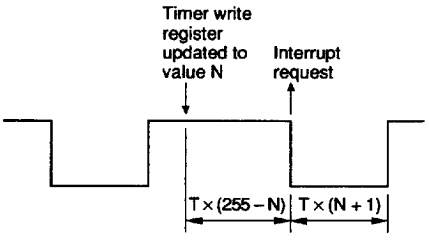
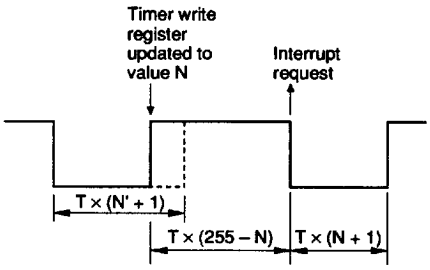
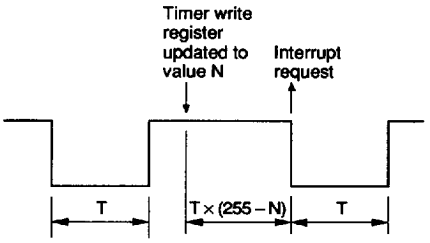
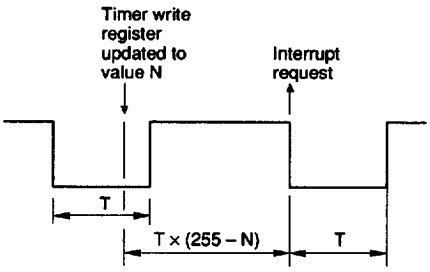
Note: Input clock source and its dividing ratio are controlled by the timer mode register.

Figure 23 Timer Output Waveform Examples

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 24. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 24 PWM Output Following Update of Timer Write Register

Mode	PWM Output: Timer Write Register is Updated during High PWM Output	PWM Output: Timer Write Register is Updated during Low PWM Output
Free running		
Reload		

Serial Interface

The MCU incorporates two clock-synchronous 8-bit serial interfaces that are composed of serial data registers, serial mode registers, serial clock registers, octal counters, and multiplexers as shown in figure 24.

Two serial interfaces have identical functions, however, the transmit clock and transmit speed can be set independently. Each serial interface also functions as a clock output.

Table 25 Serial Interface Function

Item			Function		
Transmit format			Clock synchronous serial interface (LSB transmitted first)		
Number of transmit bits			8 bits		
Transmit rate (baud rate at t_{cyc} = 2 µs: BPS)			$1/t_{cyc}$ (500000) to $1/4096 \times t_{cyc}$ (122)		
Operation mode			Transmit mode: transmit mode receive mode transmit/receive mode Special mode: clock output mode		
Transmit clock			Internal clock (transmit clock output) External clock (transmit clock input)		
Pin	Serial interface A	Clock	$\overline{SCKA}$	$R4_0$	I/O
		Data input	SIA	$R4_1$	I
		Data output	SOA	$R4_2$	O
	Serial interface B	Clock	$\overline{SCKB}$	$R5_0$	I/O
		Data input	SIB	$R5_1$	I
		Data output	SOB	$R5_2$	O

Table 26 Related Serial Interface Registers

Serial Interface	Register Name	Abbr.	Address	Read/Write
Serial interface A	Serial mode register A	SMRA	$014	R/W
	Serial clock register A	SCRA	$015	W
	Serial data register A (L)	SRAL	$016	R/W
	Serial data register A (U)	SRAU	$017	R/W
Serial interface B	Serial mode register B	SMRB	$018	R/W
	Serial clock register B	SCRB	$019	W
	Serial data register B (L)	SRBL	$01A	R/W
	Serial data register B (U)	SRBU	$01B	R/W

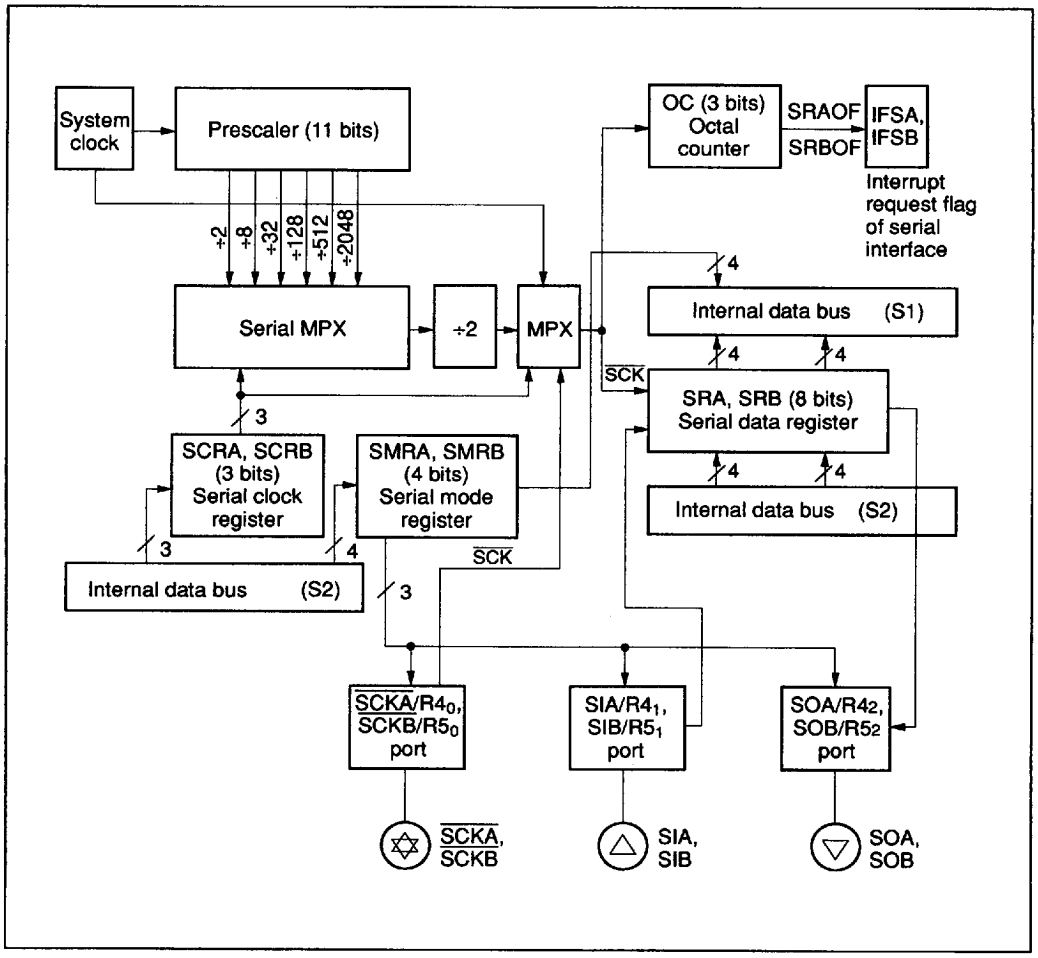


Figure 24 Serial Interface Block Diagram

Serial Mode Registers A, B (SMRA: $014, SMRB: $018): 4-bit read/write registers which control serial interface operation and the $\overline{SCKA}$, $\overline{SCKB}$, SIA, SIB, SOA, and SOB pins as explained in figure 25. When the serial mode register is written to, the transmit clock stops to be supplied to the serial data register and octal counter, and the octal counter is initialized to $0. Therefore, if the serial mode register is written to during serial interface operation, data transmission stops and the serial interrupt request flag is set.

A serial mode register change becomes valid from the second instruction after the serial mode register write instruction, so an STS instruction must be executed two cycles after the serial mode register write instruction. The serial mode register is initialized to $0 by MCU rest.

Bit	3	2	1	0
	STSE	SCKE	SIE	SOE
	R/W	R/W	R/W	R/W

Bit 3 (STSE: STS instruction Enable): Controls the STS instruction which starts/stops serial transmission. If this instruction is executed when STSE is 1, serial transmission begins. When STSE is 0, serial transmission is inhibited regardless of the STS value. STSE is automatically reset after STS instruction execution. During reset, STSE is initialized to 0.

Bit 2 (SCKE: SCK Enable): Controls the transfer clock input/output pins for serial transmission. When SCKE is 1, these pins are automatically set to input or output according to the type of transmit clock being used (internal/external). When SCKE is 0, these pins function as port pins. SCKE is initialized to 0 during reset.

Bit 1 (SIE: SI Enable): Controls the data input pins for the serial interface. When SIE is 1, the pins are automatically set to input. When SIE is 0, they function as port pins. SIE is initialized to 0 during reset.

Bit 0 (SOE: SO Enable): Controls the data output pins for the serial interface. When SOE is 1, the pins are automatically set to output. When SOE is 0, they function as port pins. SOE is initialized to 0 during reset.

Figure 25 Serial Mode Registers A and B

Serial Clock Registers A, B (SCRA: $015, SCRB: $019): 3-bit dedicated write registers. These registers can be written to on a bit basis with the bit set/bit reset instruction as well as on a digit basis.

Writing in the serial clock register becomes valid two cycles after instruction execution. Writing in the register initializes the octal counter to 000. If the serial clock register is written to during transmission, the octal counter becomes 000 to stop transmission, and the serial interrupt request flag is set at the same time.

Serial Data Registers AL, AU, BL, BU (SRAL: $016, SRAU: $017, SRBL: $01A, SRBU: $01B): 8-bit registers which shift to the right (towards the LSB) with every transmit clock input. During serial transmission, the LSB is output through a data pin and 0 is written to the MSB. In transmit/receive mode, the LSB output and MSB input are performed at the same time.

The serial data register is separated into lower and upper digits which are located at sequential addresses. Therefore, data read/write must be performed twice. Since data shift and data read/write are performed asynchronously, data read/write cannot be performed during serial data transmission. If read/write is executed during serial transmission, the accuracy of the data cannot be guaranteed.

The serial data register cannot be reset. The value of the serial data register is undefined after reset.

Table 27 Input Clock Sources

Bit			SCK		Prescaler	System Clock	Baud Rate at
SCS2	SCS1	SCS0	I/O	Clock Source	Divide Ratio	Divide Ratio	t_{cyc} = 2 µs (BPS)
0	0	0	O	Prescaler	÷ 2048	÷ 4096	122
0	0	1	O	Prescaler	÷ 512	÷ 1024	488
0	1	0	O	Prescaler	÷ 128	÷ 256	1953
0	1	1	O	Prescaler	÷ 32	÷ 64	7812
1	0	0	O	Prescaler	÷ 8	÷ 16	31250
1	0	1	O	Prescaler	÷ 2	÷ 4	125000
1	1	0	O	System clock	—	÷ 1	500000
1	1	1	I	External clock	—	—	—

Note: If an internal clock is selected (transmit clock output: SCK I/O = O) when the SCKE bit of the serial clock mode register is 1, the clock input/output pin is automatically set to output. When an external clock (transmit clock input: SCK I/O = I) is selected, the pin is automatically set to input.

Bit	3	2	1	0
	—	SCS2	SCS1	SCS0
		W	W	W

Bits 2–0 (SCS2–SCS0: Serial Clock Select): Select the input clock source for the serial interface. These bits are initialized to 0 during reset.

Figure 26 Serial Clock Register

Serial Interface Operation: The serial interface is used to transmit data between an HD404678 Series device and other devices. As shown in figure 27, the clock pin, data input pin, and data output pin of one device are connected to the respective clock pin, data output pin, and data input pin of another device. If omni-directional transfer is required, a data input pin and a data output pin are connected. For example, during serial transmission from an HD404678 Series device, the serial output pin of the HD404678 Series device and the data input pin of the other device are connected. (The HD404678 Series device can also operate in receive mode.) Data transfer timing is shown in figure 28.

Proper transfer timing and AC timing must be implemented for serial transmissions to different devices.

Note that the HD404678 Series device transmits the LSB first. However, some other devices transmit the MSB first. Accordingly, the order of data conversion should be checked.

STS Instruction and STSE Bit: The STS instruction (Start Serial) initiates two serial interface operations. Each serial interface has an STS instruction enable bit (STSE). When this bit is set, the STS instruction is executed. When both STSE bits are set, two serial interfaces operate with one STS instruction. Conversely, when two STSE bits are reset, the serial interface does not operate even if the STS instruction is executed. To prevent conflict between two serial interfaces, after the STS instruction is executed, the STSE bit is automatically reset at the following cycle.

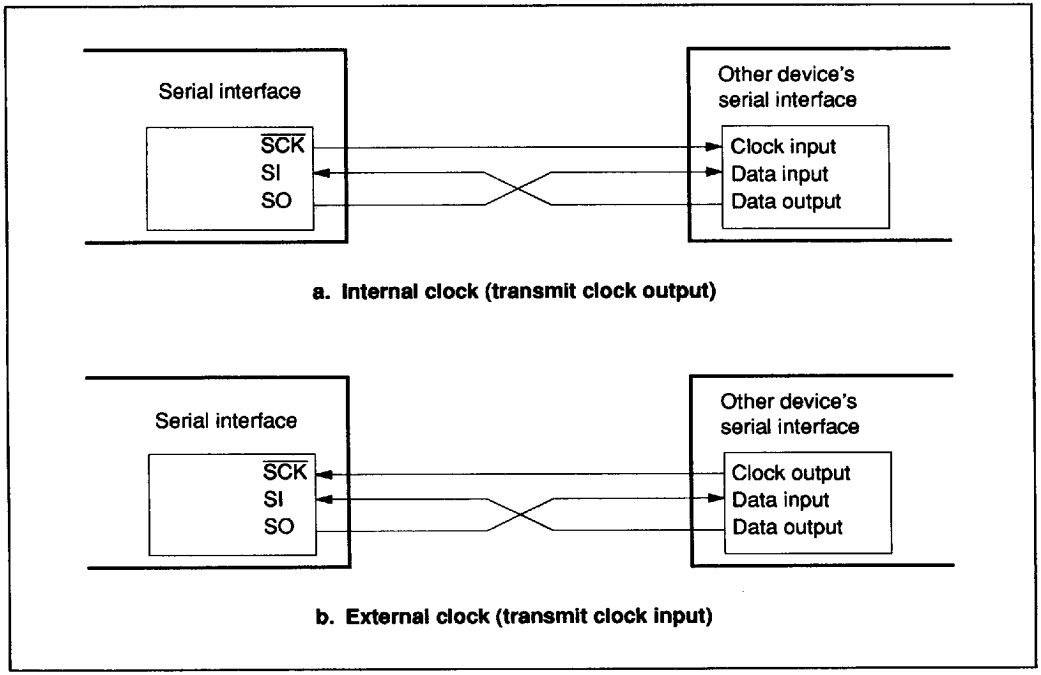


Figure 27 Serial Interface Connection

Serial Interface Operation Mode: The serial interface operation mode is set with the serial mode register, and the serial transmit clock is set with the serial clock register as listed in table 28. The serial interface has four operation modes: three transmit modes and a special mode. When the serial interface is set in any one of these modes, the pins multiplexed with ports function as serial input/output pins.

- Transmit mode: Data is transmitted synchronously with a transmit clock. At the same time, 0 is received by the MSB.
- Receive mode: Data is received via an input synchronously with the transmit clock.
- Transmit/receive mode: Data is transmitted and received simultaneously and synchronously with a transmit clock.
- Clock output mode: A transmit clock is output when transmit clock output mode (internal clock) is selected. The serial data register does not shift.

Table 28 Serial Interface Operation Modes

Serial Mode Register Bit				
SCKE	SIE	SOE	Serial Interface Operation Modes	
1	0	1	Transmit mode	Transmit mode
1	1	0	Receive mode	Transmit mode
1	1	1	Transmit/receive mode	Transmit mode
1	0	0	Clock output mode	Special mode

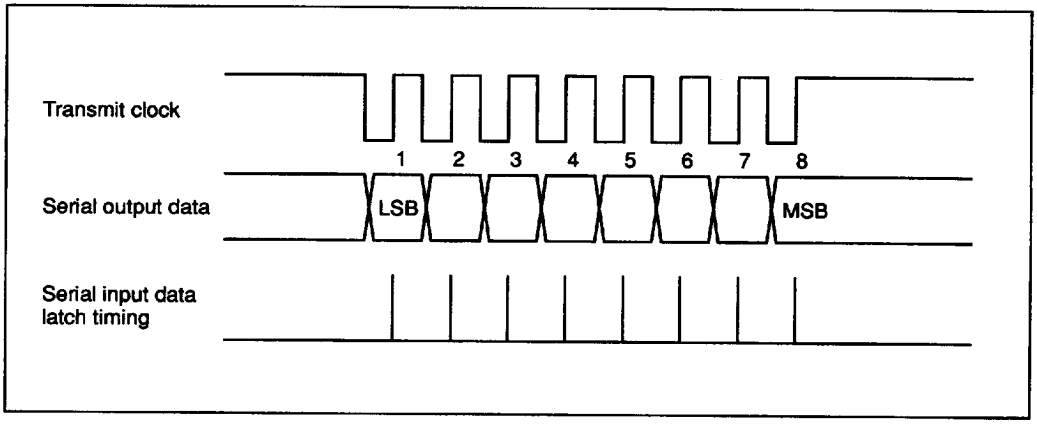


Figure 28 Serial Interface I/O Timing

Data Transmit Procedure: Four operating states are provided for the serial interface. Their interaction is shown in figure 29.

The serial interface is initialized in the transfer inhibit state in which the STS instruction and transmit clock are ignored.

The serial interface is in a STS wait state if the STSE bit of the serial mode register of the desired serial interface is set. When the STS instruction is executed while the STSE bits of serial interfaces 1 and 2 are both set, two serial interfaces can be controlled by one STS instruction.

During transmit state, an input to the transmit clock increments the octal counter, shifts the serial data register, and starts serial transmission. If a clock output mode is selected by the serial mode register, the transmit clock continues to output without data transmission.

During transmission, 8 clock inputs set the octal counter to 000 and also set the serial interrupt request flag. In this state, if the internal clock is selected, serial transmission is inhibited, and if an external clock is selected, the system enters the transmit clock wait state. If the serial mode register and the serial clock register are written to during transmission, the octal counter is set to 000, which stops transmission, and, at the same time, the interrupt request flag is set.

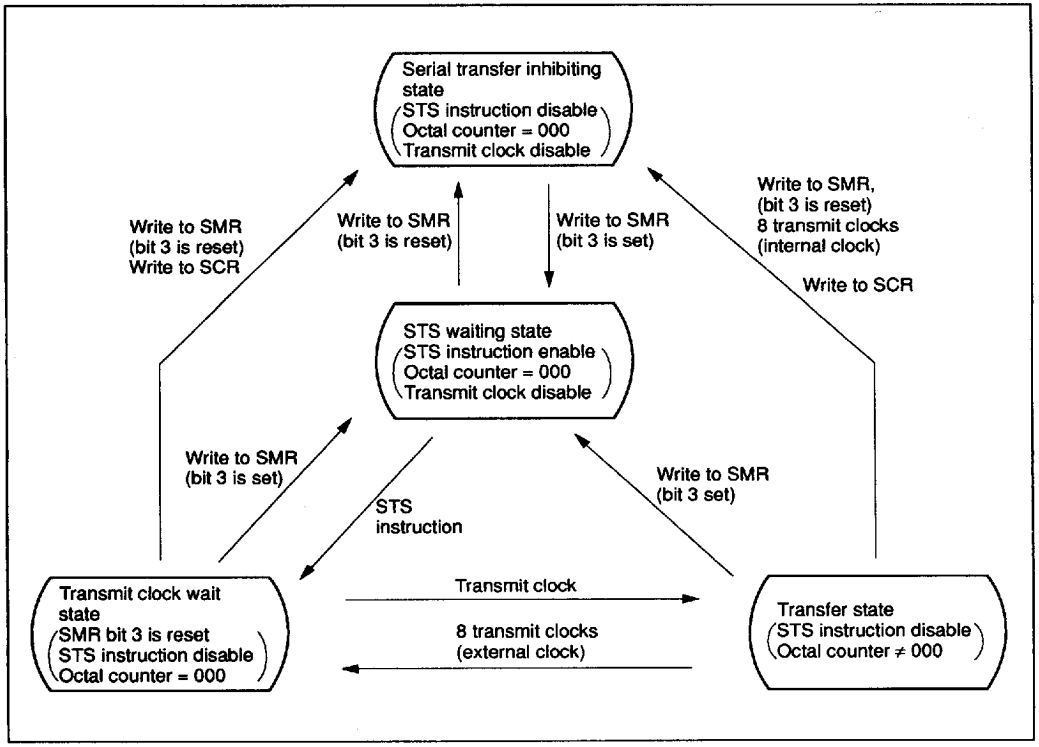


Figure 29 Serial Interface Operation State

Transmit Clock Error Detection: The serial interface malfunctions when a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error can be detected as shown in figure 30.

During the transmit clock wait state, more than 8 transmit clock inputs set the serial interface transmit state, the transmit clock wait state, and then the transmit state. If the serial interrupt request flag (IFS) is reset after SMR has been programmed to enter the STS wait state, the serial interrupt request flag is set again.

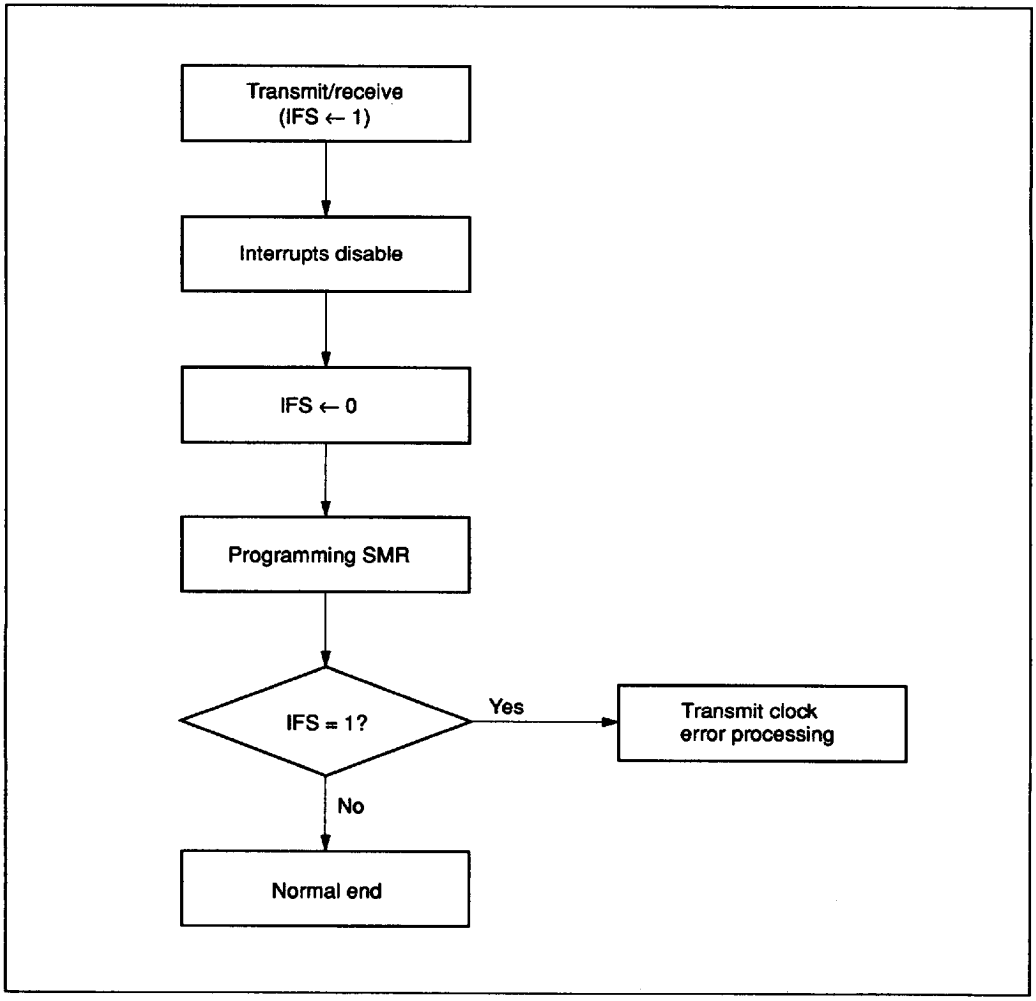


Figure 30 Example of Transmit Clock Error Detection

DTMF Receiver

The HD404678 Series has a high-/low-frequency group isolation circuit and a frequency measurement circuit for DTMF signal reception. A DTMF signal can be examined by these circuits. A block diagram of the DTMF receiver is shown in figure 31.

The DTMF signal is generated by mixing two sine waves, one of a group of four low frequencies (697, 770, 852, 941 Hz) and one of a group of four high frequencies (1209, 1336, 1477, 1633 Hz).

This signal is used for communication over telephone lines. A matrix of telephone pushbuttons and the corresponding DTMF frequencies is shown in figure 32.

The DTMF signal is a combination waveform that passes through a nonlinear telephone line, so the receiver recognizes that the signal will include harmonic and intermodulation components other than the two main frequencies.

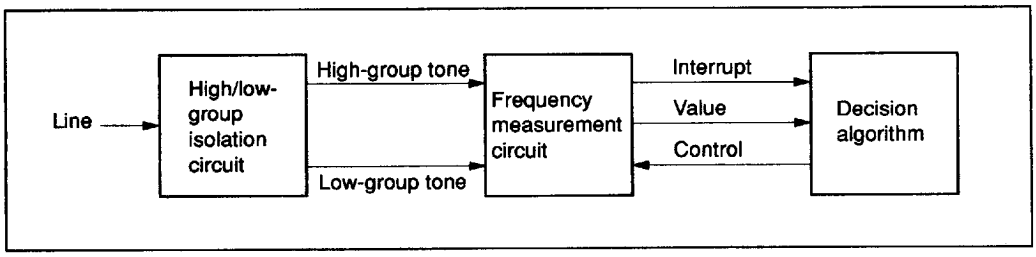


Figure 31 DTMF Receiver Block Diagram

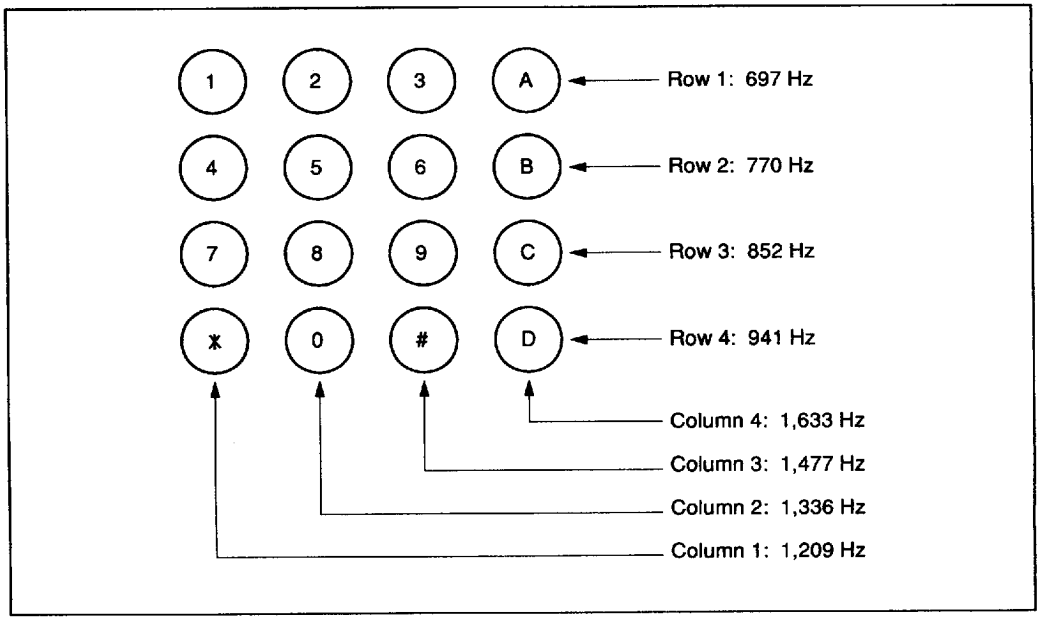


Figure 32 DTMF Keypad and Corresponding Frequencies

DTMF Receiver Configuration

High-/Low-Group Isolation Circuit: Consists of a gain control preamplifier, an anti-aliasing filter, high-/low-group bandpass filters, and high-precision comparators as shown in figure 33.

The gain control preamplifier compensates for line loss and loss generated within the telephone set. The anti-aliasing filter is an analog filter that reduces sampling noise in the switched capacitor filter (SCF) in the next stage. It employs a second-order Sallen-Key circuit having a cutoff of around 8 kHz (typ.). Each high-/low-group bandpass circuit is a sixth-order bandpass filter consisting of an SCF. The rejection ratio of high/low frequencies is designed to be 32 dB (figure 34).

Each high-precision comparator has an offset compensation circuit to detect the zero-crossing point of each signal isolated in the corresponding high- and low-frequency groups.

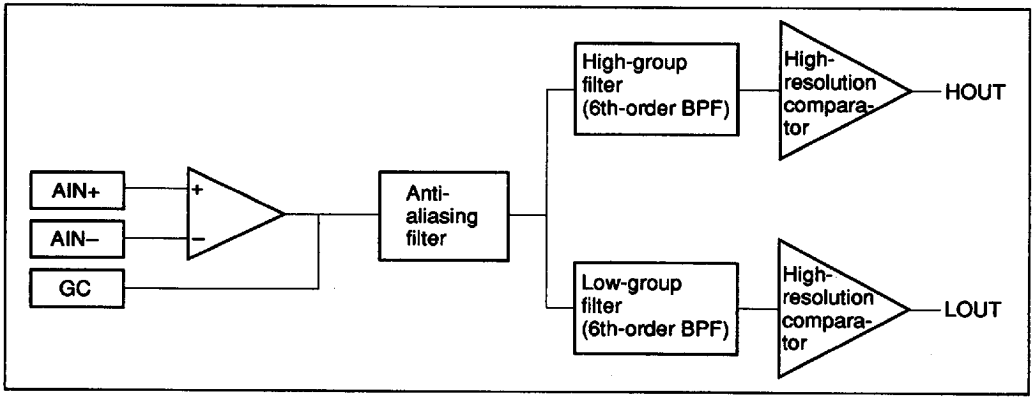


Figure 33 High-/Low-Group Isolation Circuit (Analog Block)

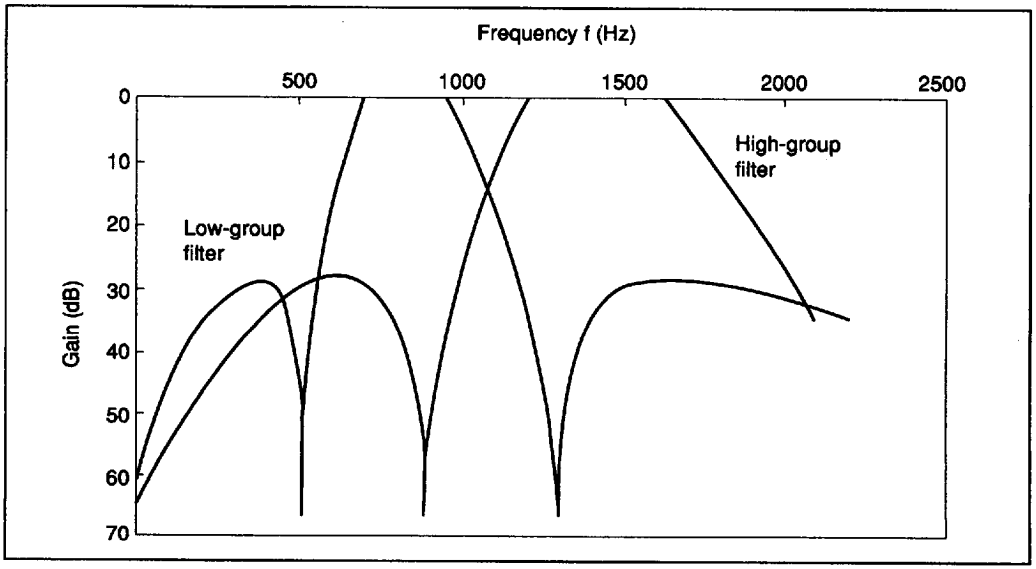


Figure 34 Frequency Characteristics of High-/Low-Group Isolation Circuit

Frequency Measurement Circuit: Consists of control sections that contain edge-generation circuits, edge counters, period counters, data registers, and flags as shown in figure 35.

Each edge counter is a 4-bit counter whose value can be set from a half cycle up to 7.5 cycles. Several cycles must be examined to prevent errors due to individual voice characteristics. Each period counter is a 10-bit counter in which one bit is equivalent to 10 µs for the high-frequency group or 20 µs for the low-frequency group. Each measurement value hold register is a 10-bit register that maps on three contiguous addresses in RAM.

To determine a frequency, the period between zero-crossings must be measured by the corresponding edge and period counters. The period counter counts the time until the edge counter reaches a target value. When the edge counter reaches that value, the value of the period counter at that point is fetched into the measurement value hold register. The edge and period counters are then initialized to start measuring the next cycle. At the same time, a load flag is set to show that the CPU acknowledges that a measurement value has been loaded into the measurement value hold register. The CPU can then identify DTMF signal transmission and its code by examining whether the value corresponds to a DTMF signal.

Tone Receiver Mode Register (TRM) (Low-Group (TRML): $024, High-Group (TRMH): $028): Retains the number of cycles to be measured by the frequency measurement circuit, and this value is set as a count in the edge counter.

The values in the TRM value are in half-cycle units, so $6 is set in the TRM for a three-cycle measurement. The frequency measurement circuit is initialized to measure the period of a signal by updating the value in the TRM.

When the TRM is $0, the frequency measurement circuit stops. This mode is useful when waiting for the filters to stabilize and when no signal is being examined.

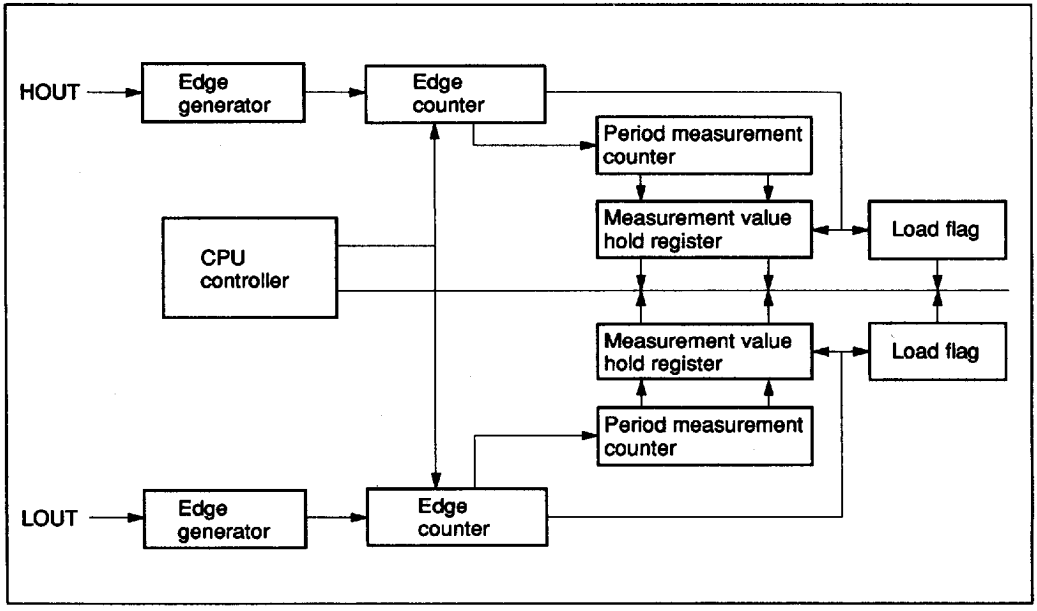


Figure 35 Frequency Measurement Circuit (Digital Block)

Tone Receiver Control Register (TRC: $02C): Consists of the 4 bits shown in table 29.

- TRON (bit 3): Tone receiver enable bit. When this bit is set, the analog circuit and period measurement circuit become active. Signal examination must be delayed for at least 100 ms after this bit is set, because the analog circuit needs at least ten milliseconds to stabilize.
- HGLF (bit 2): Indicates that data has been loaded into the data register of the high-group frequency measurement unit. This bit can be reset, but it cannot be set by software.
- LGLF (bit 1): Indicates that data has been loaded into the data register of the low-group frequency measurement unit. This bit can be reset, but it cannot be set by software.

Once the load flag has been set, the value in the data register is not updated even when the edge counter becomes equal to TRM again. Reset the load flag after the CPU has completed the process described above.

Table 29 Tone Receiver Control Register

Bit	Function
3	TRON
2	HGLF
1	LGLF
0	Not used

Table 30 DTMF Receiver Registers

Register Name	Address	Bit	Function
TRML	$024	0–3	Sets the number of measurement cycles for the low-group frequency
TDLL	$025	0–3	Contains low-group frequency period measurement data (bits 0–3)
TDLM	$026	0–3	Contains low-group frequency period measurement data (bits 4–7)
TDLU	$027	0, 1	Contains low-group frequency period measurement data (bits 8, 9)
		2, 3	Not used
TRMH	$028	0–3	Sets the number of measurement cycles for the high-group frequency
TDHL	$029	0–3	Contains high-group frequency period measurement data (bits 0–3)
TDHM	$02A	0–3	Contains high-group frequency period measurement data (bits 4–7)
TDHU	$02B	0, 1	Contains high-group frequency period measurement data (bits 8, 9)
		2, 3	Not used
TRC	$02C	0	Not used
		1	Low-group measurement data load flag (1: Load ended)
		2	High-group measurement data load flag (1: Load ended)
		3	DTMF receiver enable (0: Disabled, 1: Enabled)

Pin Description in PROM Mode

The HD4074678 is a ZTAT™ microcomputer incorporating PROM. In the PROM mode, the MCU does not operate and the HD4074678 can program the on-chip PROM.

	MCU Mode		PROM Mode			MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin Name	I/O
1	$R3_0$	I/O	A_{13}	I	33	D_7	I/O	O7	I/O
2	$R3_1$	I/O	A_{14}	I	34	D_8	I/O		
3	$R3_2/\overline{INT_0}$	I/O	$\overline{CE}$	I	35	D_9	I/O		
4	$R3_3/\overline{INT_1}$/TIB	I/O	$\overline{OE}$	I	36	D_{10}	I/O		
5	$R4_0/\overline{SCKA}$	I/O			37	D_{11}	I/O		
6	$R4_1$/SIA	I/O			38	D_{12}	I/O		
7	$R4_2$/SOA	I/O			39	D_{13}	I/O		
8	$R4_3$	I/O			40	D_{14}	I/O		
9	$R5_0/\overline{SCKB}$	I/O			41	D_{15}	I/O		
10	$R5_1$/SIB	I/O			42	$R8_0$	I	V_{PP}	
11	$R5_2$/SOB	I/O			43	$R8_1$	I	A_9	I
12	$R5_3$	I/O			44	$R8_2/R_{IN}$	I	$\overline{M_0}$	I
13	$R6_0$	I/O			45	$R8_3/R_{ref}$	I	$\overline{M_1}$	I
14	$R6_1$	I/O			46	V_{CC}		V_{CC}	
15	$R6_2/INT_2$/TIC	I/O			47	$R0_0$	I/O	A_1	I
16	$R6_3/INT_3$/TID	I/O			48	$R0_1$	I/O	A_2	I
17	$R7_0$/TOB	I/O			49	$R0_2$	I/O	A_3	I
18	$R7_1$/TOC	I/O			50	$R0_3$	I/O	A_4	I
19	$R7_2/TOD_1$	I/O			51	$R1_0$	I/O	A_5	I
20	$R7_3/TOD_2$	I/O			52	$R1_1$	I/O	A_6	I
21	RESET	I	RESET	I	53	$R1_2$	I/O	A_7	I
22	GND		GND		54	$R1_3$	I/O	A_8	I
23	OSC_1	I			55	AV_{CC}			
24	OSC_2	O			56	AIN–	I		
25	$\overline{TEST}$	I	$\overline{TEST}$	I	57	AIN+	I		
26	D_0	I/O	O0	I/O	58	GC	O		
27	D_1	I/O	O1	I/O	59	V_{ref}			
28	D_2	I/O	O2	I/O	60	AGND			
29	D_3	I/O	O3	I/O	61	$R2_0$	I/O	A_0	I
30	D_4	I/O	O4	I/O	62	$R2_1$	I/O	A_{10}	I
31	D_5	I/O	O5	I/O	63	$R2_2$	I/O	A_{11}	I
32	D_6	I/O	O6	I/O	64	$R2_3$	I/O	A_{12}	I

Note: I/O: Input/output pin, I: Input pin, O: Output pin

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling $\overline{TEST}$, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high as shown in figure 36. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 31.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower 5 bits and an upper 5 bits that are read from or written to consecutive addresses. This means that if, for example, 8 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 16-kbyte address space ($0000–$3FFF) must be specified.

Programming and Verification: The built-in PROM of the MCU can be programmed in a high-speed programming sequence without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 32.

For details of PROM programming, refer to the preface section.

Warnings

1. Always specify addresses $0000 to $3FFF when programming with a PROM programmer. If address $4000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. A voltage of 12.5 V is the Intel 27256 setting.

Table 31 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Manufacturer**	**Model Name**
DATA I/O Corp.	121B 29B	FP-64A	Hitachi	HS467ESH01H
AVAL Data Corp.	PKW-1000	FP-64A	Hitachi	HS467ESH01H

Table 32 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_7
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibition	High	High	V_{PP}	High impedance

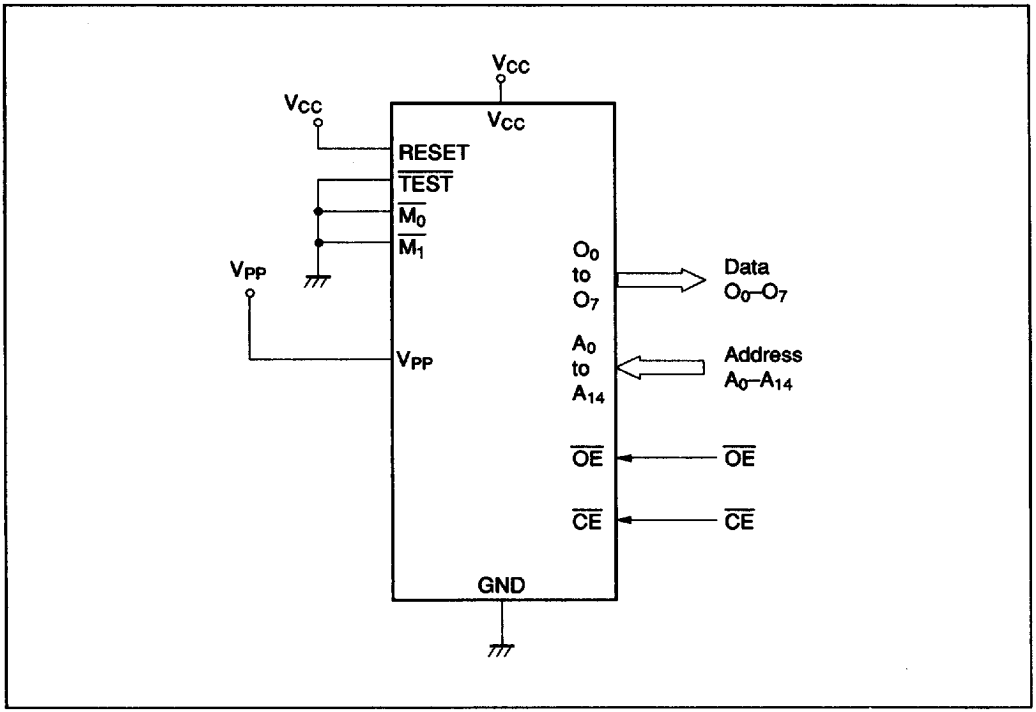


Figure 36 Connections in PROM Mode

Addressing Mode

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 37 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory register (MR), which consists of 16 addresses from $040 to $04F, is accessed with the LAMR and XMRA instructions.

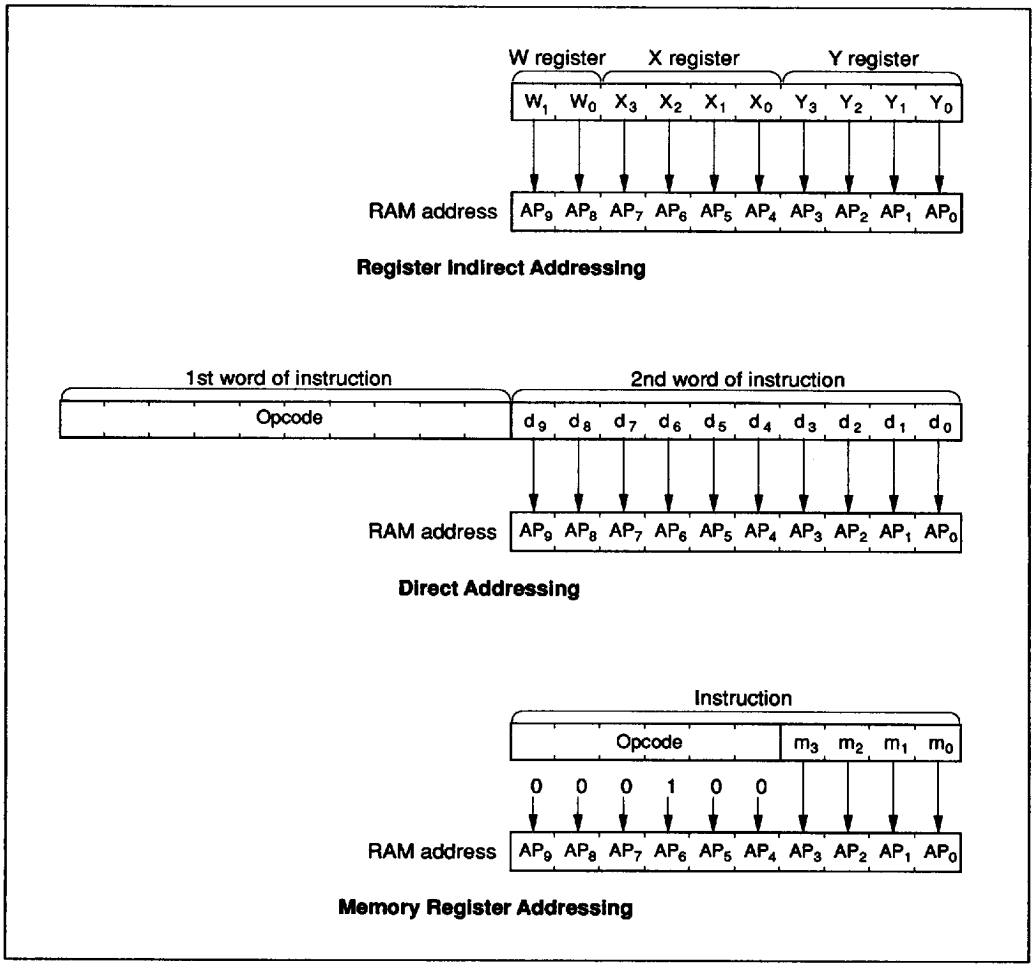


Figure 37 RAM Addressing Mode

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 38 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 32 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 39. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 40. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

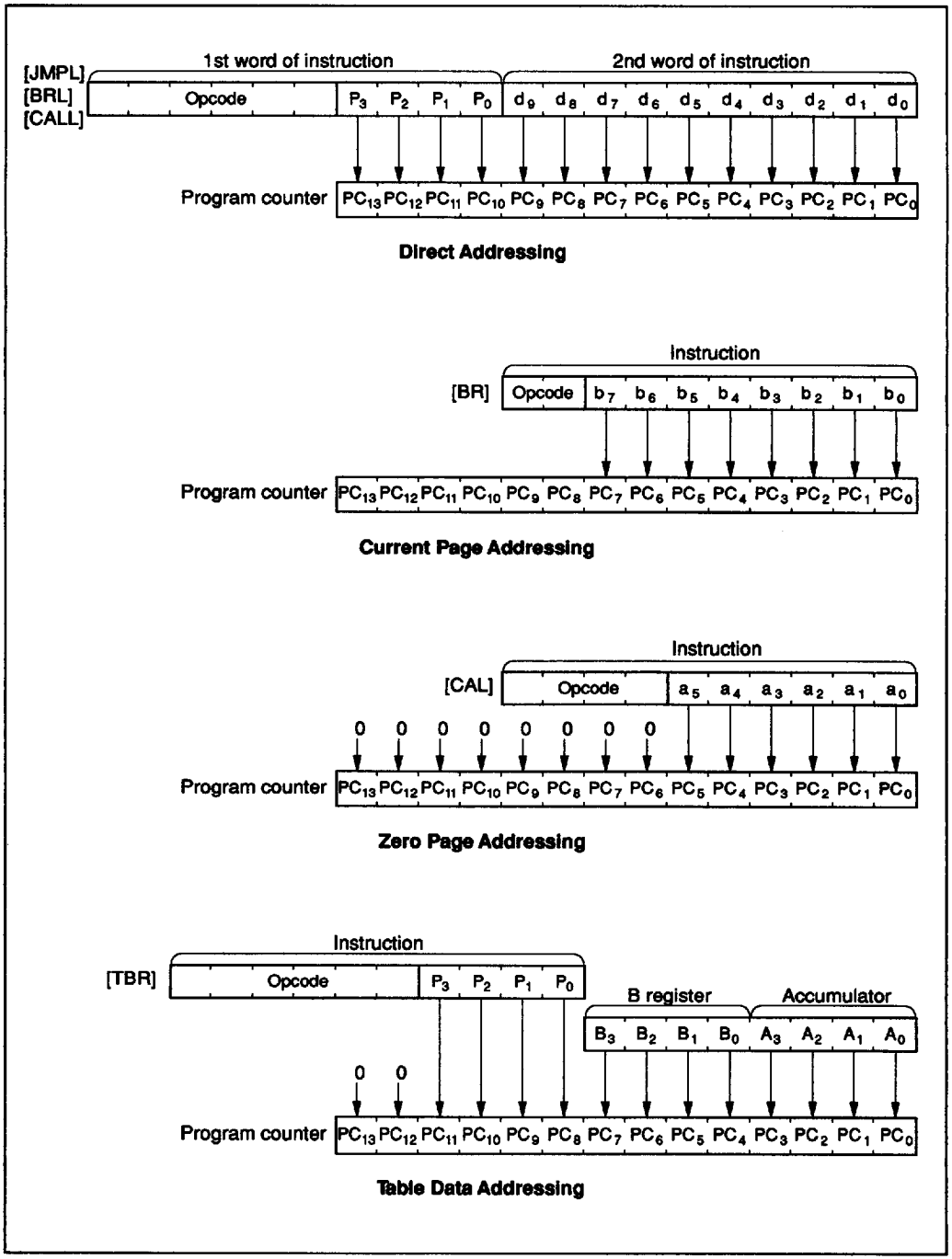


Figure 38 ROM Addressing Modes

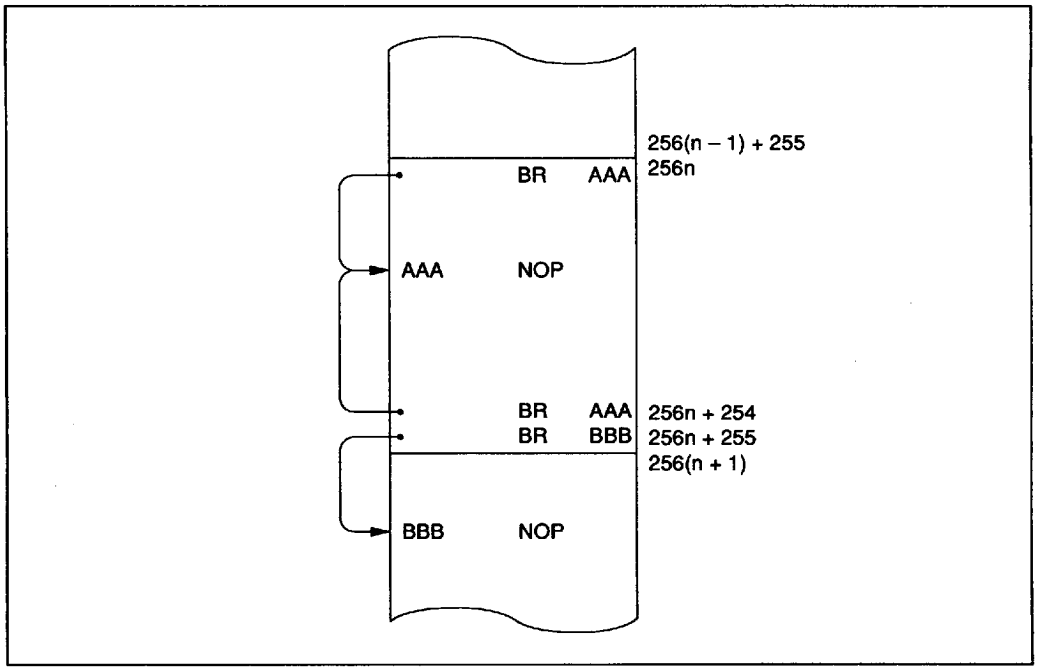


Figure 39 Page Boundary between BR Instruction and Branch Destination

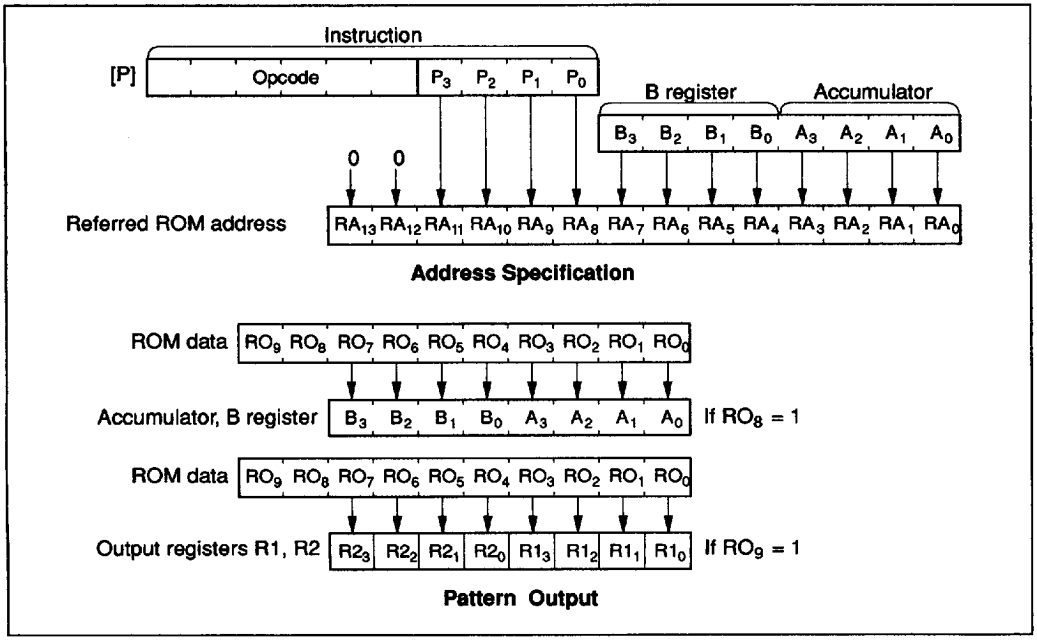


Figure 40 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	
Total permissible input current	ΣI_o	105	mA	1
Total permissible output current	$-\Sigma I_o$	60	mA	2
Maximum input current	I_o	4	mA	3, 4
		30	mA	3, 5
Maximum output current	$-I_o$	4	mA	6, 7
		20	mA	6, 8
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
2. Total permissible output current is the sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
3. Maximum input current is the maximum amount of input current from each I/O pin to GND.
4. Applies to D_{10}–D_{15} and R0–R7.
5. Applies to D_0–D_9.
6. Maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
7. Applies to D_0–D_9 and R0–R7.
8. Applies to D_{10}–D_{15}.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET	0.85V_{CC}	—	V_{CC} + 0.3	V		
		$\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{SCKA}$, $\overline{SCKB}$	0.8V_{CC}	—	V_{CC} + 0.3	V		
		SIA, SIB	0.8V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	External clock operation	
Input low voltage	V_{IL}	RESET	–0.3	—	0.15V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{SCKA}$, $\overline{SCKB}$	–0.3	—	0.2V_{CC}	V		
		SIA, SIB	–0.3	—	0.2V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	External clock operation	
Output high voltage	V_{OH}	$\overline{SCKA}$, SOA, $\overline{SCKB}$, SOB, TOB, TOC, TOD_1, TOD_2	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
Output low voltage	V_{OL}	$\overline{SCKA}$, SOA, $\overline{SCKB}$, SOB, TOB, TOC, TOD_1, TOD_2	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	RESET, OSC_1, $\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3, $\overline{SCKA}$, SIA, $\overline{SCKB}$, SIB	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, DTMF receiver and analog comparator stop	2
	I_{CCA}	V_{CC}	—	—	20	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, DTMF receiver operates	3
	I_{CCB}	V_{CC}	—	—	7	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, Analog comparator operates	4

DC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Maximum logic operation	5
	I_{SBY2}	V_{CC}	—	—	3	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Minimum logic operation	
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V	6
Stop mode retaining voltage	V_{STOP}	V_{CC}	2.0	—	—	V		7

Notes:
1. Output buffer current is excluded.
2. The MCU is in the reset state. Input/output current does not flow. The test conditions are:
   MCU: Reset
   Pin: RESET, $\overline{TEST}$: V_{CC}
3. DTMF signal receive mode. Input/output current does not flow.
4. Analog comparator operates and input/output current does not flow.
5. The timer operates with the fastest clock and input/output current does not flow. The test conditions are:
   MCU: Standby mode
   Input/output: Reset state
   Serial interface: Stop
   Timer: Prescaler divide ratio is ÷2
   Pin: RESET: GND
   $\overline{TEST}$: V_{CC}
6. Input/output current does not flow. The test conditions are:
   MCU: Stop mode
   Pin: RESET: GND
   $\overline{TEST}$: V_{CC}
7. RAM data is retained.

Input/Output Characteristics for Standard Pins (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C unless otherwise specified)

Item	Symbol	Pin Name	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R0–R8	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	R0–R8	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R0–R7	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
Output low voltage	V_{OL}	R0–R7	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	R0–R7, $R8_1$–$R8_3$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$R8_0$	—	—	1			2
			—	—	20			3
Input high/ low voltage	VR_{INH}	$R8_2$	VR_{ref} + 0.1	—	—	V	Variable voltage reset mode	
	VR_{INL}		—	—	VR_{ref} – 0.1			
Analog input reference voltage range	VR_{ref}	$R8_3$	0	—	V_{CC} – 1.2	V		
Pull-up MOS current	$-I_{PU}$	R0–R5	20	100	200	µA	V_{CC} = 5.0 V V_{in} = 0 V	
Pull-down MOS current	I_{PD}	R6–R8	20	100	200	µA	V_{CC} = 5.0 V V_{in} = 5.0 V	

Notes: 1. Output buffer current is excluded.
2. Applies to HD404676 and HD404678.
3. Applies to HD4074678.

Input/Output Characteristics for High-Current Pins (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{15}	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{15}	–0.3	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_{10}–D_{15}	2.0	—	—	V	$-I_{OH}$ = 10 mA	
		D_0–D_{15}	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
Output low voltage	V_{OL}	D_0–D_9	—	—	2.0	V	I_{OL} = 15 mA	
		D_0–D_{15}			0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{15}	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$-I_{PU}$	D_0–D_9	20	100	200	µA	V_{CC} = 5.0 V V_{in} = 0 V	
Pull-down MOS current	I_{PD}	D_{10}–D_{15}	20	100	200	µA	V_{CC} = 5.0 V V_{in} = 5.0 V	

Note: 1. Output buffer current is excluded.

AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item		Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Crystal oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	1	4	4.2	MHz		
	Instruction cycle time	t_{cyc}		1.91	2	8	µs		
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
External clock operation	External clock frequency	f_{CP}	OSC_1	1	4	4.2	MHz		2
	External clock high width	t_{CPH}	OSC_1	82	—	—	ns		2
	External clock low width	t_{CPL}	OSC_1	82	—	—	ns		2
	External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2

AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified) (cont)

Item		Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
External clock operation (cont)	External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
	Instruction cycle time	t_{cyc}		1.91	2	8	µs		2
External interrupt signal high width		t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3	2	—	—	t_{cyc}		3
External interrupt signal low width		t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, INT_2, INT_3	2	—	—	t_{cyc}		3
RESET high width		t_{RSTH}	RESET	3	—	—	t_{cyc}		4
Input capacitance		C_{in}	Except $R8_0$	—	—	15	pF	f = 1 MHz V_{in} = 0 V	
			$R8_0$	—	—	15	pF		7
				—	—	90	pF		8
RESET fall time		t_{RSTf}		—	—	20	ms		4
Analog comparator stabilization time		t_{CSTB}	$R8_2$	—	—	2	t_{cyc}	Variable voltage reset mode	5
DTMF receiver filter stabilization time		t_{DTMFR}		—	—	120	ms	DTMF receive mode	6

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 4.5 V at power-on or after RESET input goes high after stop mode is cancelled. At power-on and when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. If using a crystal oscillator, contact the manufacturer to determine what oscillation stabilization time is required, since it depends on the circuit constants and stray capacitances.
2. Refer to figure 41.
3. Refer to figure 42.
4. Refer to figure 43.
5. t_{CSTB} is the time required for the analog comparator to stabilize after $R8_2$ enters variable voltage reset mode.
6. t_{DTMFR} is the time required for the filter and comparator to stabilize to read correct data after the DTMFR enable bit is set to 1.
7. Applies to HD404676 and HD404678.
8. Applies to HD4074678.

Serial Interface Timing Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCKA}$, $\overline{SCKB}$	1	—	—	t_{cyc}	Refer to figure 45	1
Transmit clock high width	t_{SCKH}	$\overline{SCKA}$, $\overline{SCKB}$	0.5	—	—	t_{Scyc}	Refer to figure 45	1
Transmit clock low width	t_{SCKL}	$\overline{SCKA}$, $\overline{SCKB}$	0.5	—	—	t_{Scyc}	Refer to figure 45	1
Transmit clock rise time	t_{SCKr}	$\overline{SCKA}$, $\overline{SCKB}$	—	—	100	ns	Refer to figure 45	1
Transmit clock fall time	t_{SCKf}	$\overline{SCKA}$, $\overline{SCKB}$	—	—	100	ns	Refer to figure 45	1
Serial output data delay time	t_{DSO}	SOA, SOB	—	—	250	ns	Refer to figure 45	1
Serial input data setup time	t_{SSI}	SIA, SIB	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SIA, SIB	150	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCKA}$, $\overline{SCKB}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCKA}$, $\overline{SCKB}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCKA}$, $\overline{SCKB}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCKA}$, $\overline{SCKB}$	—	—	100	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCKA}$, $\overline{SCKB}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SOA, SOB	—	—	250	ns	Refer to figure 45	1
Serial input data setup time	t_{SSI}	SIA, SIB	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SIA, SIB	150	—	—	ns		1
Transmit clock end detection time	t_{SCKHD}	$\overline{SCKA}$, $\overline{SCKB}$	1	—	—	t_{cyc}		1, 2

Notes are on next page.

Notes: 1. Refer to figure 44.
2. Transmit clock end detection time is the high level period after 8 pulses of transmit clock are input. The serial interrupt request flag is not set when the next transmit clock is input before the transmit clock end detection time has passed.

DTMF Receiver Characteristics (V_{CC} = 5 V, GND = 0 V, T_a = 25°C, f_{OSC} = 4.00 MHz)

Item		Min	Typ	Max	Unit	Test Condition	Unit	Notes
Dynamic range	Valid input signal levels (each composite signal tone)	–29.0	—	+1.0	dBm			1, 2, 5
	Noise tolerance	—	–16	—	dB			1, 3, 5
	Hum tolerance	—	+20	—	dB			1, 5
	Dial tone tolerance	—	0	—	dB			1, 5
Twist	Positive/negative twist accept	—	±10	—	dB			1, 5
Accuracy	Frequency deviation accept	—	±1.8	—	%			1, 5
	Frequency deviation reject	—	±3.5	—	%			1, 5
Speech immunity		—	2	—	No. of times			1, 4, 5

Notes: 1. Receiver characteristics evaluated program is used.
2. dBm = decibels above or below a reference power of 1 mW into a 600-Ω load.
3. Noise power is the total power of white noise (300 Hz – 3.4 kHz).
4. MITEL standard tape is used.
5. Use the measurement circuit (figure 46).

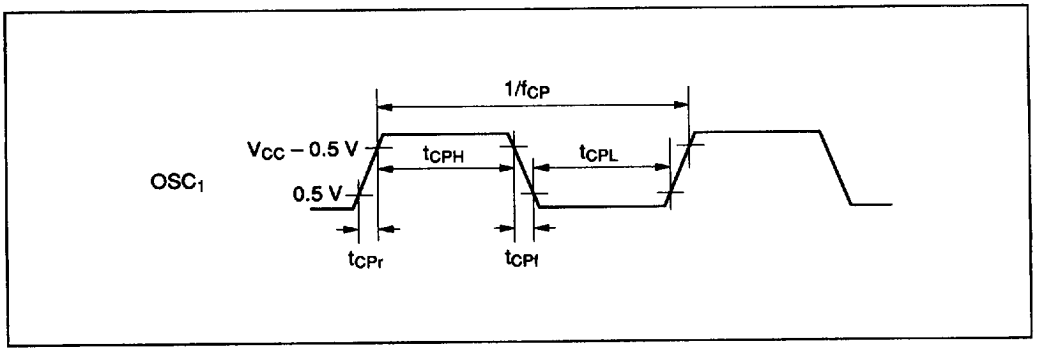


Figure 41 External Clock Timing

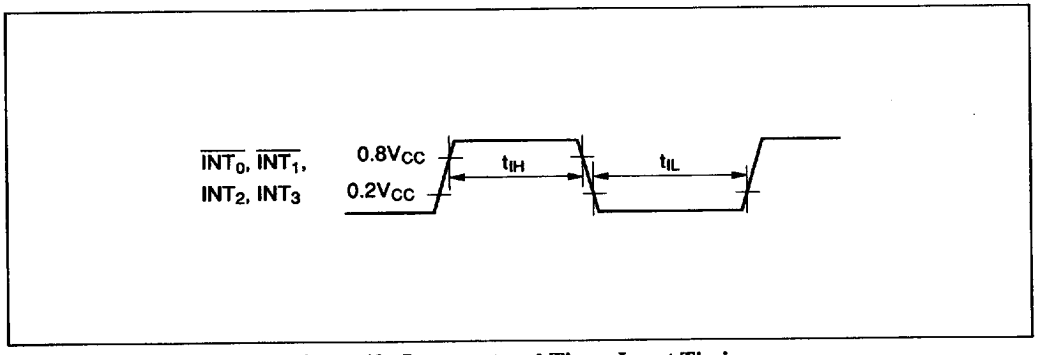


Figure 42 Interrupt and Timer Input Timing

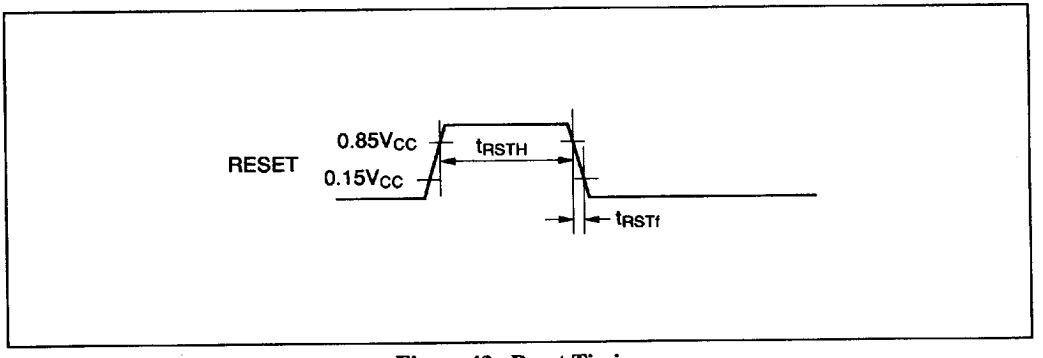


Figure 43 Reset Timing

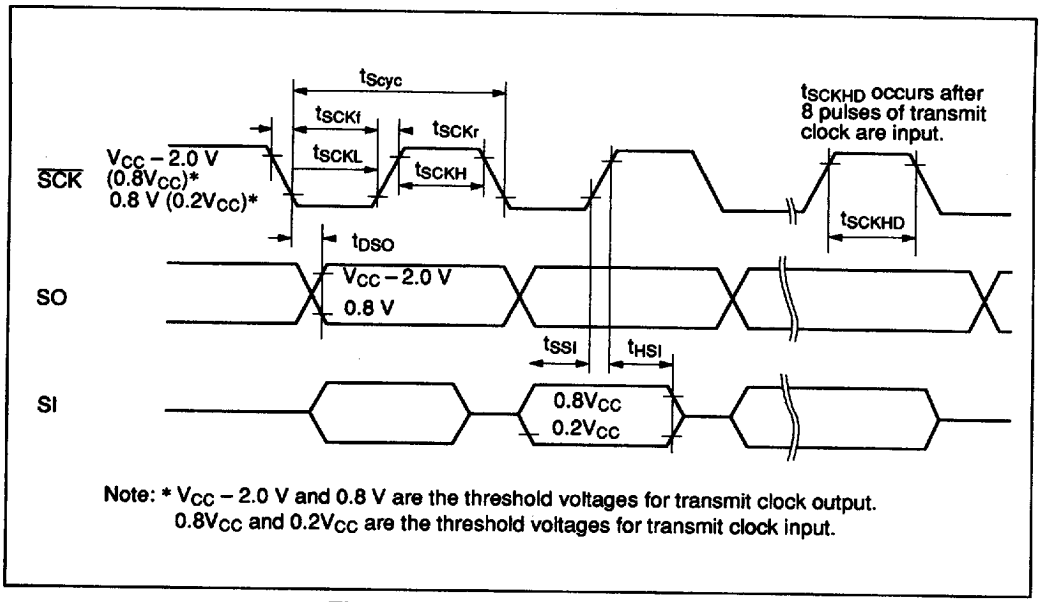


Figure 44 Timing of Serial Interface

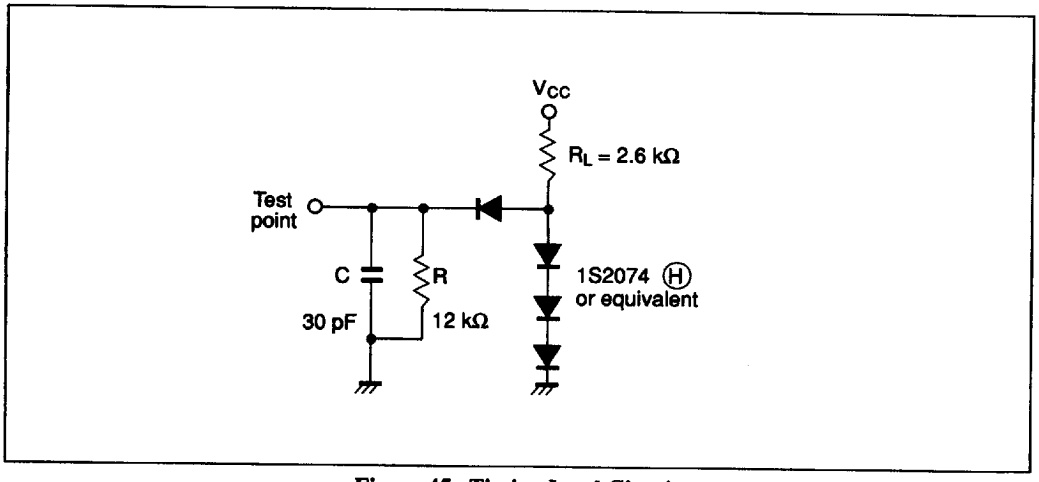


Figure 45 Timing Load Circuit

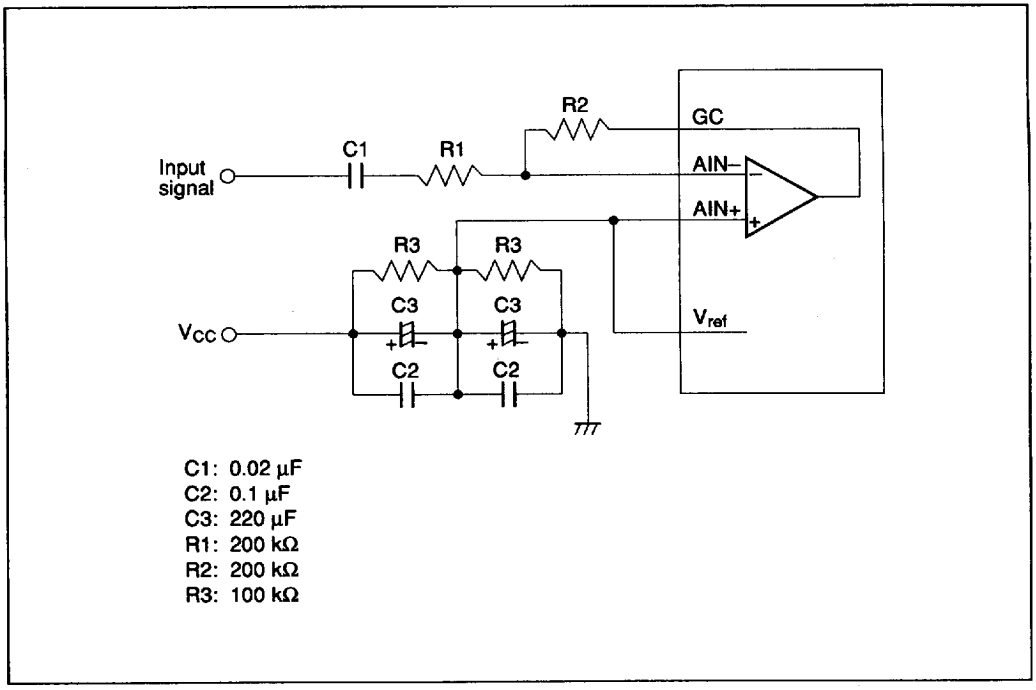


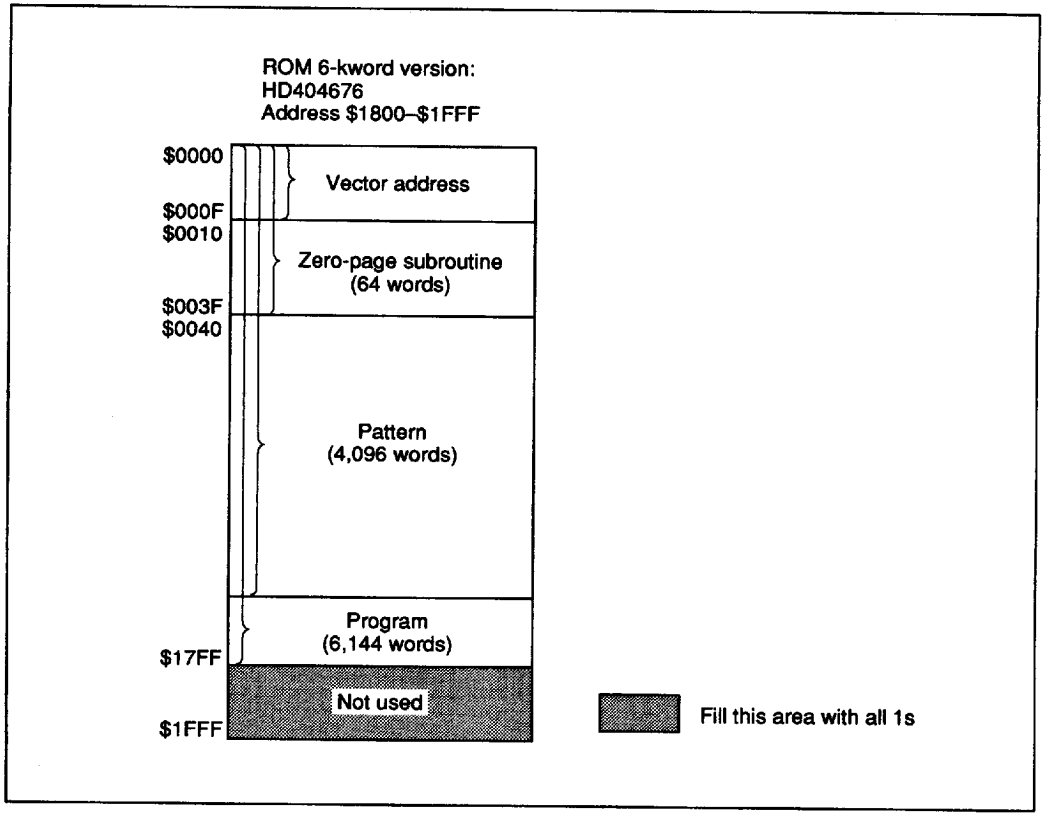
Figure 46 DTMF Receive Signal Characteristic Measurement Circuit

Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as an 8-kword version (HD404678). An 8-kword data size is required to change ROM data to mask manufacturing data since the program used is for an 8-kword version.

This limitation applies when using EPROM or a data base.



HD404676/HD404678 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404676	6-kword
☐ HD404678	8-kword

2. ROM Code Media
Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. Oscillator for OSC1 and OSC2

☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop Mode

☐ Used
☐ Not used

5. Package

■ FP-64A