HD404708/HD404709/ HD4074709

Description

The MCU are 4-bit single-chip HMCS400 series microcomputers providing high programming productivity. They incorporate high-voltage I/O pins, a Vacuum Fluorescent Display (VFD) controller/driver, a pulse width modulation output circuit, and a 32.768 kHz oscillator used for the precise watch.

Features

- 8192 words × 10 bits ROM (HD404708)
  16384 words × 10 bits ROM (HD404709)
  16384 words × 10 bits PROM (HD4074709)
  (The PROM is compatible with the 27256 type.)
- 576 digits × 4 bits RAM
- 56 I/O pins including 32 high-voltage (max. 40V), high current (max. 15mA) pins.
- Three on-chip timer/counters
- Clock synchronous 8-bit serial interface
- 14 bit PWM D/A converter
- Four external (including two double-edged) and five internal interrupt sources
- Subroutine stack which allows up to 16 levels including interrupts
- Three low power dissipation modes: Standby mode, Watch mode, Stop mode
- Two builtin oscillators: System/subsystem oscillator
- Instruction cycle time: 0.89μs (V_{CC} = 3.5 – 6V)
- Modes: MCU mode
  PROM mode (HD4074709)

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Type of Products

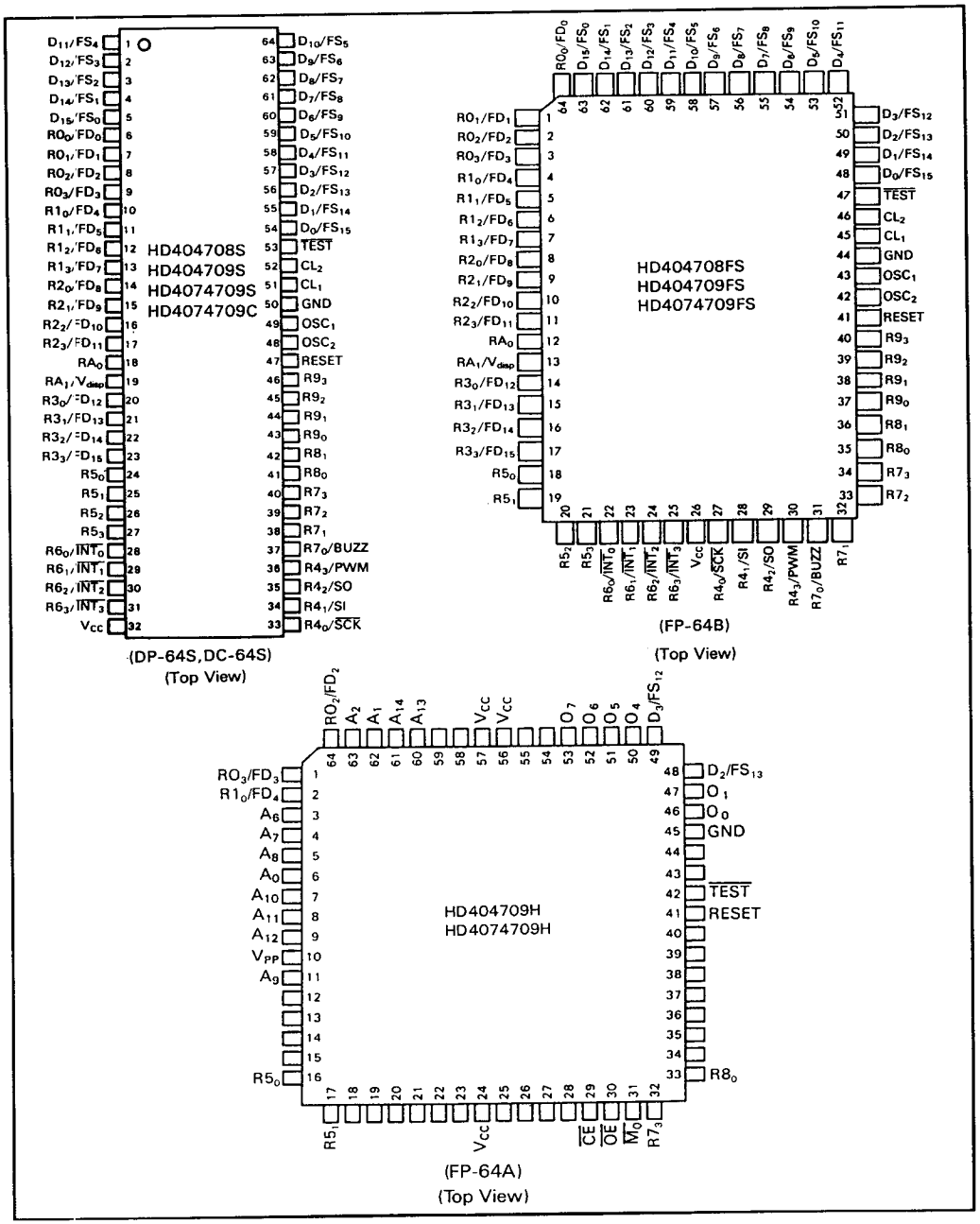
Mask ROM type (* * *: ROM code)

Part No.	ROM (Words)	Package
HD404708***S	8192	DP-64S
HD404708***FS		FP-64B
HD404709***S	16384	DP-64S
HD404709***FS		FP-64B
HD404709***H		FP-64A

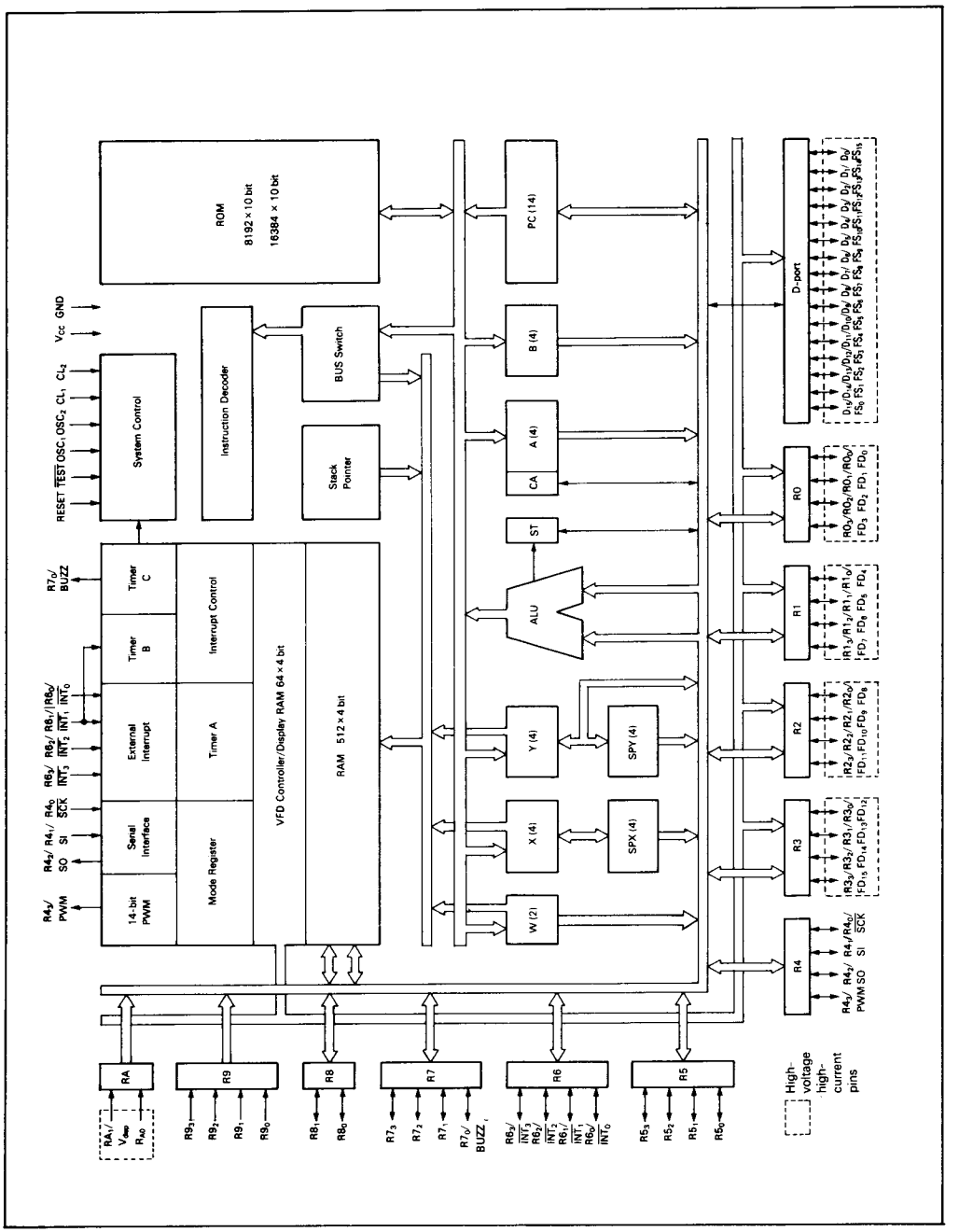
ZTAT type

Part No.	ROM (Words)	Package
HD4074709S	16384	DP-64S
HD4074709FS		FP-64B
HD4074709C		DC-64S
HD4074709H		FP-64A

Pin Arrangment



Block Diagram



Pin Description

GND, V_{CC} (Power)

These are the power supply pins for the MCU. Connect the GND to the ground (0V) and apply the V_{CC} power supply voltage to V_{CC}.

$\overline{TEST}$

$\overline{TEST}$ is used for test purposes only. $\overline{TEST}$ must be connected to V_{CC}.

RESET

RESET resets the MCU.

OSC_1, OSC_2

OSC_1 and OSC_2 are input and output pin for the internal oscillator circuit. They can be connected to a crystal resonator, a ceramic filter resonator. In the case of an external oscillator circuit, an external clock signal is connected to OSC_1 and OSC_2 is open.

CL_1, CL_2

These pins are input pins for the 32.768 kHz crystal oscillator used for the precise watch.

D_0 – D_{15} (D Ports)

The D ports are input/output ports addressed by bit. Each port output consists of an open-drain PMOS, which realizes high-voltage and high drive current capability on these port pins. These pins are multiplexed with the segment pins used for the VFD controller.

R0 – RA (R Ports)

The R ports are 4-bit ports, except for R8 and RA which are addressed by 2 bits. R9 and RA are input ports and R0 to R8 are input/output ports. While R4 to R9 port pins are standard pins, R0 to R3 and RA pins are high-voltage pins. Each R0 to R3 output consists of an open-drain PMOS which realizes high-voltage and high drive current capability on these port pins. These pins are multiplexed with the digit pins for the VFD controller. Port pins $R4_0$ to $R4_3$, $R6_0$ to $R6_3$ and $R7_0$ are multiplexed with peripheral pins.

$\overline{INT_0}$, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{INT_3}$ (Interrupts)

These signals externally interrupt the MCU. $\overline{INT_1}$ can be also used as an external event input for timer B. $\overline{INT_0}$ to $\overline{INT_3}$ are multiplexed with $R6_0$ to $R6_3$, respectively.

$\overline{SCK}$, SI, SO (Serial Communications Interface)

The MCU is provided with a clock input/output ($\overline{SCK}$), receive data input (SI), and transmit data output (SO) for a serial communications interface. $\overline{SCK}$, SI and SO are multiplexed with $R4_0$ to $R4_2$, respectively.

BUZZ (Timer Output)

This pin outputs a variable-duty square wave. It is multiplexed with $R7_0$.

FD_0 – FD_{15}, FS_0 – FS_{15} (VFD Controller)

FD_0 to FD_{15} are the digit pins for the VFD (Vacuum Fluorescent Display) controller. They are multiplexed with port pins R0 to R3. FS_0 to FS_{15} are the segment pins for the VFD controller. They are multiplexed with the D port pins.

PWM (PWM D/A Converter)

This pin output a square wave from the PWM D/A converter. It is multiplexed with pin $R4_3$.

Functional Description

ROM Memory Map

The following paragraphs describe the ROM in detail. Figure 1 shows the ROM memory map.

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for the JMPL instruction which results in a branch to the starting address of the reset routine and the starting address of the interrupt service routine. After reset or interrupt execution, the program starts from the vector address.

Zero-page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines to which the CAL instruction branches the program.

Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data which can be referred to as a pattern by the P instruction.

Program Area ($0000 to $1FFF : HD404708, $0000 to $3FFF : HD404709/HD4074709): Locations $0000 through $1FFF, $3FFF can be used for the program code.

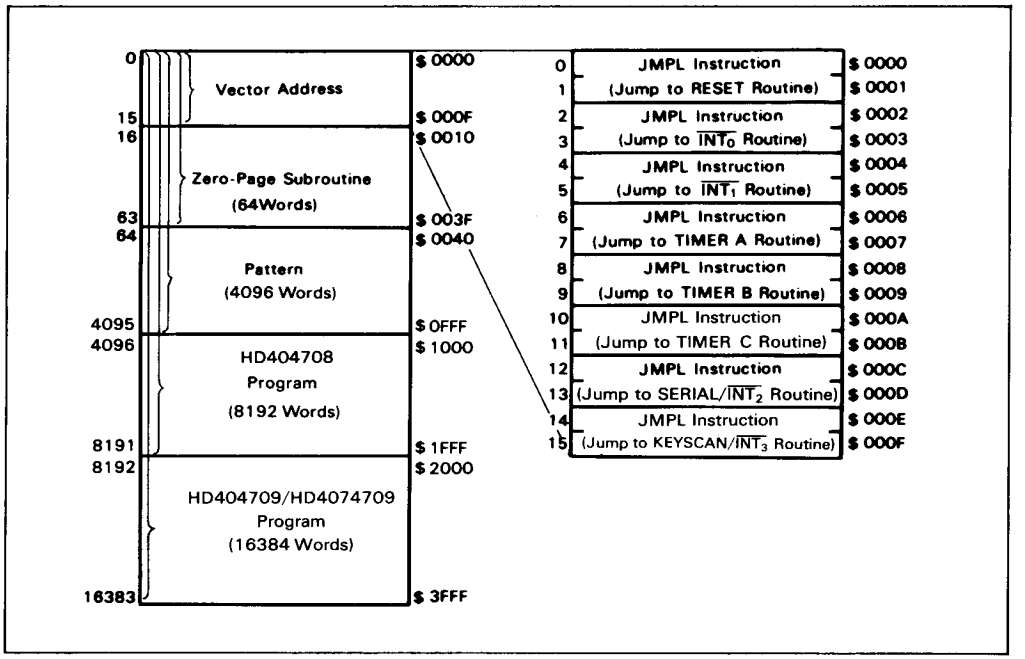


Figure 1. ROM Memory Map

RAM Memory Map

The MCU contains 512 digits of 4-bit RAM for the data and stack areas. In addition to these areas, interrupt control bits, special function registers and a VFD data area are also mapped on the RAM. The following paragraphs describe the RAM in detail. Figure 2 shows the RAM memory map.

Interrupt Control Bit Area ($000 to $003, $020 to $023): This area is used for interrupt control. Figure 3 shows this area. It can be accessed only by the RAM bit manipulation instructions.

The interrupt request flag cannot be set by software. The RSP bit resets only the stack pointer. The state of the LSON flag depends on the low power mode. The WDON flag is affected by the SEM and SEMD instructions only.

Special Function Registers Area ($004 to $01F, $024 to $03F): This area consists of mode or data registers for external interrupts, the serial interface, the timer/counter, and data control registers for all I/O ports. There are three types of the registers: read-only, write-only and read/write. These registers cannot be affected by the RAM bit manipulation instructions.

VFD Data Area ($060 to $09F): This area stores the data to be displayed on the VFD. This data automatically appears in the VFD segment. Data "1" indicates the segment is ON and "0" indicates OFF. Also, this area is available as a data area.

Data Area ($040 to $04F, $0A0 to $24F): Location $040 through $04F, the memory registers (MR), can be also accessed by the LAMR and XMRA instructions. Figure 4 shows memory register area.

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for the stack area to save the contents of the program counter (PC), the status flag (ST) and the carry flag (CA) during subroutine calls (the CAL and CALL instructions) or during interrupt servicing. One level of subroutine requires four digits, which allows the programmer to use up to 16 levels of subroutines. Figure 4 shows the stack area and saved data. The program counter is popped off the stack by the RTN and RTNI instructions, while the status and carry flags are popped off the stack only by the RTNI instruction. The unused area is available as a data area.

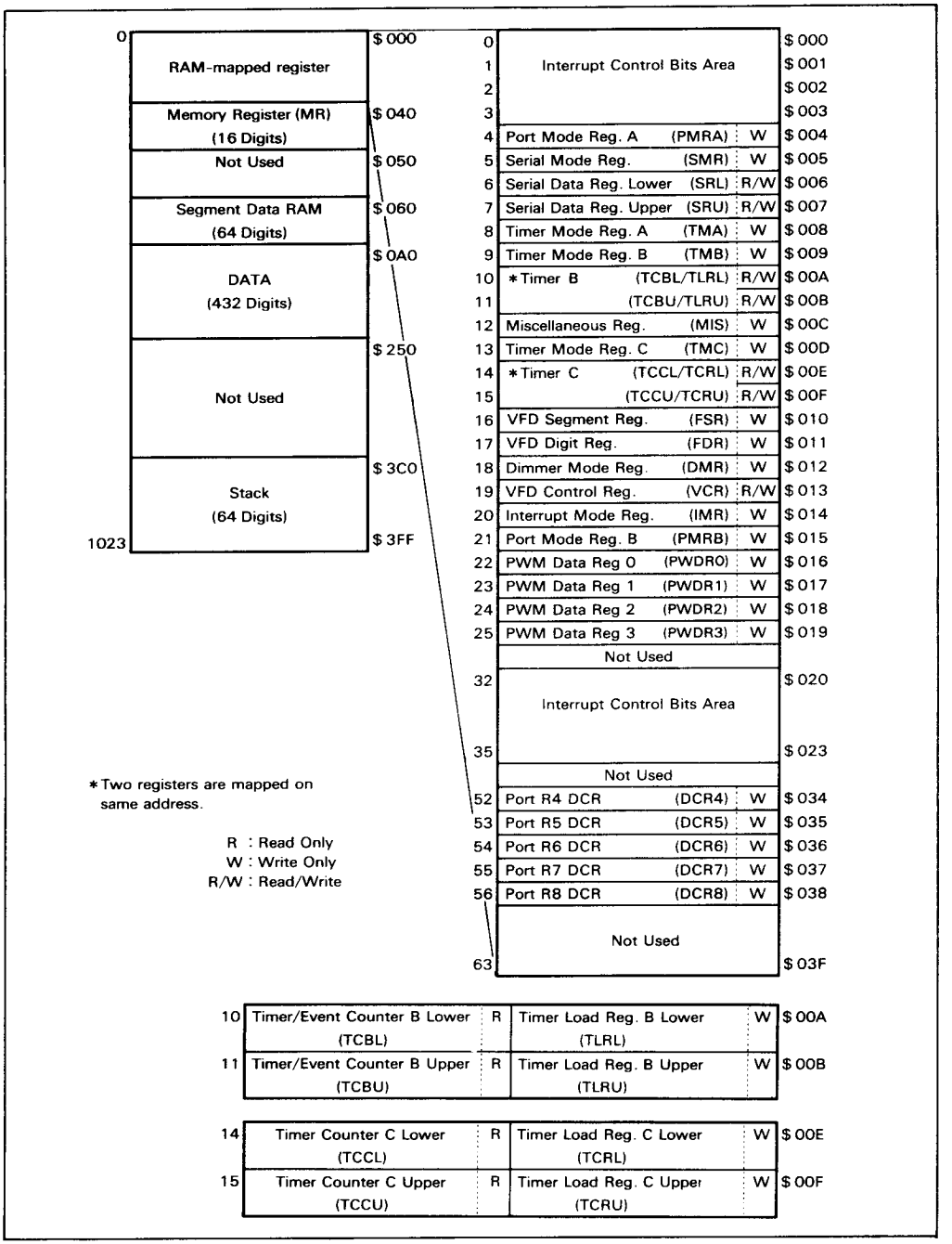


Figure 2. RAM Memory Map

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER A)	IFTA (IF of TIMER A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of TIMER C)	IFTC (IF of TIMER C)	IMTB (IM of TIMER B)	IFTB (IF of TIMER B)	$002
3	IMKS (IM of KEY SCAN)	IFKS (IF of KEY SCAN)	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

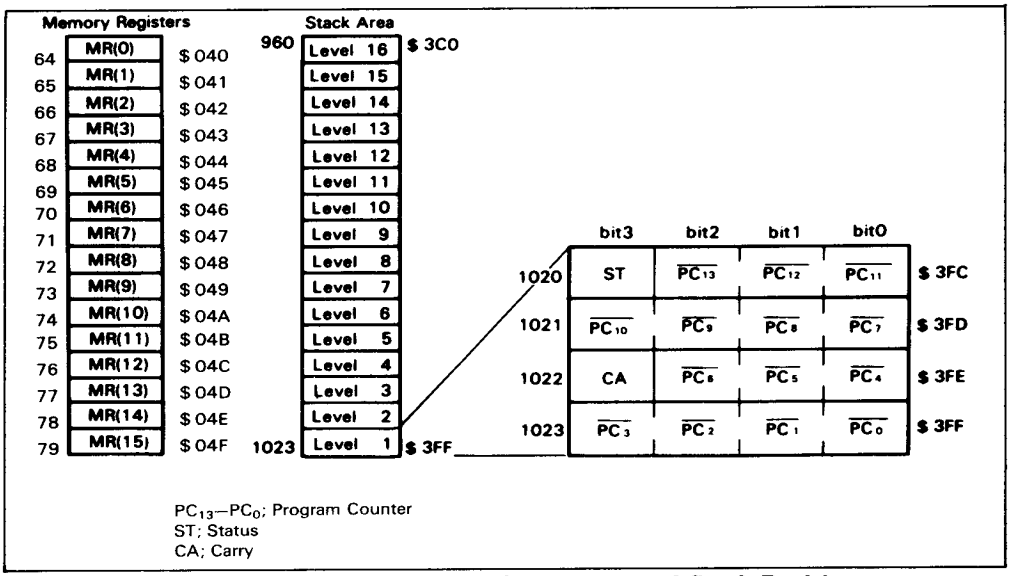
IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer

(Note) Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. This bit is not affected by other instructions. Furthermore, IF (interrupt request flag) is not affected by the SEM/SEMD instruction. The contents of status become invalid when the RSP bit and the bits which do not exist are tested.

	bit 3	bit 2	bit 1	bit 0	
0			WDON (Watch Dog ON Flag)	LSON (Low Speed ON Flag)	$020
1					$021
2	Reserved				$022
3	IM_3 (IM of $\overline{INT_3}$)	IF_3 (IF of $\overline{INT_3}$)	IM_2 (IM of $\overline{INT_2}$)	IF_2 (IF of $\overline{INT_2}$)	$023

(Note) The WDON flag is set by the SEM/SEMD instruction and reset by the MCU reset.
The contents of status become invarid when the WDON flag and the bits which do not exist are tested.

Figure 3. Interrupt Control Bits Area and Register Flag Area



PC_{13}—PC_0; Program Counter
ST; Status
CA; Carry

Figure 4. Memory Register, Stack Area and Stack Position

Register and Flags

The MCU has nine registers and two flags for CPU operation. The following paragraphs describe the registers and flags in detail. Figure 5 shows these registers and flags.

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the Arithmetic Logic Unit (ALU) as well as transfer data between memories, I/O and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers indirectly address the RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are used to assist the X and Y registers, respectively.

Carry (CA): The carry flag (CA) indicates an overflow resulting from the ALU during arithmetic operation. It is also affected by the SEC, REC, ROTL and ROTR instructions. The content of the carry flag is pushed onto the stack during interrupt servicing, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Status (ST): The status flag (ST) indicates an ALU overflow and ALU non-zero during arithmetic or compare instructions and the result of the bit test instruction. Moreover, the status flag controls branches caused by the BR, BRL, CAL or CALL instructions. Whether these instructions are executed or skipped, the status flag is set to 1. The state of this flag remains unchanged until the next arithmetic, compare, bit test, and branch instruction is executed. During interrupt servicing, the content of the status is pushed onto the stack, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which holds the ROM address.

Stack Pointer (SP): The stack pointer (SP) is a 10-bit register which indicates the next stack address. This pointer, which is initialized to $3FF, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped off the stack. The highest four bits are fixed to 1111, which allows the pointer to indicate up to 16 levels of subroutines. The stack pointer is initialized when the MCU is reset or the RSP bit is reset by the REM or REMD instructions.

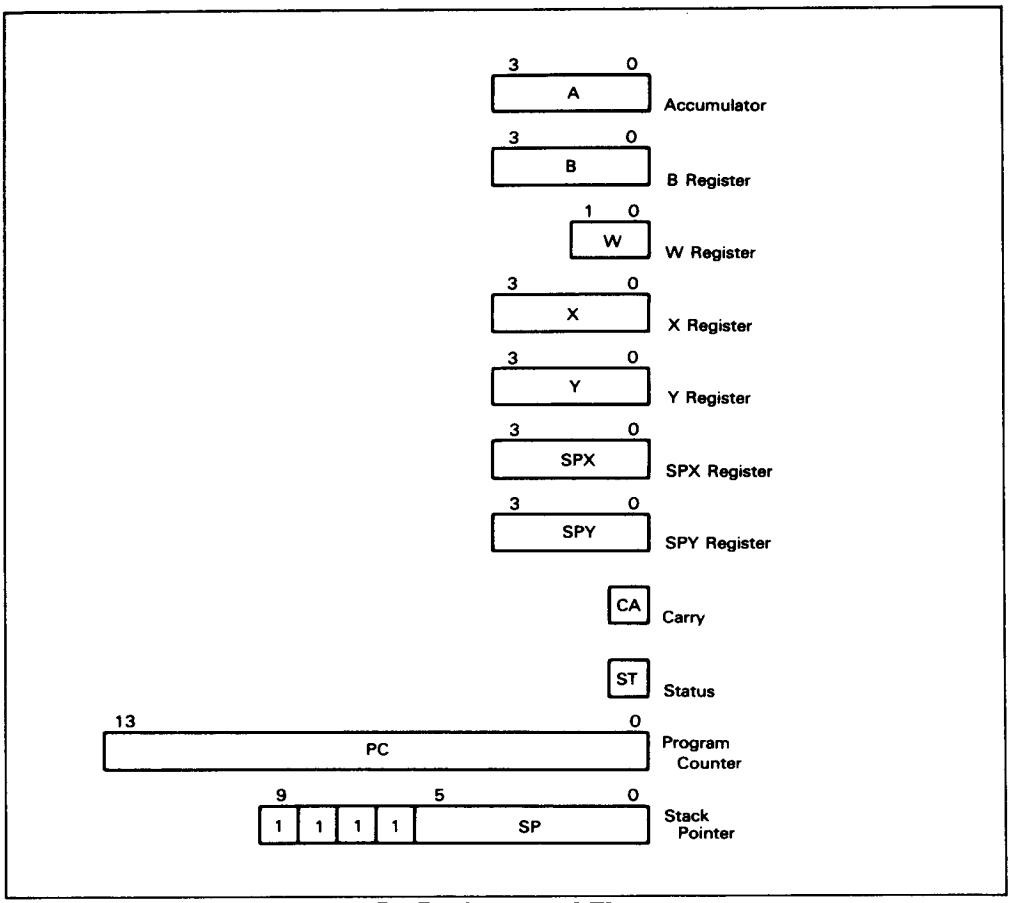


Figure 5. Registers and Flags

Reset

The MCU is reset by setting the RESET pin to high level. At power-on or releasing the system oscillator from stop state, the RESET input must be applied for t_{RC} or for a longer period in order to stabilize the oscillator. In other cases, the RESET input for two instruction cycles resets the MCU. Table 1 lists the initialization values for the registers and counters at the MCU reset.

Interrupt

The MCU has nine interrupt sources; external signals ($\overline{INT_0}$ – $\overline{INT_3}$), timer counter (timer A, timer B, timer C), serial interface, and key scanning. For each interrupt source, an interrupt request flag (IF), an interrupt mask bit (IM) and vector address are provided in order to control the interrupt request. The interrupt enable flag (I/E) allows interrupt service.

Interrupt Control Bits and Interrupt Service: Locations $000 through $003 and $020 through $023 in RAM are reserved for the interrupt control bits. These bits can be accessed by the RAM bit manipulation instructions. The interrupt request flags are set only by signals from interrupt sources. The MCU reset initializes the interrupt enable flag and the interrupt request flags to 0 and the interrupt mask bits to 1. Figure 6 shows the interrupt control circuit block diagram. Table 2 lists interrupt priority and vector addresses for each interrupt source. Table 3 lists the state of the interrupt control bits for interrupt service caused by each interrupt source. An interrupt request occurs when the interrupt request flag is set to 1 and the interrupt mask flag is set to 0. In this case the interrupt enable flag is then set to 1, an interrupt occurs and a vector address corresponding to the interrupt source is then obtained from the PLA.

The sequence and flowchart for interrupt service are shown in figures 7 and 8 respectively. If an interrupt is requested, the current instruction is completed in the first cycle. The interrupt enable flag is then reset in the second cycle. The contents of the carry flag, status flag and program counter are pushed onto the stack in the second and third cycles. In the third cycle the program routine jumps to the appropriate vector address and the interrupt routine is executed. The user must assign each vector address to the JMPL instruction which branches to the starting address of the interrupt routine. In the interrupt routine, the interrupt request flag must be reset by software.

Table 1. Initial Values at the MCU Reset

Registers		Initial value	Description
Program Counter (PC)		$0000	The program is executed from address $0000
Status (ST)		1	The program branches by branch instruction
Stack Pointer (SP)		$3FF	The stack level is set to 0
Interrupt flag/mask	Interrupt enable flag (I/E)	0	Any interrupts are masked
	Interrupt request flag (IF)	0	No interrupt request occurs
	Interrupt mask (IM)	1	Interrupt request is masked
I/O	Port data reg. (PDR) (high voltage pin)	0	Output 0 is enabled
	Port data reg. (PDR) (standard pin)	1	Output 1 is enabled
	Data control reg. (DCR)	0	Output buffer is OFF (in high impedance)
	Port mode reg. A (PMRA)	0000	See port mode register A section
	Port mode reg. B (PMRB)	0000	See port mode register B section
	Interrupt mode reg. (IMR)	0000	See interrupt mode register section
Timer/ serial	Timer mode reg. A (TMA)	0000	See timer mode register A section
	Timer mode reg. B (TMB)	0000	See timer mode register B section
	Timer mode reg. C (TMC)	0000	See timer mode register C section
	Serial mode reg. (SMR)	0000	See serial mode register section
	Prescaler S	$000	—
	Prescaler W	$00	—
	Timer counter A (TCA)	$00	—
	Timer counter B (TCB)	$00	—
	Timer counter C (TCC)	$00	—
	Timer load reg. B (TLR)	$00	—
	Timer load reg. C (TCR)	$00	—
	Octal counter	000	—
VFD	VFD segment reg. (FSR)	0000	See VFD segment register section
	VFD digit reg. (FDR)	0000	See VFD digit register section
	VFD dimmer mode reg. (DMR)	0000	See VFD dimmer mode register section
	VFD control reg. (VCR)	0000	See VFD control register
PWM	PWM data reg. (PWDR3-0)	0000	See PWM data register
Bit register	Low speed ON flag (LSON)	0	See low power dissipation mode section
	Watchdog timer ON flag (WDON)	0	See timer C section
Miscellaneous reg. (MIS)		0000	See miscellaneous register section

The following is the state of other registers and flags at the MCU reset:

Registers	In canceling Stop mode by the MCU reset	In other cases at the MCU reset
Carry (CA) Accumulator (A) B register (B) W register (W) X/SPX register (X/SPX) Y/SPY register (Y/SPY)	The value before the MCU reset may be changed. In this case the MCU must be initialized by software.	The value before the MCU reset may be changed. In this case the MCU must be initialized by software.
Serial data register (SR)	Same as above	Same as above
RAM	The value before the MCU reset (the value before the STOP instruction execution)	Same as above

Table 2. Vector Addresses and Interrupt Priority

Reset and interrupt	Priority	Vector address
Reset		$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
Serial, $\overline{INT_2}$	6	$000C
KEY SCAN, $\overline{INT_3}$	7	$000E

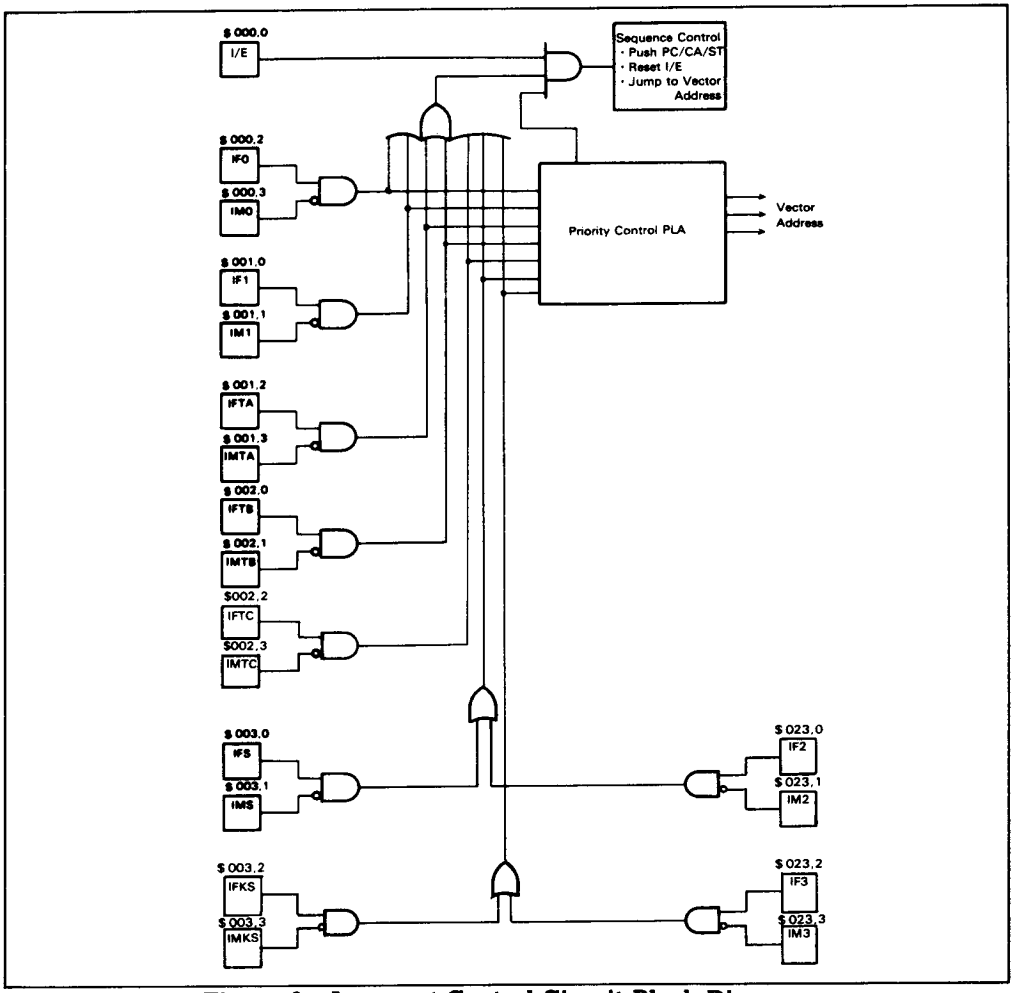


Figure 6. Interrupt Control Circuit Block Diagram

Table 3. Interrupt Service Conditions

	Interrupt Source						
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**Timer A**	**Timer B**	**Timer C**	**Serial, $\overline{INT_2}$**	**Key Scan, $\overline{INT_3}$**
I/E	1	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	*	*	1	0	0
IFS · $\overline{IMS}$ + IF2 · $\overline{IM2}$	*	*	*	*	*	1	0
IFKS · $\overline{IMKS}$ + IF3 · $\overline{IM3}$	*	*	*	*	*	*	1

*: Don't care

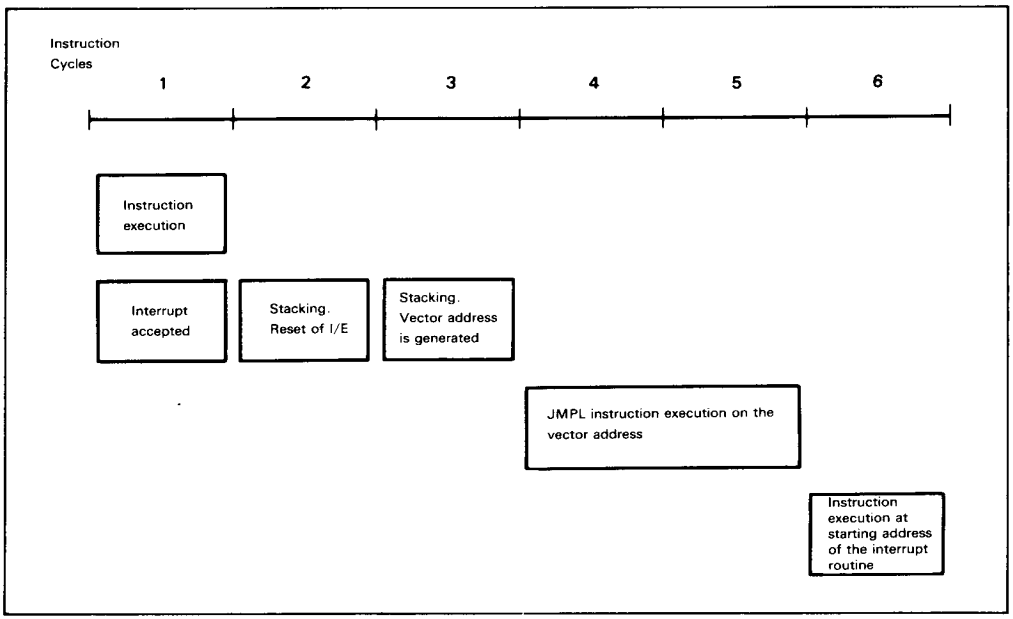


Figure 7. Interrupt Servicing Sequence

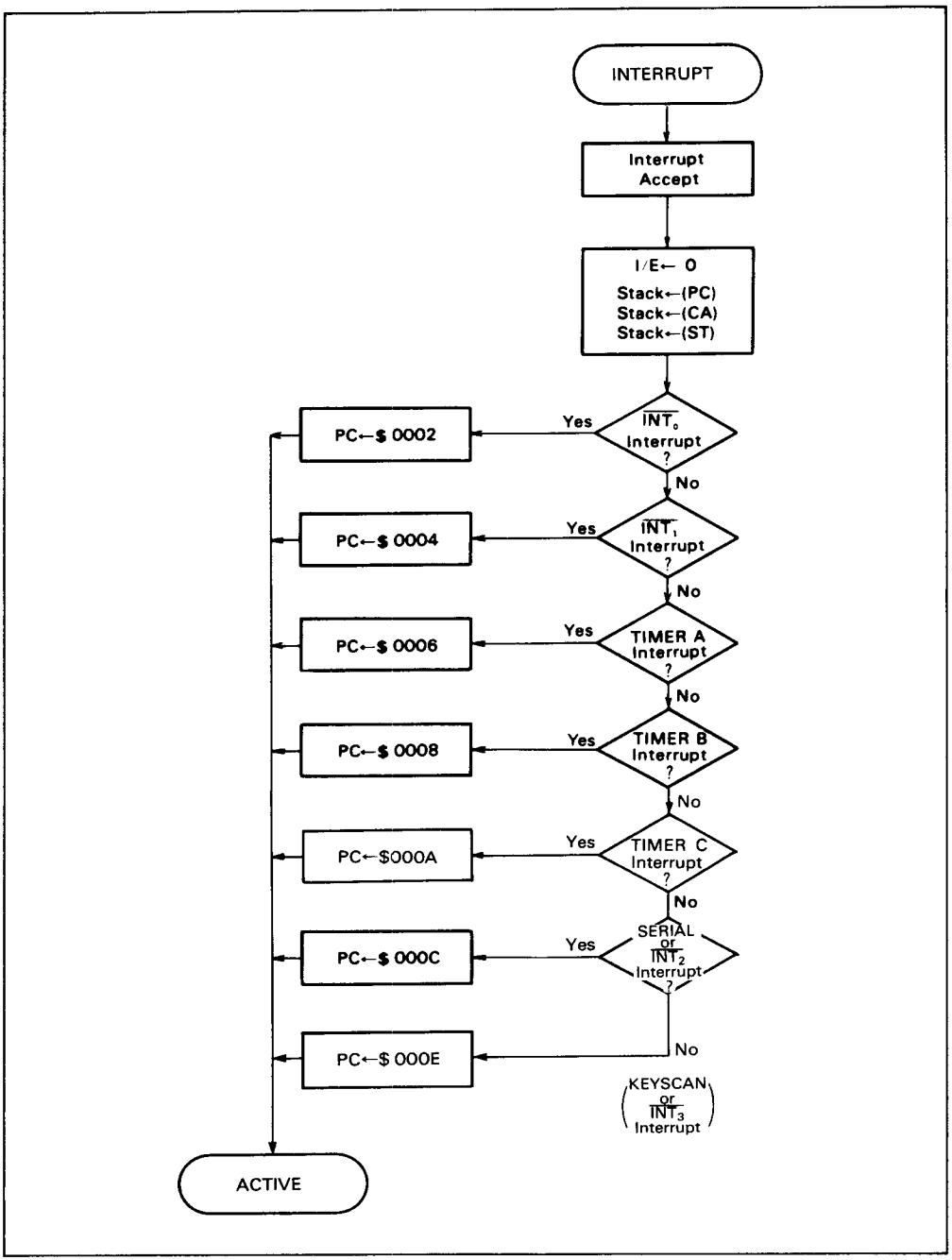


Figure 8. A Flowchart of Interrupt Servicing

Interrupt Enable Flag (I/E: $000, 0): The interrupt enable flag controls all interrupts. This flag is reset by interrupt service and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$ – $\overline{INT_3}$): The external interrupt input is activated by the port mode register (PMRA:$004, PMRB:$005). The external interrupt request flags IF0 and IF1 are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$. IF2 and IF3 are set at the rising and/or falling edge of $\overline{INT_2}$ and $\overline{INT_3}$ respectively. The contents of the interrupt mode register (IMR : $014) specify the active edges. Figure 9 shows the interrupt mode register.

The $\overline{INT_1}$ can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the $\overline{INT_1}$. In this case, the external interrupt mask flag (IM1) must be set so that $\overline{INT_1}$ should not request an interrupt.

External Interrupt Request Flags (IF0: $000, 2, IF1:$001, 0, IF2:$023, 0, IF3:$023, 2): The external interrupt request flags, IF0 through IF3, are set depending on the edge of $\overline{INT_0}$ through $\overline{INT_3}$ respectively.

External Interrupt Mask (IM0:$000, 3, IM1:$001, 1, IM2:$023, 1, IM3:$023, 3): The external interrupt mask bits mask an interrupt request caused by the external interrupt request flags.

Timer A Interrupt Request Flag (IFTA: $001, 2): The timer A interrupt request flag is set when an overflow occurs in timer A.

Timer A Interrupt Mask (IMTA:$001, 3): The timer A interrupt mask bit masks an interrupt request caused by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: $002, 0): The timer B interrupt request flag is set when an overflow occurs in timer B.

Table 4. Interrupt Enable Flag

Interrupt enable flag (I/E)	Interrupt
0	Disable
1	Enable

Table 5. External Interrupt Request Flag

External interrupt request flag (IF0, IF1, IF2, IF3)	Interrupt request
0	Disable
1	Enable

Table 6. External Interrupt Mask Flag

External mask flag (IM0, IM1, IM2, IM3)	Interrupt request
0	Enable
1	Disable (mask)

Table 7. Timer A Interrupt Request Flag

Timer A interrupt request flag (IFTA)	Interrupt requests
0	Disable
1	Enable

Table 8. Timer A Interrupt Mask Flag

Timer A interrupt mask flag (IMTA)	Interrupt request
0	Enable
1	Disable (mask)

Table 9. Timer B Interrupt Request Flag (IFTB)

Timer B interrupt request flag (IFTB)	Interrupt request
0	Disable
1	Enable

Timer B Interrupt Mask (IMTB:$002, 1): The timer B interrupt mask bit masks an interrupt request caused by the timer B interrupt request flag.

Timer C Interrupt Request Flag (IFTC: $002, 2): The timer C interrupt request flag is set when an overflow occurs in timer C.

Timer C Interrupt Mask (IMTC:$002, 3): The timer C interrupt mask bit masks an interrupt request caused by the timer C interrupt request flag.

Serial Interrupt Request Flag (IFS:$003, 0): The serial interrupt request flag is set when the octal counter counts eight transfer clock cycles or when data transfer is halted intermediately and the counter is reset.

Serial Interrupt Mask (IMS:$003, 1): The serial interrupt mask bit masks an interrupt request caused by the serial interrupt request flag.

Key Scan Interrupt Request Flag (IFKS: $003, 2): The key scan interrupt request flag is set when the VFD controller is put in the key scan mode.

Key Scan Interrupt Mask (IMKS:$003, 3): The key scan mask bit masks an interrupt request caused by the key scan interrupt flag.

Table 10. Timer B Interrupt Mask Flag

Timer B interrupt mask flag (IMTB)	Interrupt request
0	Enable
1	Disable (Mask)

Table 11. Timer C Interrupt Request Flag

Timer C interrupt request flag (IFTC)	Interrupt request
0	Disable
1	Enable

Table 12. Timer C Interrupt Mask Flag

Timer C interrupt mask flag (IMTC)	Interrupt request
0	Enable
1	Disable (Mask)

Table 13. Serial Interrupt Request Flag

Serial interrupt request flag (IFS)	Interrupt request
0	Disable
1	Enable

Table 14. Serial Interrupt Mask Flag

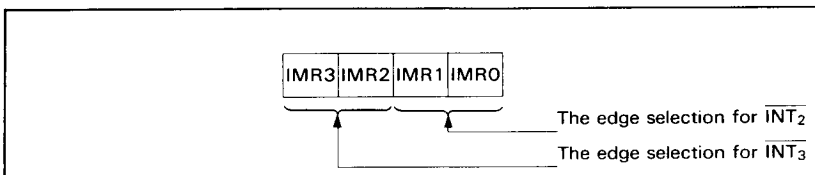
Serial interrupt mask flag (IMS)	Interrupt request
0	Enable
1	Disable (Mask)

Table 15. Key Scan Interrupt Request Flag

Key scan interrupt request flag (IFKS)	Interrupt request
0	Disable
1	Enable

Table 16. Key Scan Interrupt Mask Flag

Key scan interrupt mask flag (IMKS)	Interrupt request
0	Enable
1	Disable (Mask)



IMR

Bit 3	Bit 2	The edge of $\overline{INT_3}$ to be detected
0	0	No detection
	1	the falling edge
1	0	the rising edge
	1	both the rising and falling edge

IMR

Bit 1	Bit 0	The edge of $\overline{INT_2}$ to be detected
0	0	No detection
	1	the falling edge
1	0	the rising edge
	1	both the rising and falling edge

Figure 9. Interrupt Mode Register

Operating Modes

The MCU has two internal oscillation circuits. The oscillation clocks are used in the state shown in figure 10. Five operating modes are available according to how the clock is used.

Tables 17, 18, 19, show low power dissipation modes, the operations of low power dissipation modes, and I/O state in low power dissipation modes, respectively. Figure 10 shows the transition of the MCU operation modes.

Table 17. Low Power Dissipation Modes

		ϕ_{CPU} Note 2	
		Active	**Stop**
ϕ_{PER} Note 1	Active	Active mode (LSON = 0)	Standby mode
	Stop	Sub Active mode Note 3 (LSON = 1)	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)

Notes: 1. ϕ_{PER} : Clock signal for peripheral function except for time base.
2. ϕ_{CPU} : System clock
3. Sub Active mode is an optional mode.

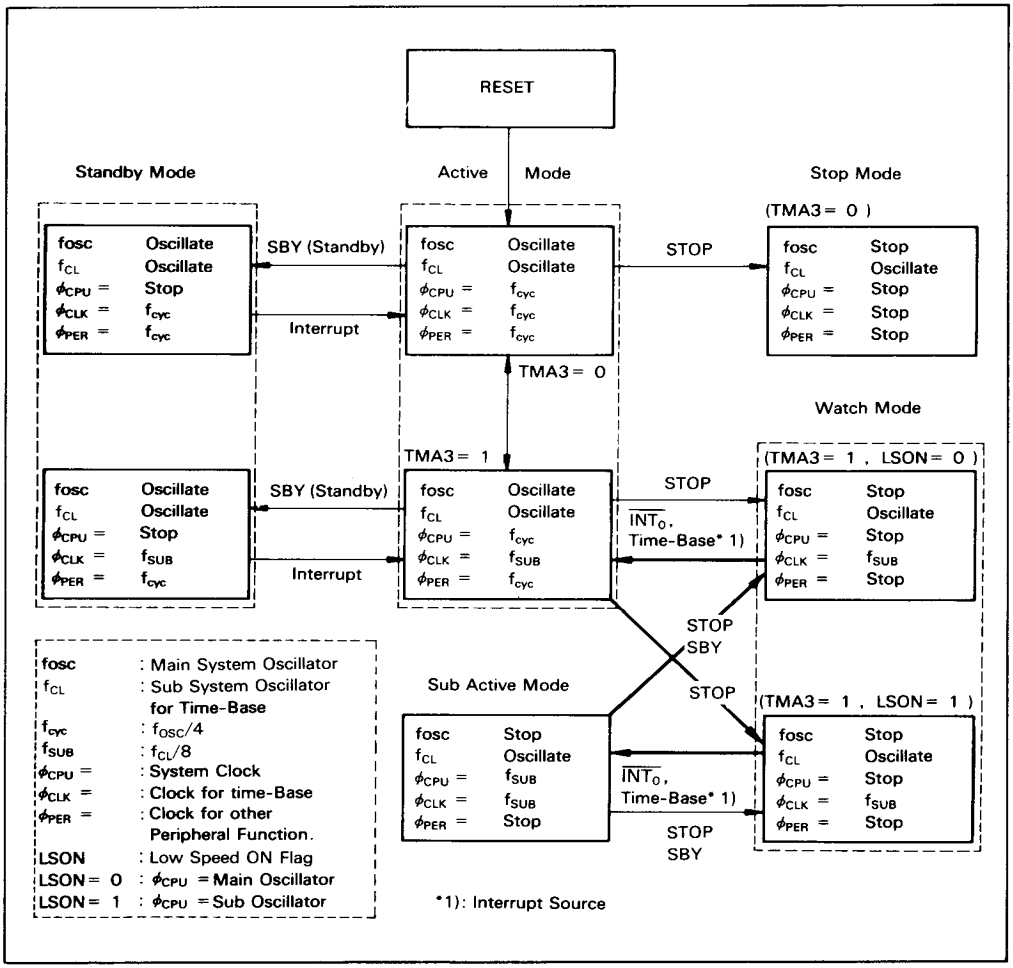


Figure 10. The Transition of the MCU Operation Modes

Table 18. The Operations of Low Power Dissipation Modes

Function		Stop Mode	Watch Mode	Standby Mode	Active Mode	Sub Active Mode[Note 7]
System Oscillator		Stop	Stop			Stop
Subsystem Oscillator		Note 2				
CPU Operation (ϕ_{CLK})	Instruction Execution	Stop	Stop	Stop		
	RAM	Hold	Hold	Hold		
	Registers, Flags	Reset	Hold	Hold		
	I/O[Note 3]	Reset	Hold	Hold		
Peripheral Function, Interrupt (ϕ_{PER})	$\overline{INT_0}$	Reset	Hold			Hold
	$\overline{INT_1}$- $\overline{INT_3}$	Reset	Hold			Hold
	Timer A	Reset	Hold			Hold
	Timer B	Reset	Hold			Hold
	Timer C	Reset	Hold			Hold
	Serial	Reset	Hold			Hold
	VFD	Reset	Hold/ Reset[Note 4]	Note 8		Hold/ Reset[Note 4]
	PWM	Reset	Hold/ Reset[Note 4]			Hold/ Reset[Note 4]
Time-Base Function, Interrupt (ϕ_{PER})	$\overline{INT_0}$	Reset	Note 5	Note 6	Note 6	Note5
	Time-Base	Reset	Note 5	Note 6	Note 6	Note5

Notes: 1. ▨ indicates active.
2. When decreasing I_{CC}, stop oscillation by an external circuit.
3. Refer to Table 19.
4. Only timing generator is reset. The contents of the mode registers are retained.
5. Refer to section interrupt frame.
6. If TMA3 is set to 1, Timer A and $\overline{INT_0}$ are switched to time-base function and interrupt, respectively.
7. Sub Active mode is an optional mode.
8. VFD is active, but it displays nothing because the display data RAM stops working.

Active Mode: In Active mode, the MCU operates based on the clock generated by the system oscillator.

Standby Mode: The SBY instruction causes the MCU to enter Standby mode. In this mode, the oscillator remains active and an interrupt, the timer/counter and serial interface are enabled. The CPU is halted, since the clock which executes instructions has stopped. The state of the the registers, RAM and I/O pins remains unchanged even after the MCU recover from Standby mode.

A RESET input or an interrupt request cancels Standby mode. In the case of the RESET input, the MCU is also reset. When an interrupt is requested, the MCU enters Active mode and an instruction next to the SBY instruction is executed. After this instruction is completed, if the interrupt enable flag is set, an interrupt is serviced; if the flag is reset, the interrupt request is suspended and the program routine is resumed. Figure 11 shows a flowchart of Standby mode.

Stop Mode: When the STOP instruction is executed while TMA3 = 0, the MCU enters Stop mode. In this mode, the system oscillator is halted, and the MCU enters stopped state.

Stop mode is canceled by the RESET input, as shown in figure 12. In this case, the RESET input must be applied for a t_{RC} (stabilization time) (See AC characteristics section.). During Stop mode, the RAM holds its contents before the MCU entered this mode. After canceling Stop mode, the contents of the accumulator, B register, W register, X and SPX registers, Y and SPY registers, carry flag and serial data register can be changed.

Watch Mode: The MCU enters Watch mode by the STOP instruction during Active mode and TMA3 = 1 or by the STOP or SBY instruction during Sub Active mode. Watch mode can be canceled by the RESET input or timer A/$\overline{INT_0}$ interrupt request. For a detailed description of the RESET input in canceling mode, see Stop mode section. If Watch mode is canceled by the timer A/$\overline{INT_0}$ interrupt request, the MCU enters either Active mode or Sub Active mode depending on the state of the LSON bit. When the MCU enters Active mode, the interrupt request is delayed for a half of the interrupt frame period (t_{RC}) in order to wait stabilization of the system oscillation (figure 13). In this case, MCU operation is the same as that when canceling Standby mode (figure 11).

Sub Active mode: When entering Sub Active mode, the MCU operates based on the clock generated by the 32.768 kHz oscillator through CL_1 and CL_2. Table 19 shows MCU operation in Sub Active mode. As Sub Active mode is optional mode, the selection must be made in mask version orders.

Table 19. The State of Input/Output in Low Power Dissipation Modes

	Output		Input
	Standby Mode	**Stop/Watch/ Sub Active Mode**	**All Modes (input state)**
D_0 – D_{15}	Hold/Peripheral function output	High impedance	Input enable
R0 – RA	Hold/Peripheral function output	High impedance	Input enable

Note: Applying V_{CC} – 0.3 to GND + 0.3V to the input state pins generates current between V_{CC} and GND.

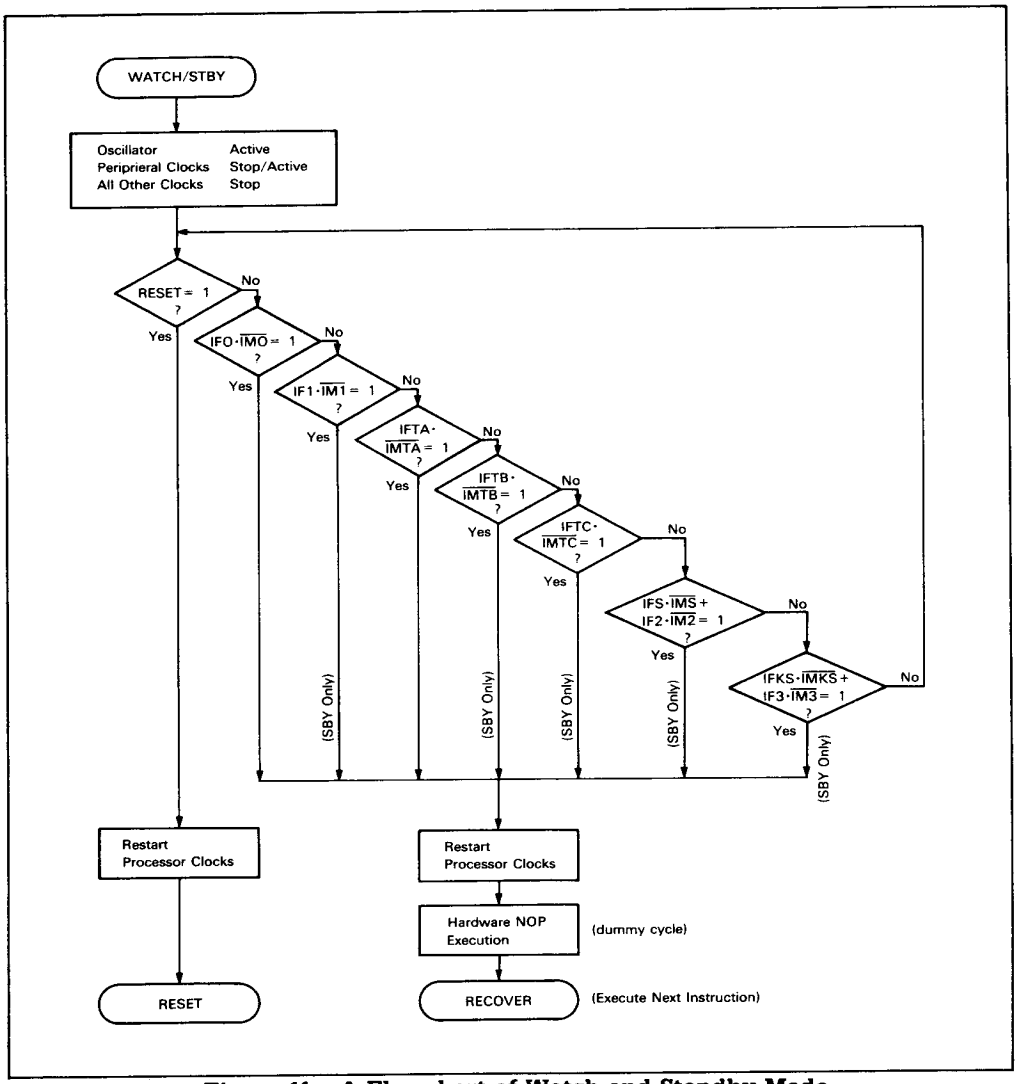


Figure 11. A Flowchart of Watch and Standby Mode

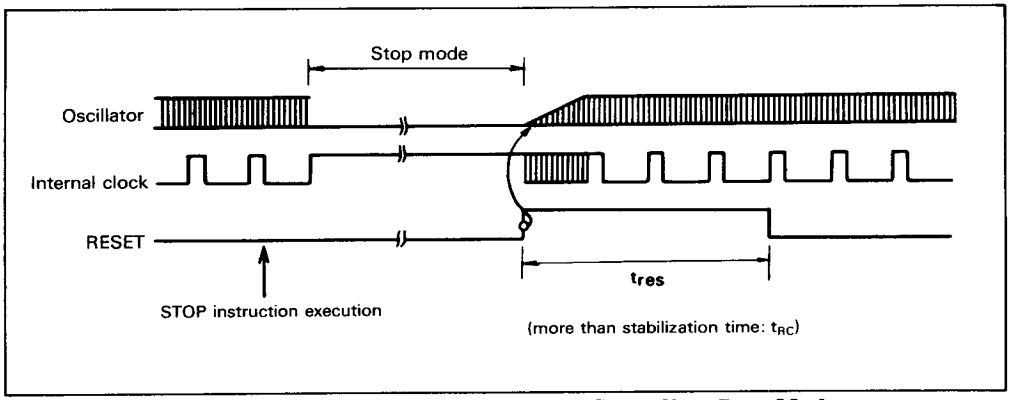


Figure 12. Timing Diagram When Canceling Stop Mode

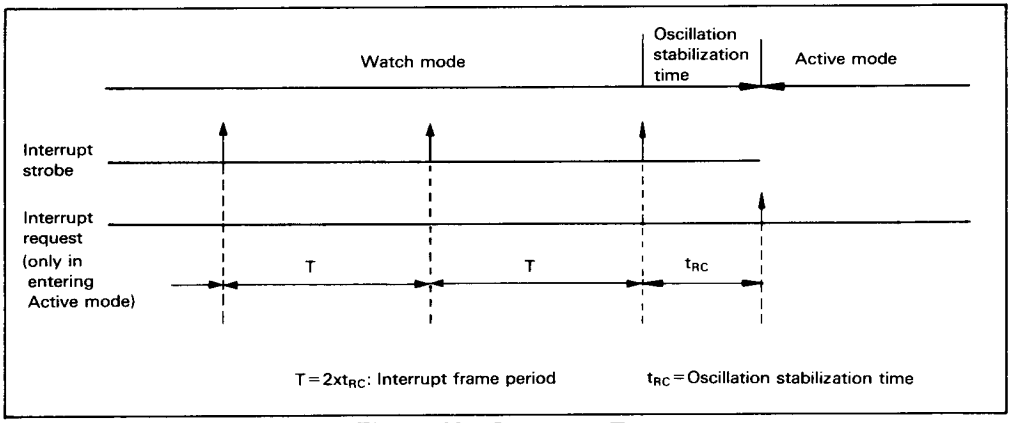
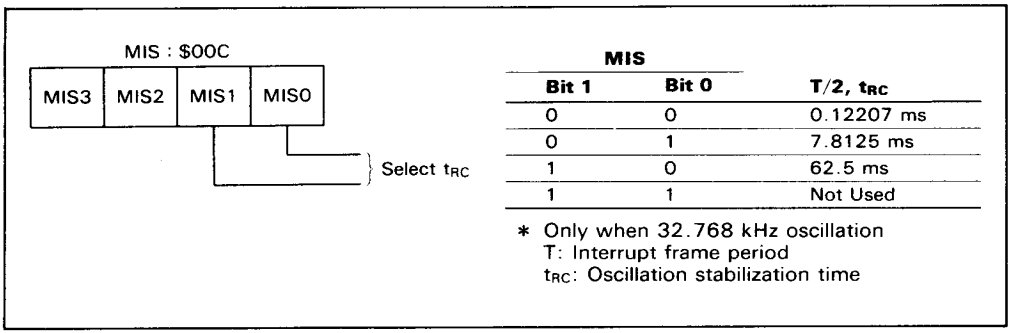


Figure 13. Interrupt Frame



MIS

Bit 1	Bit 0	T/2, t_{RC}
0	0	0.12207 ms
0	1	7.8125 ms
1	0	62.5 ms
1	1	Not Used

* Only when 32.768 kHz oscillation
T: Interrupt frame period
t_{RC}: Oscillation stabilization time

Figure 14. Miscellaneous Register

Interrupt Frame: In Watch mode and Sub Active mode, the time-base clock (ϕ_{CLK}) is applied to timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operates as the time-base and generate the timing clock for the interrupt frame. The interrupt frame period (T) depends on the state of the miscellaneous register as shown in figure 14.
In Watch mode and Sub Active mode, the timer A/$\overline{INT_0}$ interrupt occurs synchronously with the interrupt strobe timing clock. When the MCU wakes up to Active mode from Watch mode, the interrupt request is delayed for a half of interrupt frame period (t_{RC}). The falling edge of $\overline{INT_0}$, which is input regardless of the interrupt frame clock cycle, is equivalent to that synchronous with the interrupt strobe clock just after the falling edge. An overflow and interrupt request in timer A occurs synchronously with the interrupt strobe clock. But, when MCU transfers the watch mode to the active mode through the timer A interrupt, $\overline{INT_0}$ pin has to be high level.

MCU Operation Sequence

Figures 15, 16 and 17 show the MCU operation sequence. The RESET is an asynchronous input, which resets the MCU regardless of the MCU state.

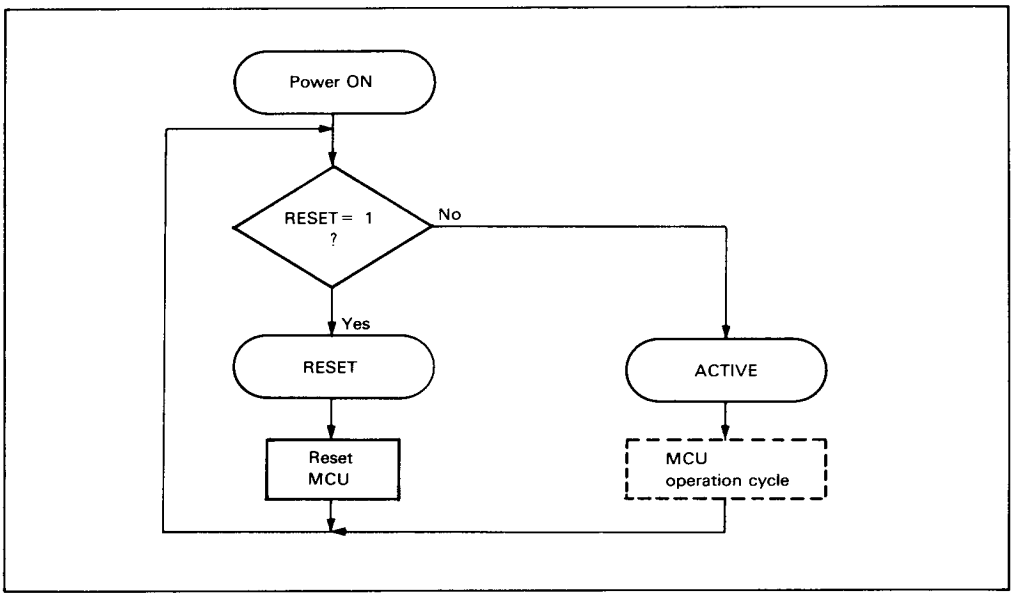


Figure 15. A Flowchart of MCU Operation (1)

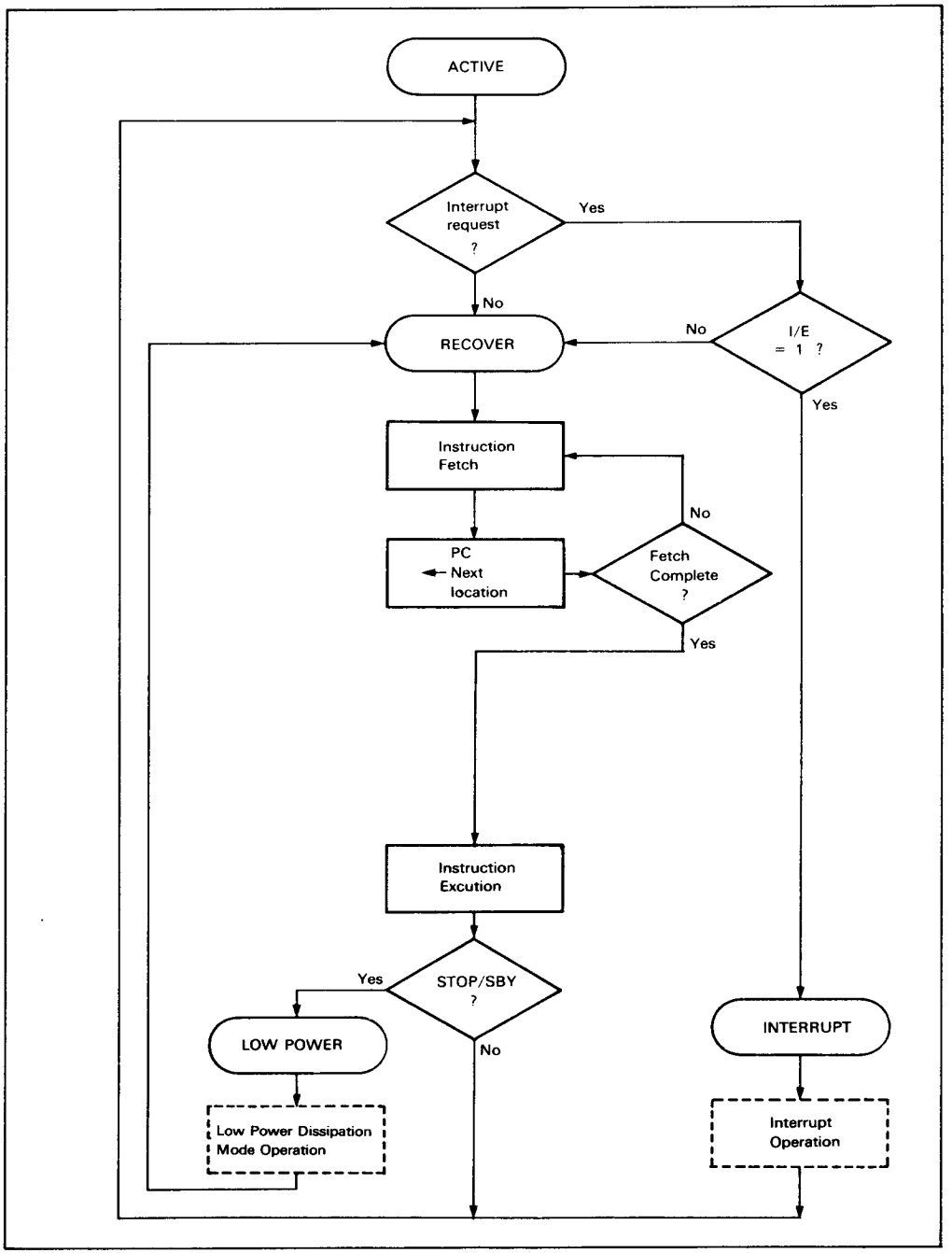


Figure 16. A Flowchart of MCU Operation (2) (MCU operation cycle)

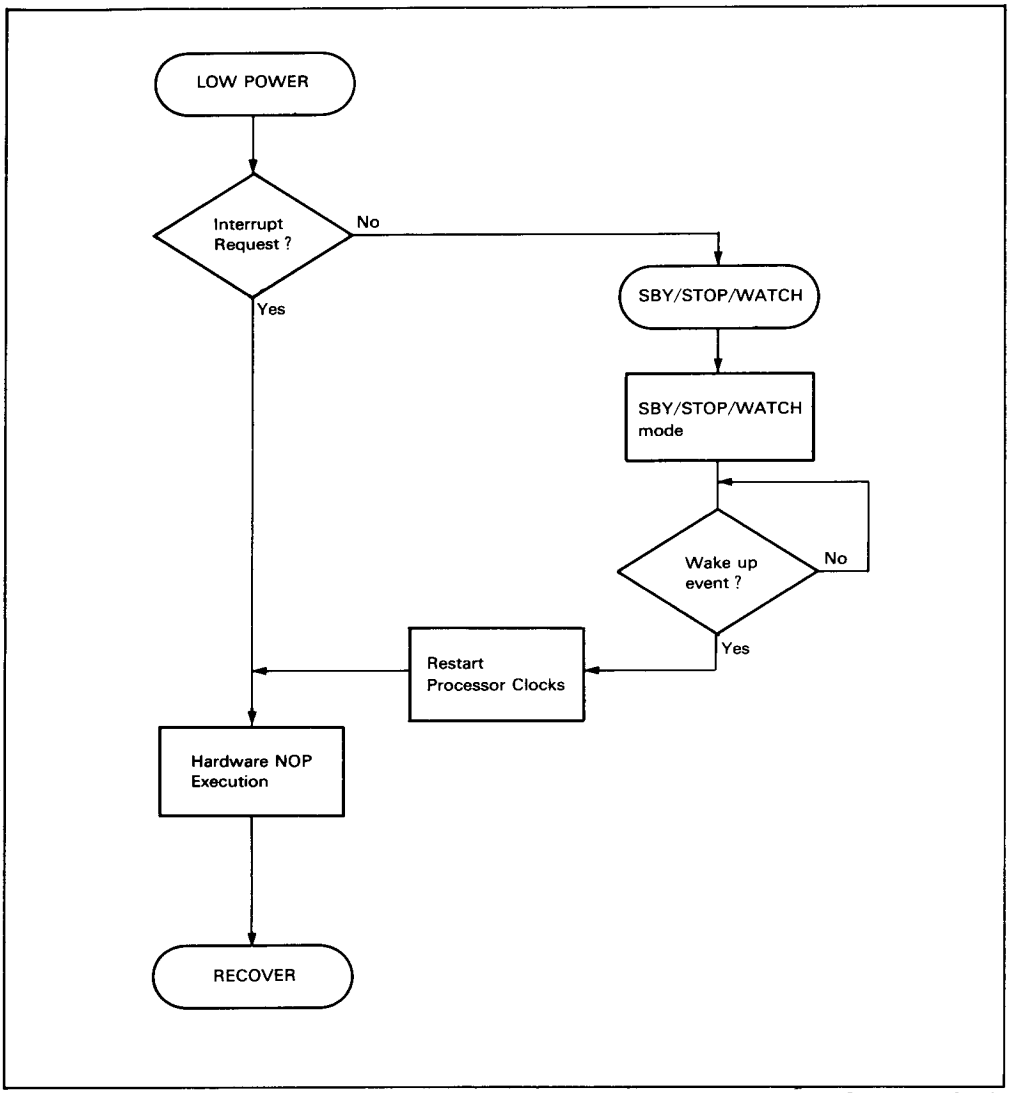


Figure 17. A Flowchart of MCU Operation (Low power dissipation mode operation)

Internal Oscillation Circuit

Figure 18 shows the internal oscillation circuit. The MCU can be connected with the oscillator through OSC_1 and OSC_2, and with the 32.768 kHz crystal oscillator through CL_1 and CL_2.

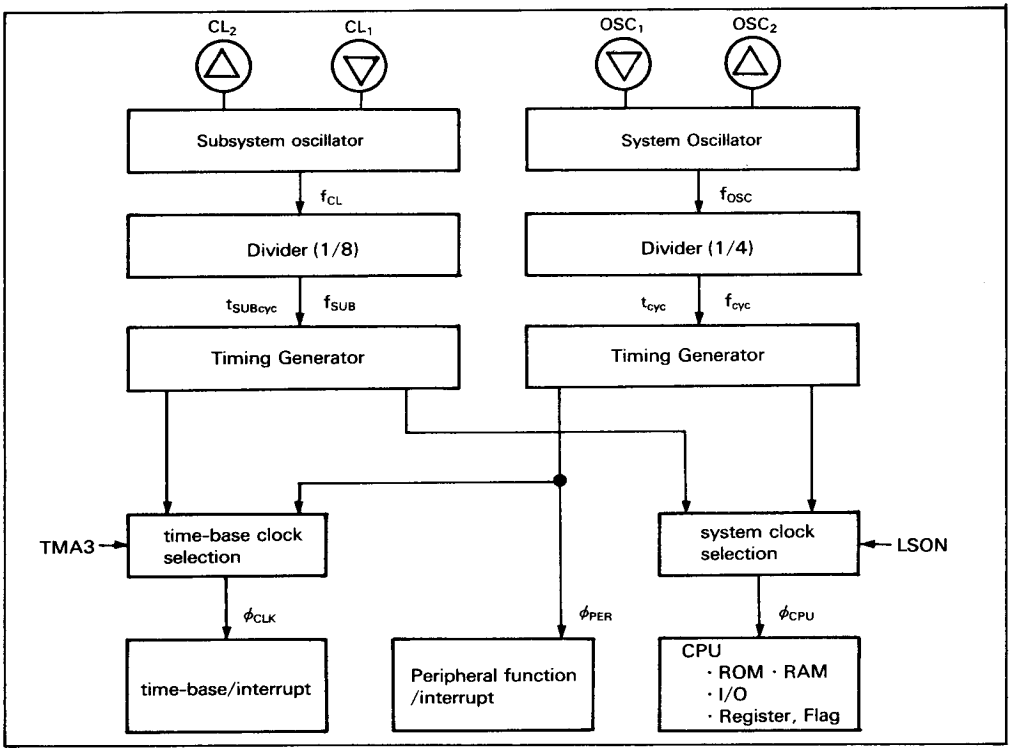


Figure 18. Internal Oscillation Circuit

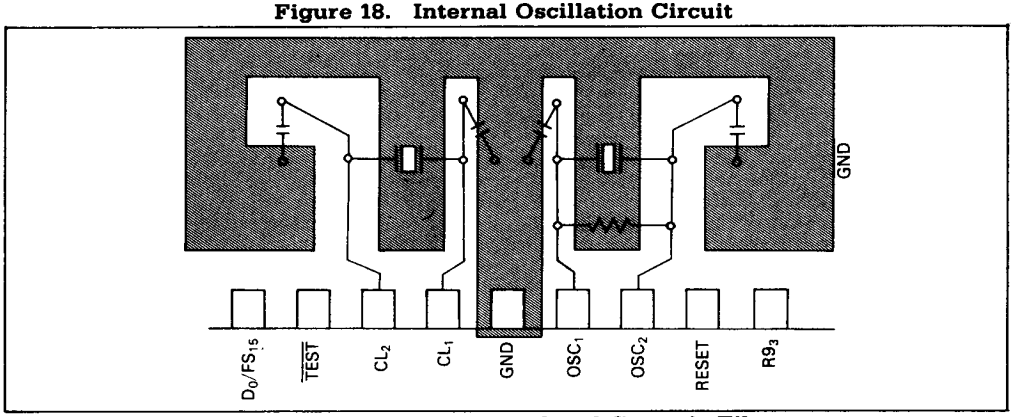
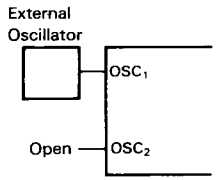
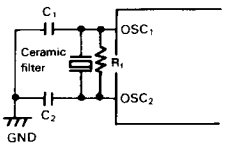
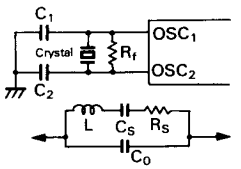
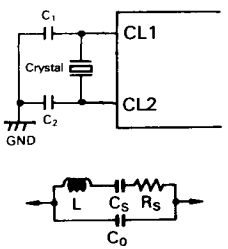


Figure 19. Layout of Crystal and Ceramic Filter

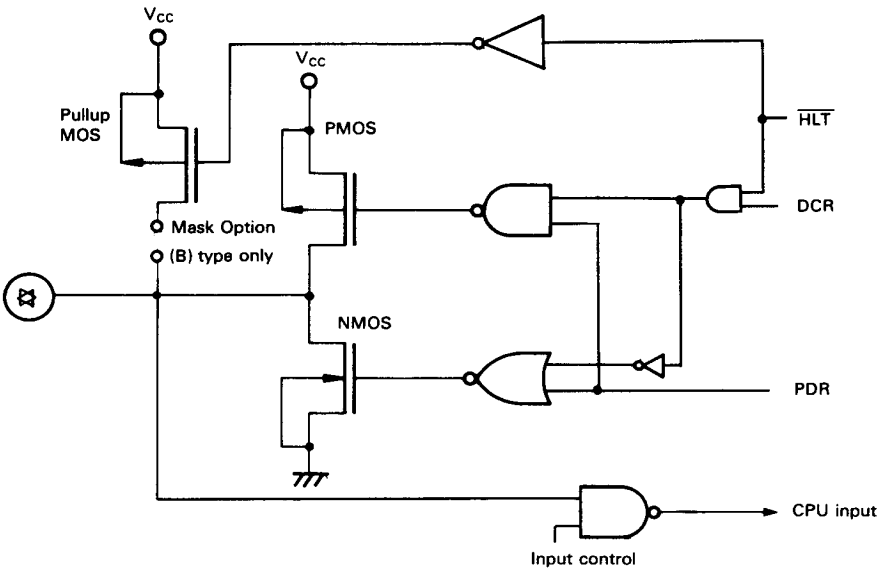
Table 20. Examples of Oscillation Circuit

	Oscillation circuit	Constant
External clock (OSC_1, OSC_2)		
Ceramic filter oscillator (OSC_1, OSC_2)		Ceramic filter: CSA4.00MG (Murata) Rf = 1MΩ ±20%, C_1 = C_2 = 30pF ±20%
Crystal oscillator (OSC_1, OSC_2)		Rf = 1MΩ ±20%, C_1 = C_2 = 10–22pF ±20% Crystal: equivalent to circuit shown below Co = 7pF max. Rs = 100Ω max. f = 1.0 – 4.5 MHz
Crystal oscillator (CL_1, CL_2)		C_1 = C_2 = 15pF ±5% Crystal: MX38T(Nippon Denpa) Co = 1.5pF typ. Rs = 14kΩ typ. f = 32.768 kHz

Notes: 1. Since the circuit constant changes depending on the crystal and ceramic filter resonator and stray capacitance of the board, it is recommended that the user should consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring among OSC_1, OSC_2, CL_1, CL_2 and elements should be as short as possible, and never cross other wiring (see figure 19).
3. If the 32.768 kHz crystal oscillator is not used, CL_1 pin must be fixed to GND and CL_2 must be open.

Input/Output

The MCU has 50 input/output pins and six input pins including 32 high-voltage, high-current pins which are multiplexed with the VFD controller pins. The state of the output buffer of the standard pins depends on a combination of the port data register (PDR) and the data control register (DCR).



Mask option		with Pull-up MOS (B)				without Pull-up MOS (C)			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS	PMOS	–	–	–	ON	–	–	–	ON
buffer	NMOS	–	–	ON	–	–	–	ON	–
Pullup MOS		ON	ON	ON	ON	–	–	–	–

Notes: 1. [–] : OFF
2. For $R4_2$/SO pin, PMOS (A) is OFF when setting bit 2 of the miscellaneous register (MIS2) to 1.

MIS bit 2	$R4_2$/SO pin PMOS
0	ON
1	OFF

Figure 20. Input/Output Buffer

D Ports: The D ports are input/output ports addressed by bit. The SED and SEDD instructions set the ports, and the RED and REDD instructions reset them. The TD and TDD instructions test these pins. Port pins D_0 through D_{15} are multiplexed with the VFD controller pins FS_{15} through FS_0, respectively.

R Rorts: The R ports are ports addressed by 4 bits. The LAR and LBR instructions input data through these ports, and the LRA and LRB instructions output data through the ports. The state of the output buffer of R4 through R8 depends on the data control register (DCR4 to DCR8). $R4_0$, $R4_1$, $R4_2$, $R4_3$, $R6_0$ to $R6_3$, $R7_0$ are multiplexed with $\overline{SCK}$, SI, SO PWM, $\overline{INT_0}$ – $\overline{INT_3}$ and BUZZ, respectively. Table 21 shows the R port circuit types.

Mask Options: The HD4074709 selects a C type circuit (without pullup MOS) or a D type circuit (without pulldown MOS), as shown in table 21. The HD404709/HD404708 can also select the B type circuit (with pullup MOS) or the E type circuit (with pulldown MOS). In this case, however, these MCUs are not compatible with the HD4074709. If the HD404709/HD404708 selects the E type (with pulldown MOS), the source of the pulldown MOS are connected to the Vdisp power supply through the RA_1/Vdisp pin by the mask option.

How to Deal with Unused I/O Pins: The state of unused pins must be fixed to V_{CC} in order to prevent the LSI from malfunctioning due to noise. Note the following cautions before connection. Without pulldown MOS and without pullup MOS are selected for high voltage pins and standard pins, respectively. The contents of PDR and DCR of target pins must be retained as in reset state. The target pins must not be selected as a peripheral function I/O pins.

Table 21. Input/Output Pin Circuit Type

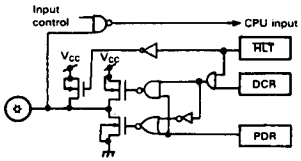
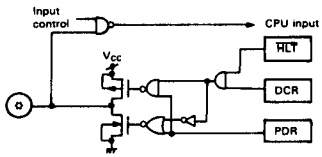
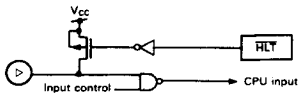
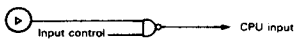
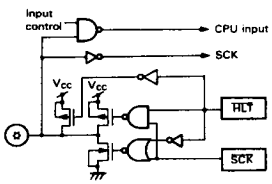
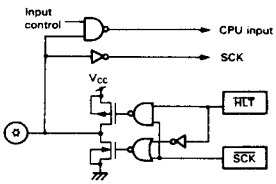
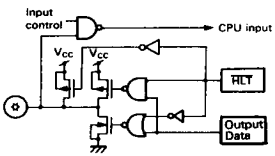
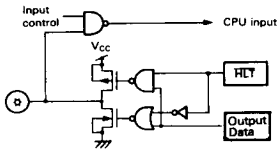
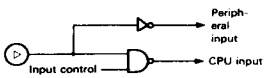
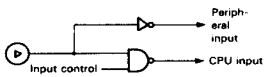
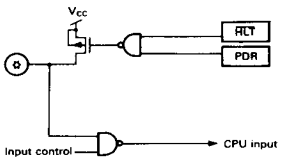
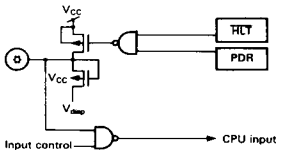
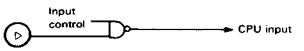
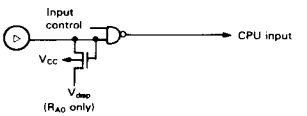
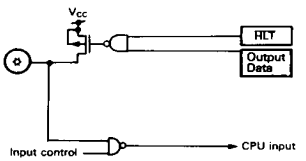
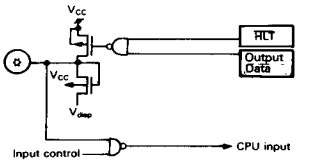
		With pullup MOS (B)	Without pullup MOS (C)	Pin name
Standard pins	I/O pins			$R4_0$ – $R4_3$ $R5_0$ – $R5_3$ $R6_0$ – $R6_3$ $R7_0$ – $R7_3$ $R8_0$ – $R8_1$
	Input pins			$R9_0$ – $R9_3$
	Peripheral I/O Pins			$\overline{SCK}$ (output) Note 1
	Peripheral output Pins			SO PWM BUZZ
	Peripheral input Pins			$\overline{SCK}$ (input) Note 1 SI $\overline{INT_0}$ $\overline{INT_1}$ $\overline{INT_2}$ $\overline{INT_3}$

Table 21. Input/Output Pin Circuit Type (Continued)

		Without pulldown MOS (D)	With pulldown MOS (E)	Pin name
High-voltage pin	I/O pins			D_0 – D_{15} RO_0 – RO_3 $R1_0$ – $R1_3$ $R2_0$ – $R2_3$ $R3_0$ – $R3_3$
	Input Pins			RA_0 – RA_1
	Peripheral output pins			FS_0 – FS_{15} FD_0 – FD_{15}

Notes: 1. If the external clock is selected to the MCU as the clock source for the serial interface, $\overline{SCK}$ is used as an input pin.
2. In Stop mode the MCU is internally reset and the selected peripheral function is canceled. The HLT signal goes to 1 and the I/O pins are put in high impedance.
3. In Watch/Sub Active mode the HLT signal is 1 and the output pins are put in high impedance. During these modes the pins selected to peripheral input or input/output must be fixed to input level, otherwise the current through V_{CC} and GND is generated.
4. The mask option of the circuit type is shown in the following. The mask ROM type MCU is compatible with the ZTAT type only when the mask ROM type selects the C and D circuit type.

Circuit type / Product type	B	C	D	E
Mask ROM type (HD404709 HD404708)	option			
ZTAT type (HD4074709)		fixed		

MIS (Miscellaneous Reg.) ADR=$00C

MIS3	MIS2	MIS1	MIS0

- MIS2 → $R4_2$ /SO pin PMOS mode selection
- MIS0 → $R7_0$ /BUZZ pin mode selection

SMR (Serial Mode Reg.) ADR=$005

SMR3	SMR2	SMR1	SMR0

- SMR0 → $R4_0$ /$\overline{SCK}$ pin mode selection

PMRA (Port Mode Reg. A) ADR=$004

PMRA3	PMRA2	PMRA1	PMRA0

- PMRA0 → $R4_2$ /SO pin mode selection
- PMRA1 → $R4_1$ /SI pin mode selection
- PMRA2 → $R6_0$ /$\overline{INT_0}$ pin mode selection
- PMRA3 → $R6_1$ /$\overline{INT_1}$ pin mode selection

PMRB (Port Mode Reg. B) ADR=$015

X	PMRB2	PMRB1	PMRB0

- PMRB0 → $R6_2$ /$\overline{INT_2}$ pin mode selection
- PMRB1 → $R6_3$ /$\overline{INT_3}$ pin mode selection
- PMRB2 → $R4_3$ /PWM pin mode selection

SMR bit 3	Port Select
0	$R4_0$
1	$\overline{SCK}$

MIS bit 3	Port Select
0	$R7_0$
1	BUZZ

PMRA bit 3	Port Select	PMRA bit 2	Port Select	PMRA bit 1	Port Select	PMRA bit 0	Port Select
0	$R6_1$	0	$R6_0$	0	$R4_1$	0	$R4_2$
1	$\overline{INT_1}$	1	$\overline{INT_0}$	1	SI	1	SO

PMRB bit 2	Port Select	PMRB bit 1	Port Select	PMRB bit 0	Port Select
0	$R4_3$	0	$R6_3$	0	$R6_2$
1	PWM	1	$\overline{INT_3}$	1	$\overline{INT_2}$

Figure 21. Pin Mode Selection Registers

Timer

The MCU contains two prescalers (prescaler W and prescaler S) and three timer/counters (timer A, timer B, timer C). Figures 22 and 23 show the block diagrams of the timers. The function of the timers depend on the state of the bits as shown in table 22.

Prescaler S: Prescaler S is driven by the system clock. This prescaler, after being initialized to $000 by the MCU reset, divides the system clock frequency. During Watch mode and Sub Active mode, dividing operation stops and count value is retained. When the mode is canceled, dividing operation restarts. From among the prescaler outputs the input clock of the timer and the transfer clock of serial interface are specified by timer mode registers (TMA, TMB, TMC) and serial mode register (SMR) respecitively.

Prescaler W: Prescaler W is driven by the CL1 input clock divided by 8. This prescaler, after being initialized to $00 by the MCU reset, divides the input clock frequency. The input clock of the timer A may be specified from among prescaler W outputs, depending on the state of timer mode register A. In this case, prescaler W and timer A can be reset by software.

Table 22. Selecting Functions of Timers A/B/C

Timer A Condition	Function
TMA3 = 0	system clock base interval timer
TMA3 = 1	time-base for watch

Timer B Condition	Function
TMB2 – 0 ≠ 111	automatic reloading timer
TMB2 – 0 = 111 PMRA3 = 1	event counter (using $R6_1/\overline{INT_1}$)

Timer C Condition	Function
WDON = 0 (MIS3 = 1)	automatic reloading timer (square wave output circuit using $R7_0$/BUZZ)
WDON = 1	watchdog timer

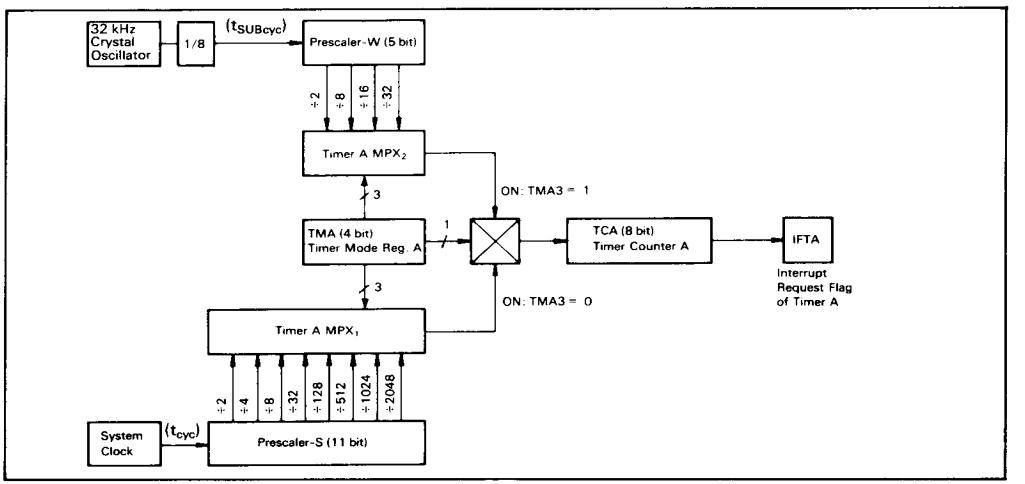


Figure 22. Timer A Block Diagram

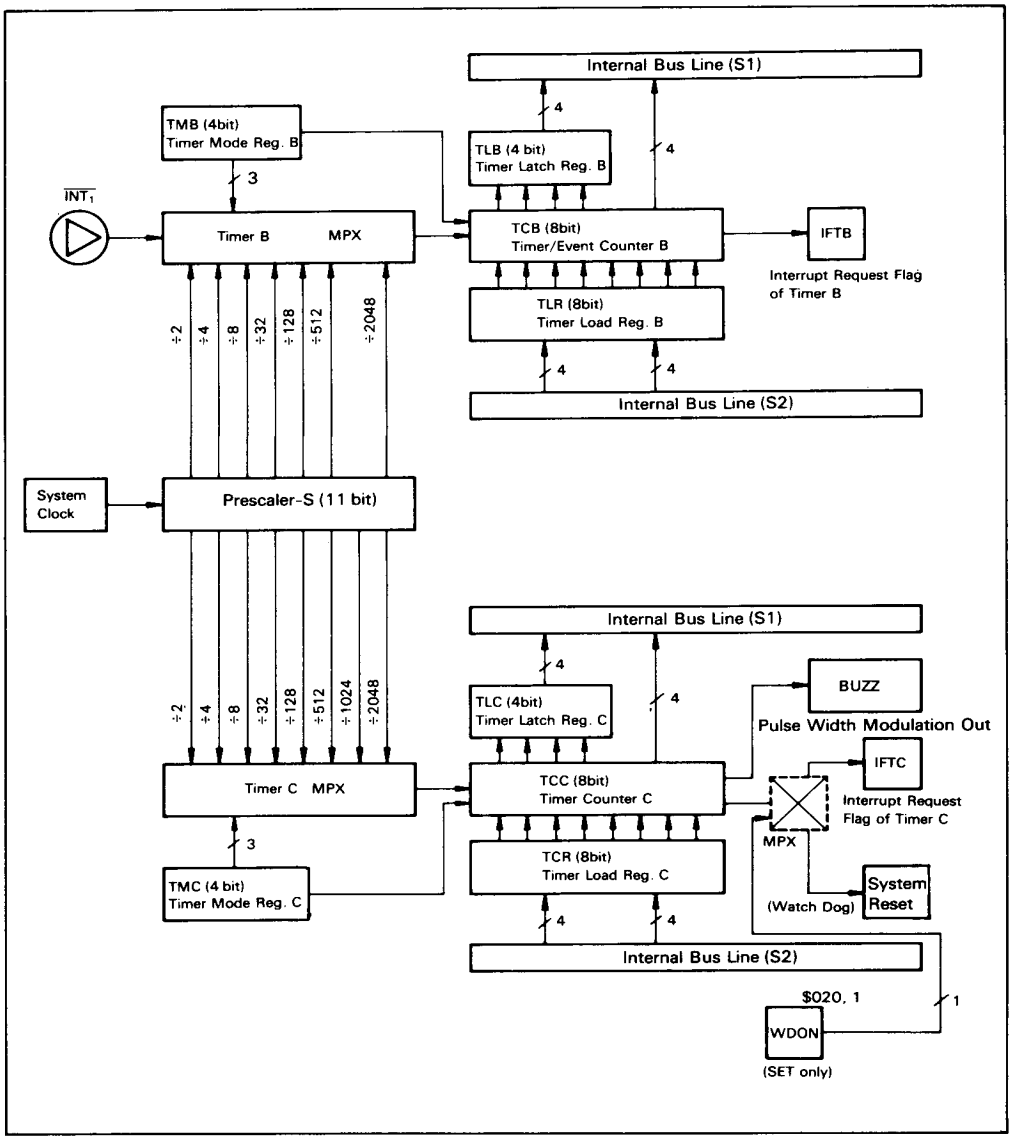


Figure 23. Timer B/Timer C Block Diagram

Timer A Operation: Timer A is initialized to $00, and then counts up at every input clock. If an input clock is applied to timer A after the timer is $FF, an overflow occurs and timer A is set to $00. The overflow causes timer A interrupt request flag (IFTA: $001, 2) to go to 1, and the timer continues to count up from $00. Timer A is an interval timer in which an overflow occurs every 256 clock inputs.

Timer A can also be used as the watch time base when the TMA3 bit of timer mode register A is set to 1. The timer is driven by the 32.768 kHz oscillator clock frequency divided by prescaler W. In this case, prescaler W and timer A can be initialized by software. The input clock of timer A is controlled by timer mode register A.

Timer B Operation: Automatic reloading, input clock source and prescaler dividing ratio of timer B depend on the state of timer mode register B. When using the external event input as the input clock source of timer B, the $R6_1/\overline{INT_1}$ pin must be defined as $\overline{INT_1}$, by the port mode register (PMRA: $004) and an interrupt must be masked by the external interrupt mask bit (IM1).

Timer B is initialized to the value set in timer load register by software, and is then incremented by one every clock input. If an input clock is applied to timer B after the timer is $FF, an overflow occurs. In this case, if automatic reloading is enabled, timer B is initialized to the initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, 0).

Timer C Operation: The automatic reloading, and the prescaler dividing ratio of timer C depend on the state of timer mode register C. Timer C is initialized to the value set in the timer load register by software, and is then incremented by one every clock input. If an input clock is applied to timer C after the timer is $FF, an overflow occurs. In this case, if automatic reloading is enabled, timer C is initialized to the initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, 2).

Timer C also functions as a watchdog timer. When the program routine goes out of control and an overflow occurs while the WDON flag is set, the MCU is reset. Moreover, timer C provides a variable-duty pulse output (BUZZ). The output waveform depends on the state of timer mode register C and timer load register, as shown in figure 24. During the pulse output, the $R7_0$/BUZZ pin must be defined as BUZZ by the miscellaneous register.

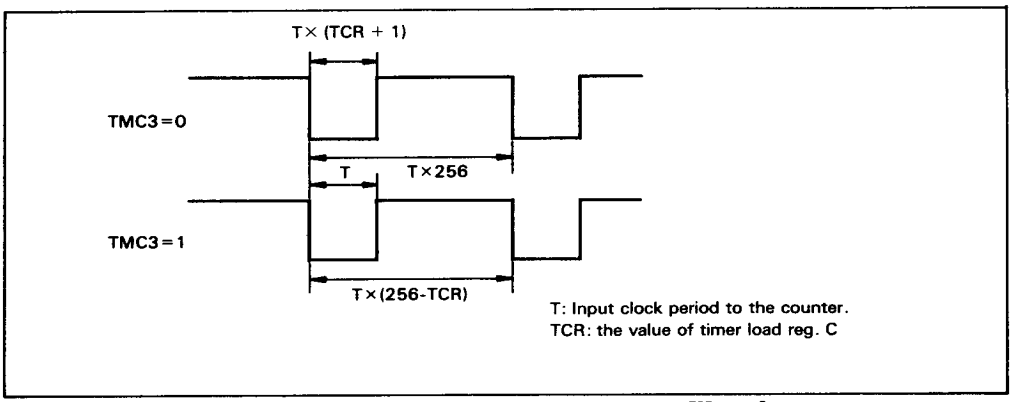
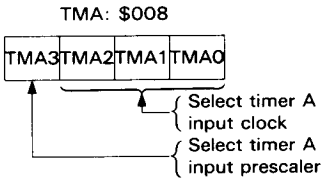


Figure 24. Variable-duty Pulse Output Waveform

Timer Mode Register A (TMA: $008): Timer mode register A is a 4-bit write-only register which controls timer A as shown in figure 25. This register is initialized to $0 by the MCU reset.

Timer Mode Register B (TMB: $009): Timer mode register B is a 4-bit write-only register which determines whether or not the MCU provides automatic reloading and selects the input clock and the prescaler dividing ratio. This register is initialized to $0 by the MCU reset. The contents of the register can be changed at the second instruction cycle following write instruction execution. Timer B must be programmed not to be initialized by the write instruction to timer load register until the timer mode is enabled.

Timer Mode Register C (TMC: $00D): Timer mode register C is a 4-bit write-only register which determines whether or not the MCU provides the automatic reloading and selects the prescaler dividing ratio. This register is initialized to $0 by the MCU reset. The contents of the register can be changed at the second instruction cycle after write instruction execution. Timer C must be programmed so as not to be initialized by the write instruction to timer load register until the timer mode is enabled.



TMA3	TMA2	TMA1	TMA0	Source prescaler, input Clock period, operation mode	
0	0	0	0	PSS, 2048 t_{cyc}	
			1	PSS, 1024 t_{cyc}	Timer A
		1	0	PSS, 512 t_{cyc}	mode
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	
			1	PSW, 16 t_{SUBcyc}	Time
		1	0	PSW, 8 t_{SUBcyc}	base
			1	PSW, 2 t_{SUBcyc}	mode
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

* t_{SUBcyc}=244.14μs (when using 32.768 kHz crystal oscillator)
* t_{cyc}=0.9536μs (when using 4.1943 MHz crystal oscillator with divide-by-4)
* Timer counter overflow output period (s) = Input clock period (S) x 256

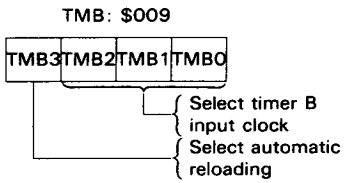
Figure 25. Timer Mode Register A

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A TLRU: $00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low digit (TCBL: $00A, TLRL: $00A) and a high digit (TCBU: $00B, TLRU: $00B).

The timer/event counter is initialized by writing data to the timer load register. In this case, the user must write data to the lower digit first. The timer/event counter is initialized to the value set in the timer load register with a write cycle of the higher digit. The timer load register is initialized to $00 by the MCU reset.

Timer B count value is obtained by reading the timer/event counter. In this case, the user must read the higher digit first. The count value is latched at the time when the higher digit is read.

Timer C (TCCL: $00E, TCCU: $00F, TCRL: $00E, TCRU: $00F): Timer C consists of an 8-bit write-only timer load register and an 8-bit read-only timer/counter. Each of them has a lower digit (TCCL: $00E, TCRL: $00E) and a higher digit (TCCU: $00F, TCRU: $00F). Timer C operation is the same as that for timer B.

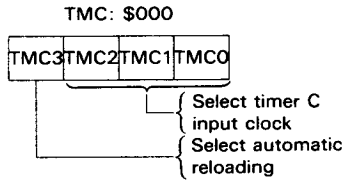


TMB 3	automatic reloading
0	disabled
1	enabled

TMB 2	TMB 1	TMB 0	Input clock period and input clock source
0	0	0	2048 t_{cyc}
0	0	1	512 t_{cyc}
0	1	0	128 t_{cyc}
0	1	1	32 t_{cyc}
1	0	0	8 t_{cyc}
1	0	1	4 t_{cyc}
1	1	0	2 t_{cyc}
1	1	1	$\overline{INT_1}$ (external event input)

t_{cyc}=0.9536μs (when using 4.1943MHz crystal oscillator with divide-by-4)

Figure 26. Timer Mode Register B



TMC 3	automatic reloading
0	disabled
1	enabled

TMC 2	TMC 1	TMC 0	Input clock period
0	0	0	2048 t_{cyc}
0	0	1	1024 t_{cyc}
0	1	0	512 t_{cyc}
0	1	1	128 t_{cyc}
1	0	0	32 t_{cyc}
1	0	1	8 t_{cyc}
1	1	0	4 t_{cyc}
1	1	1	2 t_{cyc}

t_{cyc}=0.9536μs (when using 4.1943MHz crystal oscillator with divide-by-4)

Figure 27. Timer Mode Register C

Serial Interface

The serial interface transmits/receives 8-bit serial data. It consists of the serial data register, the serial mode register, the port mode register A, the octal counter and the multiplexer (figure 28). The $R4_0/\overline{SCK}$ pin and the transfer clock signal are controlled by writing data to the serial mode register. The serial data register can by read and written by software. The contents of this register can be shifted synchronously with the transfer clock signal.

The serial interface is activated by the STS instruction. The octal counter, which is initialized to $0 by the STS instruction, starts to count at the falling edge of the transfer clock signal ($\overline{SCK}$) and is incremented by one at the rising edge of the clock signal. When the counter is reset after eight clock signals are input or when data transmission is discontinued, the serial interrupt request flag is set.

Table 23. Serial Interface Operation Modes

SMR 3	PMR 1	PMR 0	Serial interface operation modes
1	0	0	Clock Continuous Output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/Receive mode

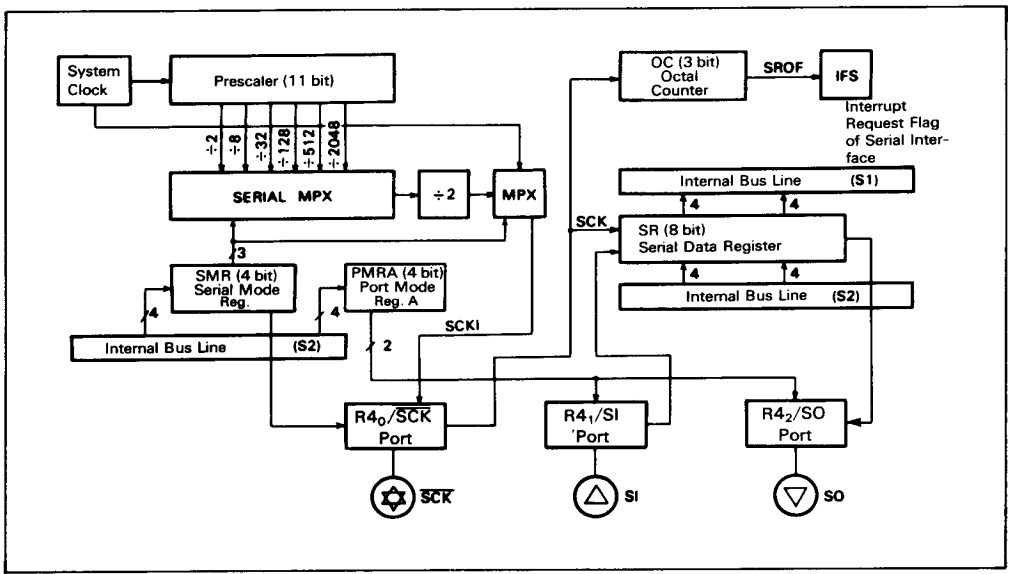
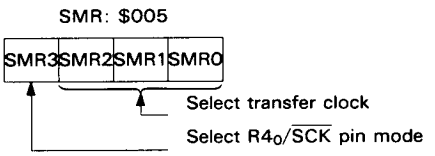


Figure 28. Serial Interface Block Diagram

Serial Mode Register (SMR: $005): The serial mode register is a 4-bit write-only register which controls the $R4_0/\overline{SCK}$ pin and the transfer clock signal. When data is written to this register, the serial interface is internally initialized. Write signal to the serial mode register discontinues the transfer clock to the serial data register and octal counter, resets the counter to $0, and sets the serial interrupt request flag if previous value of octal counter was not $0 (figure 29).

The contents of the serial mode register is not valid until the second instruction cycle after the write instruction execution. The user must program the STS instruction to be executed after this instruction cycle. The serial mode register is initialized to $0 by the MCU reset.



SMR3	$R4_0/\overline{SCK}$
0	Used as $R4_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

					Transfer Clock	
SMR2	SMR1	SMR0	$R4_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	Transfer Clock Period
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	4096 t_{cyc}
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	1024 t_{cyc}
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	256 t_{cyc}
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	16 t_{cyc}
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	4 t_{cyc}
1	1	0	$\overline{SCK}$ Output	System clock		1 t_{cyc}
1	1	1	$\overline{SCK}$ Input	External clock		

t_{cyc} = 0.9536μs (when using 4.1943MHz crystal oscillator with divide-by-4)

Figure 29. Serial Mode Register

Serial Data Register (SRL: $006, SRU: $007): The serial data register is an 8-bit read/write register which consists of a lower digit (SRL: $006) and a higher digit (SRU: $007). The data in this register is output from the least significant bit (LSB) through the SO pin synchronously with the falling edge of the transfer clock. External data is then written to the register from the LSB through the SI pin synchronously with the rising edge of the tranfer clock. Figure 30 shows the timing chart for the transfer clock and data input/output clock.

The serial data register must not be read or written until the data transmission is completed. If the register is read or written during the data transmission, the data may be changed.

Serial Interface Operation Modes: Table 23 lists the serial interface operation modes. The user must specify the state of the port mode register and serial mode register as listed in the table. In changing the operation modes, the serial interface must be internally initialized by writing data to the serial mode register.

The State of Serial Interface: The serial interface is provided with three different states as shown in figure 31. In STS waiting state, the serial interface is internally initialized. In this case, even the transfer clock input does not enable the serial interface. When the STS instruction is executed during this state, the serial interface system enters SCK waiting state. If the transfer clock is applied to the MCU during this state, the interface system enters transfer state, which enables the octal counter and the serial data register. In this case, if the system is in the clock continuous output mode, the system remains in SCK waiting state and the transfer clock is continuously output.

If eigth transfer clock cycles are applied to the MCU or the STS instruction is executed during the clock transfer state, the octal counter is reset to 000 and the interface system enters the SCK waiting state. When the system is changed from the transfer state to another state, the counter is reset to 000, which sets the serial interrupt request flag.

When the internal transfer clock is used, the STS instruction triggers the transfer clock output. The clock output is stopped after eight clock cycles. When data is written to the port mode register during the SCK waiting state or transfer state, the serial interface must be internally initialized by writing data to the serial mode register. After performing a write to the serial mode register, the serial interface system is put in the STS waiting state.

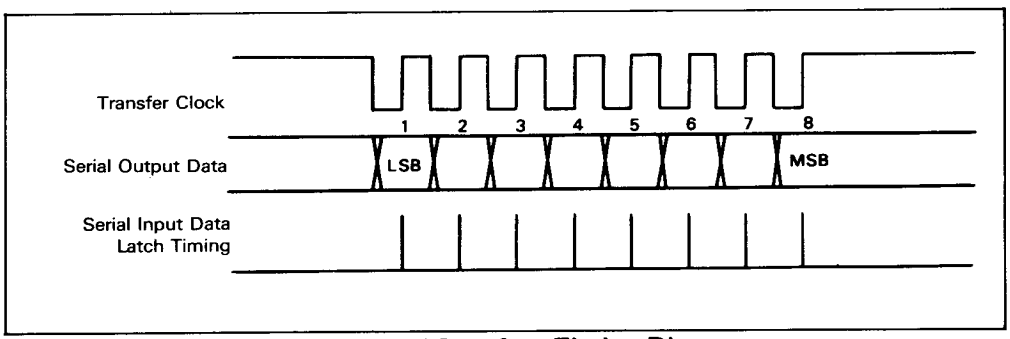


Figure 30. Serial Interface Timing Diagram

Example of Transfer Clock Error Detection: The serial interface system malfunctions when an external noise pulse is superimposed over the transfer clock pulse. Such errors can be detected through the procedure shown figure 32.

For example, if, after eight clock cycles, the transfer clock continues to be applied to the MCU during transfer clock wait state, the state of the serial interface system is changed to transfer state. This state remains unchanged for next eight clock cycles, and the system is then changed to SCK waiting state again. The serial interrupt request flag must be reset before entering the serial interface system into the STS waiting state by writing data to the serial mode register. This procedure sets the interrupt request flag again.

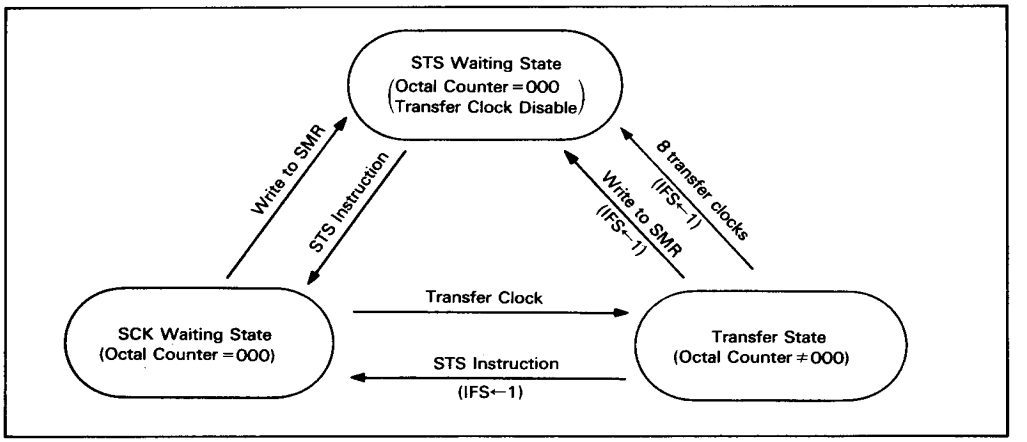


Figure 31. Serial Interface Operation State

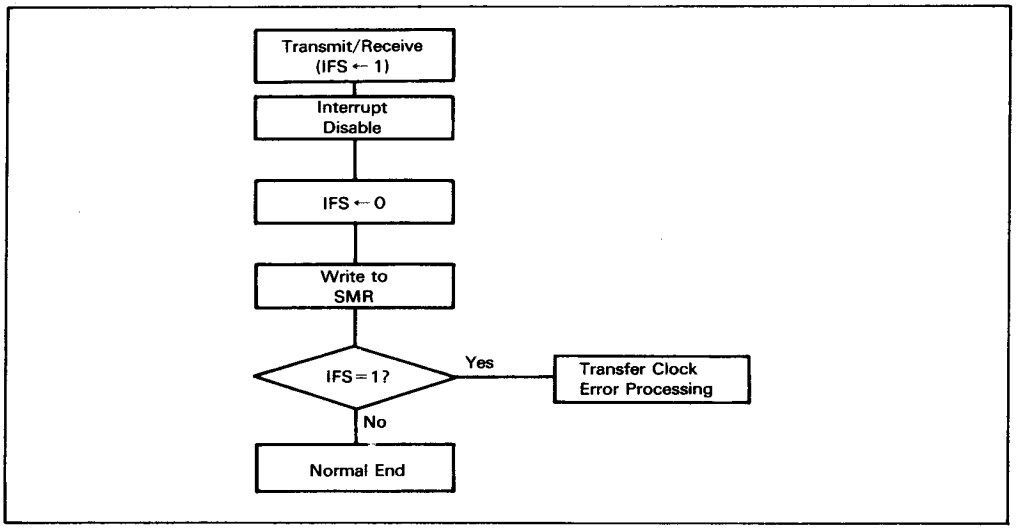


Figure 32. Example of Transfer Clock Error Detection

VFD (Vacuum Fluorescent Display) Controller

The MCU has a controller which controls up to 16 digit pins and 16 segment pins and a high-voltage, high current driver, which enables easy VFD display operation. The controller part consists of the VFD data RAM, the VFD control register (VCR), the dimmer mode register (DMR) and the display timing generator. The driver part consists of 32 high-voltage, high current pins, the VFD segment register (FSR) and the VFD digit register (FDR), which specifies the display format from 8 segments × 2 digits up to 16 segments × 16 digits.

One display frame is divided into 17 periods. 16 periods are used for VFD, and 1 period is used for key scanning. When key scanning is enabled, the CPU can control all the segment/digit pins as D port/R port.

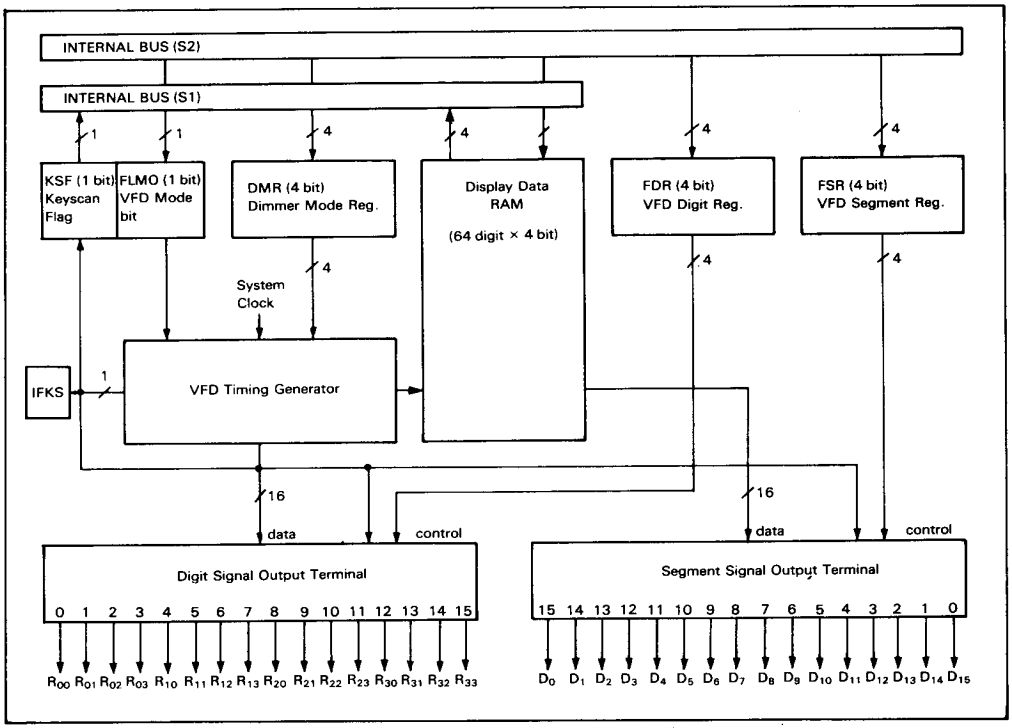


Figure 33. VFD Controller Block Diagram

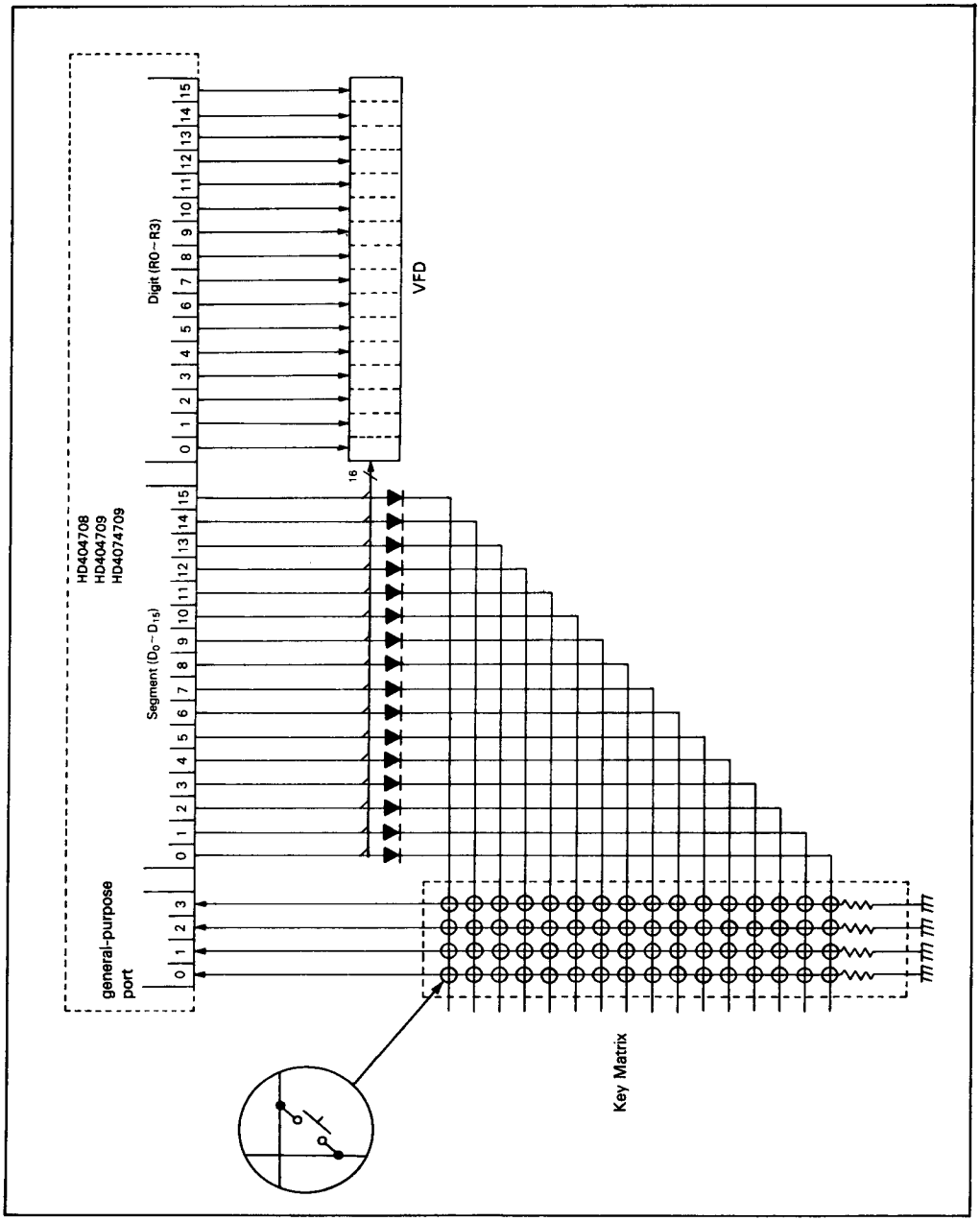


Figure 34. Example of Connection with the VFD

VFD Data RAM: Table 24 lists the addresses of the VFD data RAM. The RAM area unused in the display mode can be assigned for general purpose.

Table 24. The VFD Data RAM Addresses

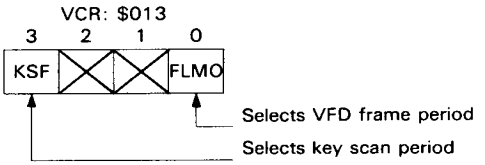
Pin	Segment / Digit	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO_0	0	$090				$080				$070				$060			
RO_1	1	$091				$081				$071				$061			
RO_2	2	$092				$082				$072				$062			
RO_3	3	$093				$083				$073				$063			
$R1_0$	4	$094				$084				$074				$064			
$R1_1$	5	$095				$085				$075				$065			
$R1_2$	6	$096				$086				$076				$066			
$R1_3$	7	$097				$087				$077				$067			
$R2_0$	8	$098				$088				$078				$068			
$R2_1$	9	$099				$089				$079				$069			
$R2_2$	10	$09A				$08A				$07A				$06A			
$R2_3$	11	$09B				$08B				$07B				$06B			
$R3_0$	12	$09C				$08C				$07C				$06C			
$R3_1$	13	$09D				$08D				$07D				$06D			
$R3_2$	14	$09E				$08E				$07E				$06E			
$R3_3$	15	$09F				$08F				$07F				$06F			

Notes: 1. In each segment, the right end corresponds to the LSB and the left end to the MSB.
2. The halftone indicates the VFD data RAM location used in displaying 8-segment x 12-digit data. In this example, other locations can be used for general purpose.
3. The contents of RAM addresses $07C – $07F and $06C – $06F (not display data) are output from segment pins at the timing of digit 12 – 15.

VFD Control Register (VCR: $013): The VFD control register consists of a write-only bit and a read/test-only bit.

The VFD mode bit (FLMO: $013, 0) is a write-only bit which selects a frame period of either 3264 or 6528 instruction cycles. This bit is initialized to 0 by the MCU reset.

The key scan flag (KSF: $013, 3) is a read/test-only flag. This flag indicates either the display period or the key scan period. The key scan period is one-seventeenth of the frame period. During the key scan period, the D port and R0 through R3 port pins are controlled by the CPU for general purpose. When using these pins, key scanning can be enabled by software. At the rising edge of the key scan flag the key scan interrupt request flag is set to 1.



VCR

bit 3	Period
0	display period
1	key scan period

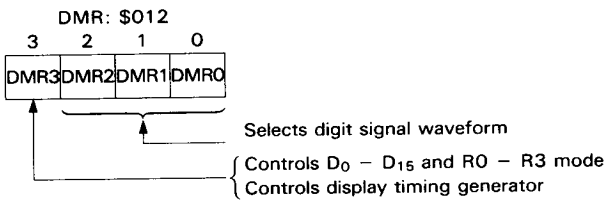
VCR

bit 0	T frame: frame period		T digit: key scan/digit period		T dimmer: dimmer resolution	
1	3264 t_{cyc}	3113 μs*	192 t_{cyc}	183.1 μs*	12 t_{cyc}	11.44 μs*
0	6528 t_{cyc}	6226 μs*	384 t_{cyc}	366.2 μs*	24 t_{cyc}	22.89 μs*

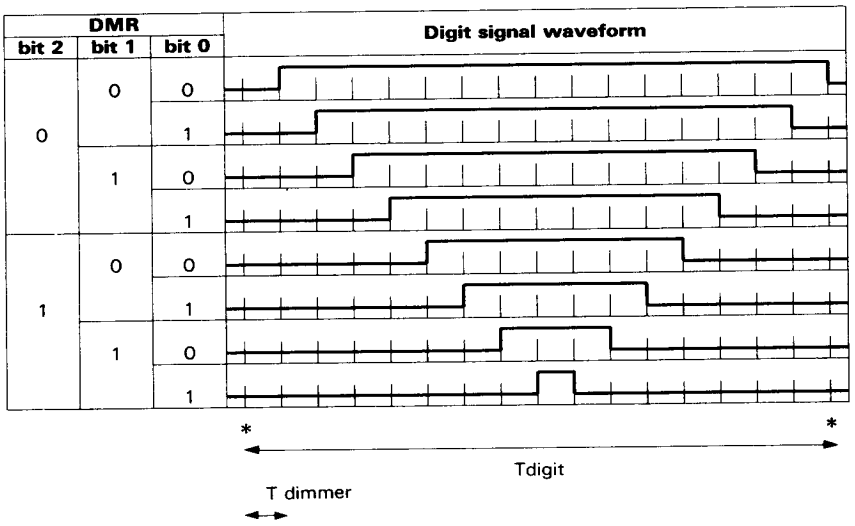
* t_{cyc} = 0.9536 μs (when using fosc = 4.1943MHz crystal oscillator with divide-by-4)

Figure 35. VFD Control Register

Dimmer Mode Register (DMR: $012): The dimmer mode register is a 4-bit write-only register which controls the VFD driver pin mode and the digit signal output waveform. The register can specify the waveform from among eight types as shown in figure 36. The dimmer mode register is initialized to $0 by the MCU reset. When specifying the waveform, the user must take into consideration the waveform resolution. For detailed description of the resolution, see the VFD control register section. DMR3 is used as a master bit for the VFD controller. During DMR3 is 0, D_0 – D_{15} and R0 – R3 function as general purpose ports, and the display timing generator is in reset state.



DCR bit 3	D_0 – D_{15} and R0 – R3 mode
0	Used as general purpose ports
1	Used as VFD driver depending on the state of FDR and FSR



Note: indicates a timing of segment signal. For Tdigit and Tdimmer, see VFD control register section.

Figure 36. Dimmer Mode Register

VFD Digit Register (FDR: $011), VFD Segment Register (FSR: $010): The VFD digit register and the VFD segment register are 4-bit write-only registers which control the VFD driver pins. The pins selected by the these registers are used for the VFD driver or general purpose, depending on the state of bit 3 of the dimmer mode register and the key scan flag. All other pins are used for general purpose. These registers are initialized to $0 by the MCU reset.

FDR: $011

FDR3	FDR2	FDR1	FDR0

Select the number of VFD digit pins

FSR: $010

FSR3	FSR2	FSR1	FSR0

Select the number of VFD segment pins

FDR 3 2 1 0	The number of digit	Digit signal output pins
0 0 0 0	0	none
0 0 0 1	2	FD_0/RO_0 – FD_1/RO_1
0 0 1 0	3	FD_0/RO_0 – FD_2/RO_2
0 0 1 1	4	FD_0/RO_0 – FD_3/RO_3
0 1 0 0	5	FD_0/RO_0 – $FD_4/R1_0$
0 1 0 1	6	FD_0/RO_0 – $FD_5/R1_1$
0 1 1 0	7	FD_0/RO_0 – $FD_6/R1_2$
0 1 1 1	8	FD_0/RO_0 – $FD_7/R1_3$
1 0 0 0	9	FD_0/RO_0 – $FD_8/R2_0$
1 0 0 1	10	FD_0/RO_0 – $FD_9/R2_1$
1 0 1 0	11	FD_0/RO_0 – $FD_{10}/R2_2$
1 0 1 1	12	FD_0/RO_0 – $FD_{11}/R2_3$
1 1 0 0	13	FD_0/RO_0 – $FD_{12}/R3_0$
1 1 0 1	14	FD_0/RO_0 – $FD_{13}/R3_1$
1 1 1 0	15	FD_0/RO_0 – $FD_{14}/R3_2$
1 1 1 1	16	FD_0/RO_0 – $FD_{15}/R3_3$

FSR 3 2 1 0	The number of segment	Segment signal output pins
0 0 0 0	0	none
0 0 0 1	8	FS_0/D_{15} – FS_7/D_8
0 0 1 0	9	FS_0/D_{15} – FS_8/D_7
0 0 1 1	10	FS_0/D_{15} – FS_9/D_6
0 1 0 0	11	FS_0/D_{15} – FS_{10}/D_5
0 1 0 1	12	FS_0/D_{15} – FS_{11}/D_4
0 1 1 0	13	FS_0/D_{15} – FS_{12}/D_3
0 1 1 1	14	FS_0/D_{15} – FS_{13}/D_2
1 0 0 0	15	FS_0/D_{15} – FS_{14}/D_1
1 0 0 1	16	FS_0/D_{15} – FS_{15}/D_0
1 0 1 0	Not used	
1 0 1 1		
1 1 0 0		
1 1 0 1		
1 1 1 0		
1 1 1 1		

Figure 37. VFD Digit Register and Segment Register

PWM (Pulse Width Modulation) D/A Converter

The PWM D/A converter is used to generate DC voltage which controls the VTR tuner using the voltage synthesizer method. This converter provides 14-bit pulse-divided PWM (Pulse Width Modulation) which realizes high resolution and high speed response.

The D/A converter consists of four registers and a pulse width modulator. When data is written to the PWM data register 3, the data is latched into the modulator and the PWM data is then output synchronously with the internal clock signal. It should be noted that bits 2 and 3 of PWM data register 3 are invalid. Figure 39 shows the flowchart of PWM D/A converter operation.

Data Register Name and Address	Bit Number	READ/WRITE
PWM data register PWDR 3 ($019)	2	W
PWM data register PWDR 2 ($018)	4	W
PWM data register PWDR 1 ($017)	4	W
PWM data register PWDR 0 ($016)	4	W

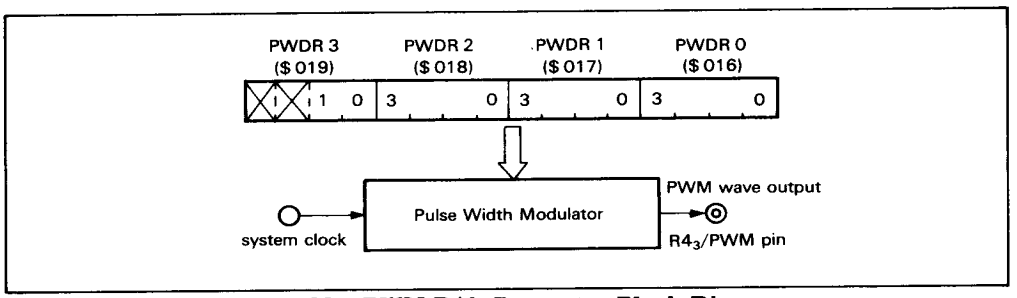


Figure 38. PWM D/A Converter Block Diagram

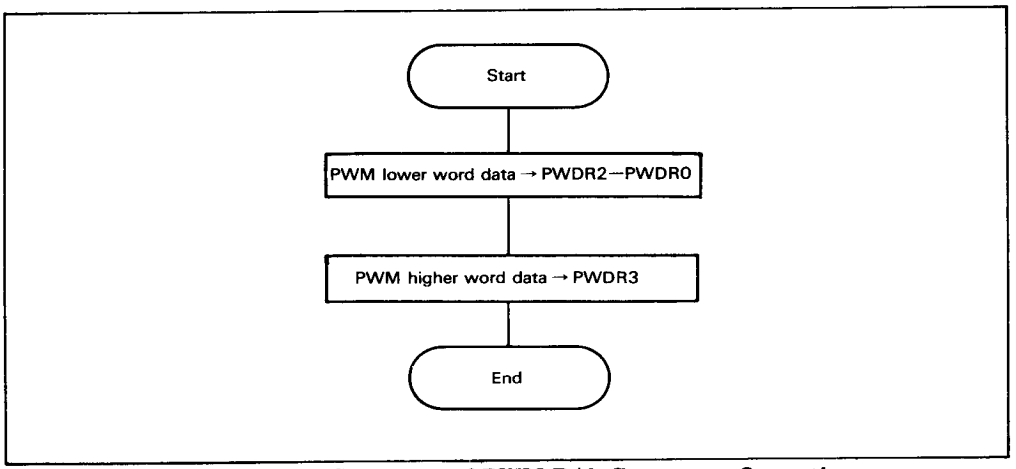


Figure 39. A Sequence of PWM D/A Converter Operation

PWM Registers

PWM data register 0 (PWDR0: $016)

a 4-bit write-only data register

3			0
DA3	DA2	DA1	DA0

PWM data register 1 (PWDR1: $017)

a 4-bit write-only data register

3			0
DA7	DA6	DA5	DA4

PWM data register 2 (PWDR2: $018)

a 4-bit write-only data register

3			0
DA11	DA10	DA9	DA8

PWM data register 3 (PWDR3: $019)

a 2-bit write-only data register

		1	0
		DA13	DA12

PWM Operation

Figure 40 shows the PWM waveform. One frame period has 64 clock pulses. The relationship between total pulse width at low level in one frame and the data value is represented by the following equation; in the equation, t_{cyc} indicates the instruction cycle time.

$$T_L = (\text{PWDR value} + 64) \times \frac{t_{cyc}}{2}$$

1 frame period = 8192 t_{cyc}
t_{fn} = 128 t_{cyc}

$$\text{resolution} = \frac{t_{cyc}}{2}$$

t_{cyc} = 0.9536 μs (when using 4.1943 MHz crystal oscillator with divide-by-4)

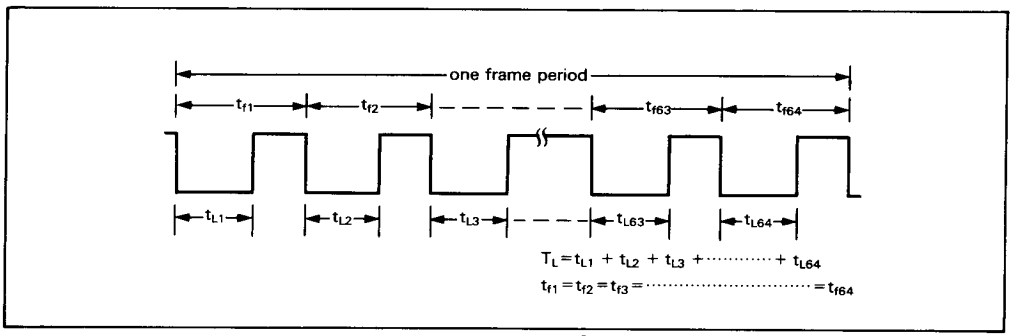


Figure 40 PWM Waveform

PROM Mode Pin Description

Table 25 and figure 41 describe the pin function in PROM mode.

Table 25. PROM Mode Signals

Pin No.		MCU mode		PROM mode		Pin No.		MCU mode		PROM mode	
DC-64S DP-64S	FP-64B	Pin name	I/O	Pin name	I/O	DC-64S DP-64S	FP-64B	Pin name	I/O	Pin name	I/O
1	59	D_{11}/FS_4	I/O			33	27	$R4_0/\overline{SCK}$	I/O		
2	60	D_{12}/FS_3	I/O			34	28	$R4_1/SI$	I/O	O_4	I/O
3	61	D_{13}/FS_2	I/O			35	29	$R4_2/SO$	I/O	O_3	I/O
4	62	D_{14}/FS_1	I/O			36	30	$R4_3/PWM$	I/O	O_2	I/O
5	63	D_{15}/FS_0	I/O			37	31	$R7_0/BUZZ$	I/O	O_4	I/O
6	64	$R0_0/FD_0$	I/O	A_1	I	38	32	$R7_1$	I/O	O_5	I/O
7	1	$R0_1/FD_1$	I/O	A_2	I	39	33	$R7_2$	I/O	O_6	I/O
8	2	$R0_2/FD_2$	I/O	A_3	I	40	34	$R7_3$	I/O	O_7	I/O
9	3	$R0_3/FD_3$	I/O	A_4	I	41	35	$R8_0$	I/O	O_1	I/O
10	4	$R1_0/FD_4$	I/O	A_5	I	42	36	$R8_1$	I/O	O_0	I/O
11	5	$R1_1/FD_5$	I/O	A_6	I	43	37	$R9_0$	I	V_{PP}	
12	6	$R1_2/FD_6$	I/O	A_7	I	44	38	$R9_1$	I	A_9	I
13	7	$R1_3/FD_7$	I/O	A_8	I	45	39	$R9_2$	I	$\overline{M_0}$	I
14	8	$R2_0/FD_8$	I/O	A_0	I	46	40	$R9_3$	I	$\overline{M_1}$	I
15	9	$R2_1/FD_9$	I/O	A_{10}	I	47	41	RESET	I	RESET	I
16	10	$R2_2/FD_{10}$	I/O	A_{11}	I	48	42	OSC_2	O		
17	11	$R2_3/FD_{11}$	I/O	A_{12}	I	49	43	OSC_1	I		
18	12	RA_0	I	V_{CC}		50	44	GND		GND	
19	13	RA_1/Vdisp	I			51	45	CL_1	I	GND	
20	14	$R3_0/FD_{12}$	I/O	A_{13}	I	52	46	CL_2	O		
21	15	$R3_1/FD_{13}$	I/O	A_{14}	I	53	47	$\overline{TEST}$	I	$\overline{TEST}$	I
22	16	$R3_2/FD_{14}$	I/O			54	48	D_0/FS_{15}	I/O		
23	17	$R3_3/FD_{15}$	I/O			55	49	D_1/FS_{14}	I/O		
24	18	$R5_0$	I/O	$\overline{CE}$	I	56	50	D_2/FS_{13}	I/O		
25	19	$R5_1$	I/O	$\overline{OE}$	I	57	51	D_3/FS_{12}	I/O		
26	20	$R5_2$	I/O	V_{CC}		58	52	D_4/FS_{11}	I/O		
27	21	$R5_3$	I/O	V_{CC}		59	53	D_5/FS_{10}	I/O		
28	22	$R6_0/\overline{INT_0}$	I/O	O_0	I/O	60	54	D_6/FS_9	I/O		
29	23	$R6_1/\overline{INT_1}$	I/O	O_1	I/O	61	55	D_7/FS_8	I/O		
30	24	$R6_2/\overline{INT_2}$	I/O	O_2	I/O	62	56	D_8/FS_7	I/O		
31	25	$R6_3/\overline{INT_3}$	I/O	O_3	I/O	63	57	D_9/FS_6	I/O		
32	26	V_{CC}				64	58	D_{10}/FS_5	I/O		

Notes: 1. I/O: Input/Output Pins, I: Input Pins, O: Output Pins
2. Connect each pair of O_4, O_3, O_2, O_1 and O_0. Hitachi supplies the socket adapter on which these pairs are internally connected.

Pins for PROM Mode (HD4074709)

V_{PP}

Apply the programming voltage (12.5V ± 0.3 V) to V_{PP}.

$\overline{CE}$

Program the internal PROM and input the control signal to enable verify.

$\overline{OE}$

Input the data output control signal when verify.

A_0 – A_{14}

A_0 – A_{14} are address input pins of the internal PROM.

O_0 – O_7

O_0 – O_7 are data bus I/O pins of the internal PROM.

$\overline{M_0}$, $\overline{M_1}$

These are for PROM mode specification. To put the MCU into the PROM mode, pull $\overline{M_0}$, $\overline{M_1}$, and $\overline{TEST}$ to low level, and RESET to high level.

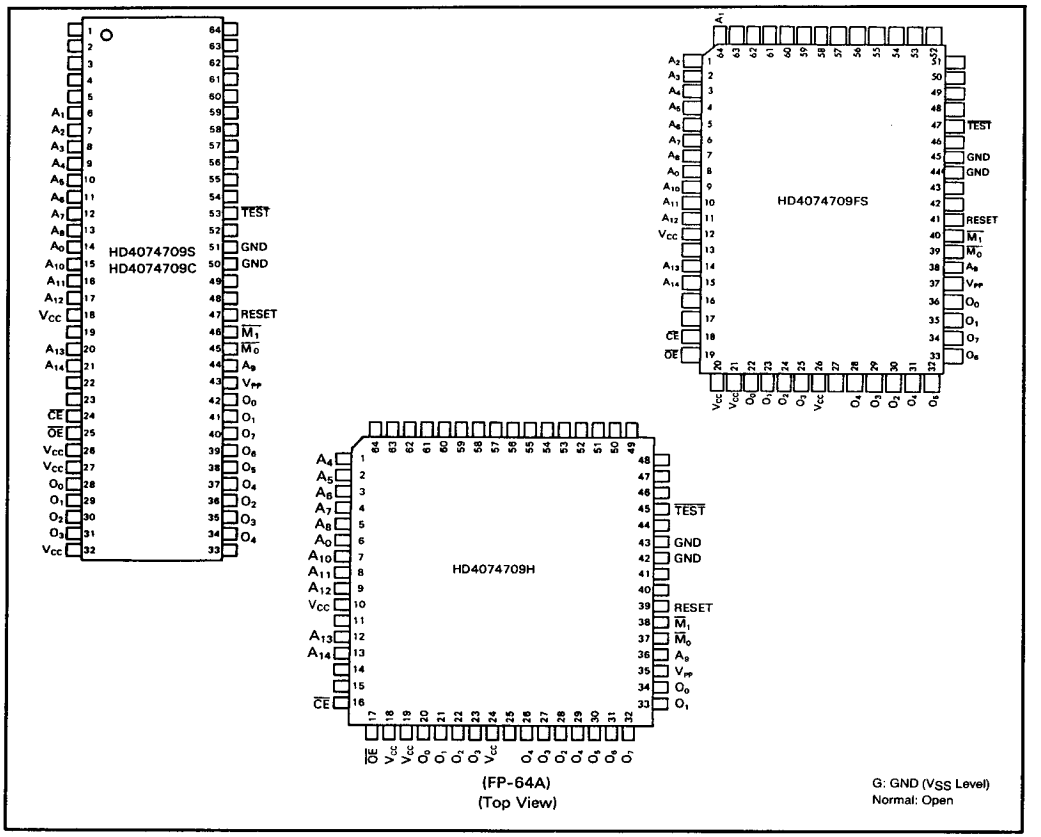


Figure 41. Pin Assignment in PROM Mode

Programmable ROM (HD4074709)

The PROM mode of the HD4074709 internally halts the MCU operation and allows the PROM to be programmed. The MCU enters the PROM mode when the $\overline{TEST}$, $\overline{M_0}$ and $\overline{M_1}$ pins go to low and the RESET pin goes to high. The specifications for the PROM are the same as for the EPROM 27256; therefore, the PROM is programmed with a general-purpose ROM writer using a 64-to-28 pin socket adapter.

In order to program the PROM with using a general-purpose PROM writer, the HD407 4709 incorporates the conversion circuit which divides a 10-bit HMCS series instruction into 5 higher bits and 5 lower bits. One MCU address is assigned to two PROM addresses. For example, in programming an 8k-word PROM with a general-purpose PROM writer, the user must assign 16 kbyte address locations.

Programming and Verification

The HD4074709 can perform high-speed programming without causing voltage stress or degrading data reliability. Figures 44 and 45 show the procedure for high-speed programming and timing chart, respectively. For details of PROM programming, see Precautions on PROM Programming.

Erasing

PROMs in ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are: ultraviolet (UV) light with wavelength 2537Å with a minimum irradiation of 15W · sec/cm². These conditions are satisfied by exposing the LSI to a 12,000 μW/cm² UV source for 15-20 minutes, at a distance of 1 inch.

Precautions

1. The user must specify address locations $0000 through $7FFF when programming the PROM with a general-purpose PROM writer. If $8000 or higher locations are addressed, the PROM cannot be programmed or verified. It should be noted that the plastic package type of the PROM cannot be erased and reprogrammed due to this error. The data written in unused address locations must be $FF.
   * The ceramic package type of the PROM can be erased and reprogrammed by ultraviolet light in the event of programming errors.
2. If any index of the PROM socket, socket adapter and LSI does not match, an overcurrent can occur, resulting in LSI destruction. Verify that the LSI is properly connected to the PROM writer before programming.
3. In general, the PROM is provided with a programming voltage (V_{PP}) either 12.5V or 21V. The V_{PP} of the HD4074709 PROM is 12.5V. If the user applies 21V to the PROM, this may permanenty damage the LSI. The PROM writer in Intel's 27256 specifications selects 12.5V as V_{PP}.

Table 26. Mode selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**$O_0 - O_7$**
Programming	low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 27. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapters		
Maker	**Type name**	**Package**	**Maker**	**Type name**
DATA I/O	22B 29B	DP-64S DC-64S	Hitachi	HS470ESS11H
		FP-64B	Hitachi	HS470ESF01H
		FP-64A	Hitachi	HS470ESH01H
AVAL CORP	PKW-1000 PKW-7000	DP-64S DC-64S	Hitachi	HS470ESS21H
		FP-64B	Hitachi	HS470ESF01H

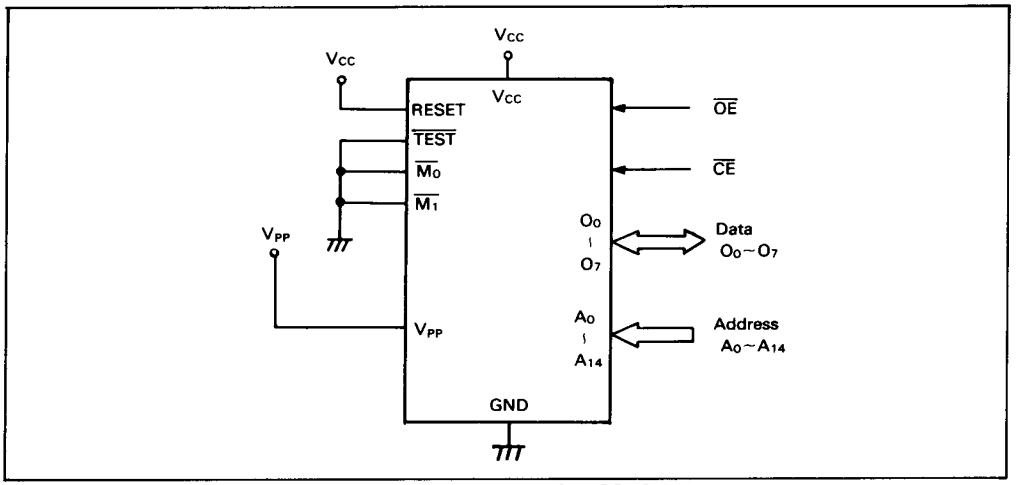


Figure 42. PROM Mode

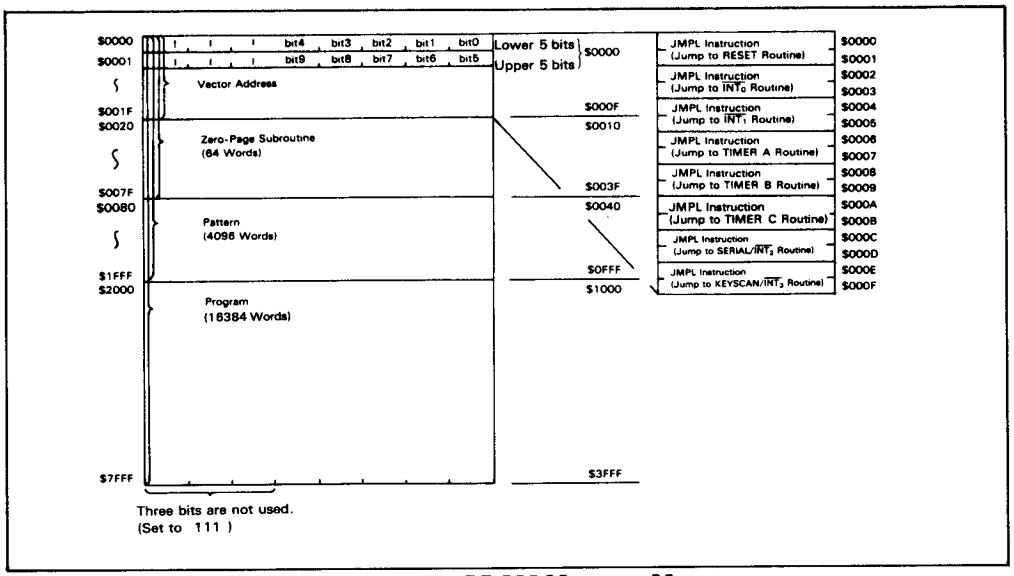


Figure 43. PROM Memory Map

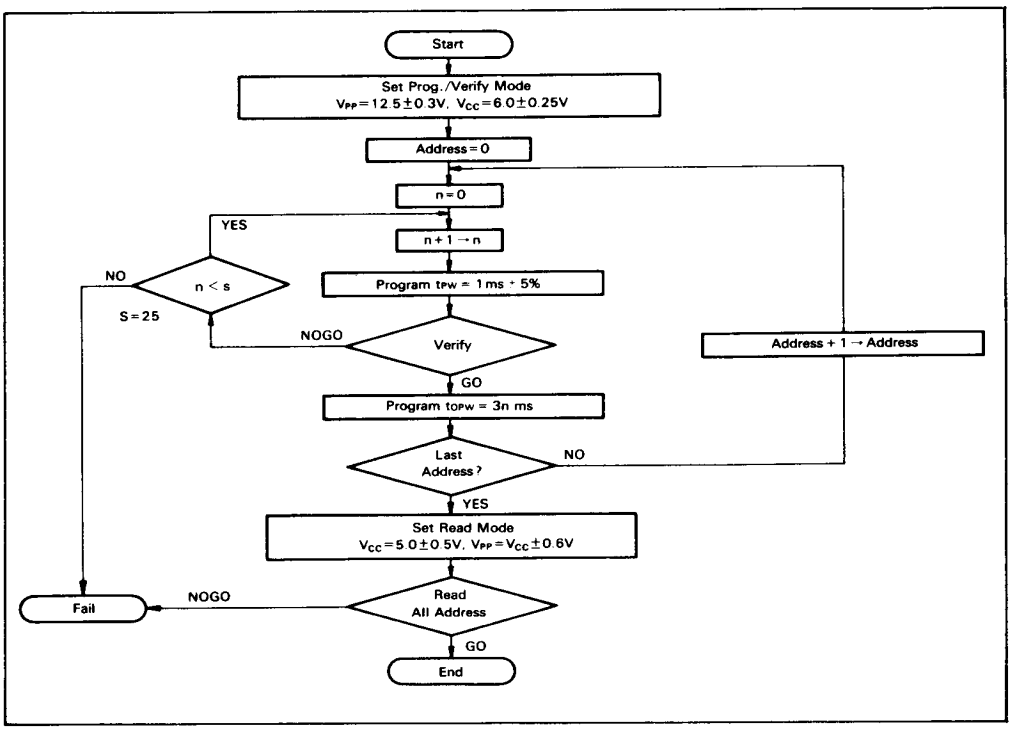


Figure 44. A Sequence of High Speed Programming

Programming Electrical Characteristics

DC Characteristics
(V_{CC}=6 V ± 0.25 V, V_{PP}=12.5 V ± 0.3 V, V_{SS}=0 V, Ta=25 °C ± 5 °C, unless otherwise notes.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	O_0—O_7, A_0—A_{14}, $\overline{OE}$, $\overline{CE}$	V_{IH}	2.2		V_{CC}+0.3	V	
Input low voltage	O_0—O_7, A_0—A_{14}, $\overline{OE}$, $\overline{CE}$	V_{IL}	−0.3		0.8	V	
Output high voltage	O_0—O_7	V_{OH}	2.4			V	I_{OH}=−200μA
Output low voltage	O_0—O_7	V_{OL}			0.4	V	I_{OL}=1.6mA
Input leakage current	O_0—O_7, A_0—A_{14}, $\overline{OE}$, $\overline{CE}$	$\|I_{LI}\|$			2	μA	V_{in}=5.25V/0.5V
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics
(V_{CC}=6 V ± 0.25 V, V_{PP}=12.5 V ± 0.3 V, V_{SS}=0 V, Ta=25 °C ± 5 °C, unless otherwise notes.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time	t_{AS}	2			μs	Figure 45[1]
$\overline{OE}$ set-up time	t_{OES}	2			μs	
Data set-up time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} set-up time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

Note : 1. Input Pulse level——0.8 to 2.2V
Input rising/falling time≦20ns
Timing reference level { input : 1.0V, 2.0V
output : 0.8V, 2.0V

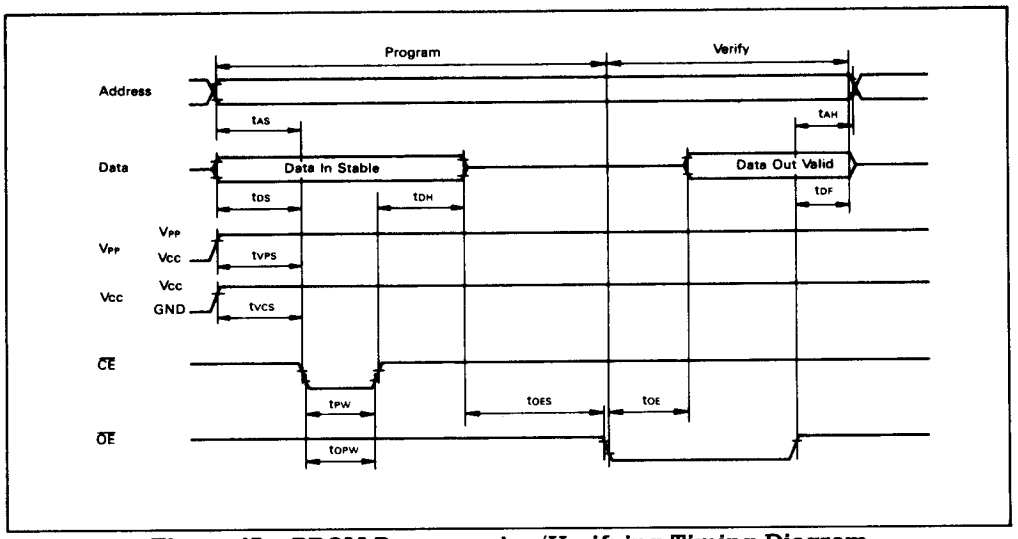


Figure 45. PROM Programming/Verifying Timing Diagram

Switching characteristics

Input pulse level ·····0.8V to 2.2V
Input rising/falling time ·····≦20 ns
Output loading ·····1TTL Gate + 100pF
Input/output timing reference level ·····Output: 1V, 2V
Input: 0.8V, 2V

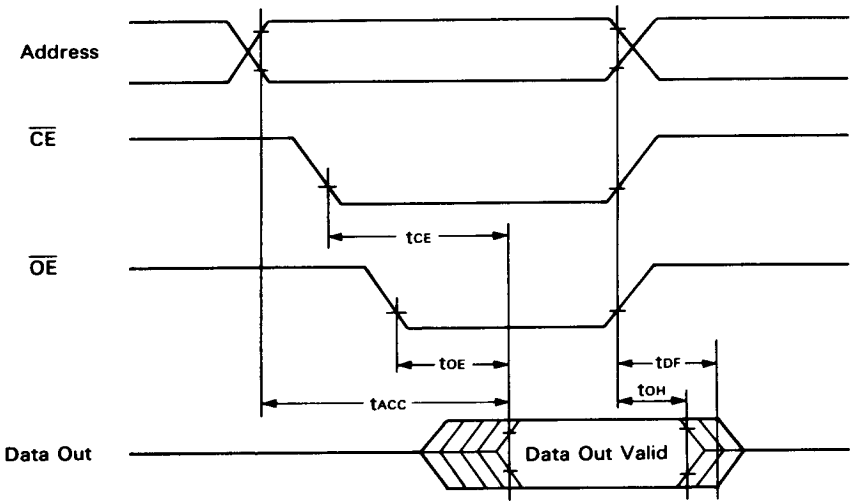


Figure 46. PROM Read Timing Diagram

Read Operation Electrical Characteristics

DC Characteristics
(V_{CC}=5 V ± 10 %, V_{PP}=V_{CC} ±0.6 V, V_{SS}=0 V, Ta=25 °C ± 5 °C, unless otherwise notes.)

Item	Symbol	Min	Typ	Max	Unit	Condition
Input Leak Current	I_{LI}			1	μA	V_{CC}=5.5V, Vin=GND to V_{CC}
Output Leak Current	I_{LO}			1	μA	V_{CC}=5.5V, Vout=GND to V_{CC}
Programming V_{PP} Current	I_{PP}		1	100	μA	V_{PP}=V_{CC}+0.6V
Operating V_{CC} Current	I_{CC}*			30	mA	f=1MHz, Iout=0mA
Input Voltage	V_{IL}	−0.3		0.8	V	
	V_{IH}	2.2		V_{CC}+0.3	V	
Output Voltage	V_{OL}			0.4	V	I_{OL}=1.6mA
	V_{OH}	2.4			V	I_{OH}=−200μA

* Input through current is excluded.

AC Characteristics
(V_{CC}=5 V ± 10 %, V_{PP}=V_{CC} ±0.6 V, V_{SS}=0 V, Ta=25 °C ± 5 °C, unless otherwise notes.)

Item	Symbol	Min	Max	Unit	Condition
Access Time	t_{ACC}		500	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}
$\overline{CE}$ Output Delay Time	t_{CE}		500	ns	$\overline{OE}$=V_{IL}
$\overline{OE}$ Output Delay Time	t_{OE}	10	150	ns	$\overline{CE}$=V_{IL}
Output Disable Delay Time	t_{DF}*	0	105	ns	$\overline{CE}$=V_{IL}
Data Output Hold Time	t_{OH}	0		ns	$\overline{CE}$=$\overline{OE}$=V_{IL}

* t_{DF} is determined when the output reaches open state and output level cannot be referred.

Precautions on PROM Programming

Principles of PROM Programming/ Erasing

The ZTAT microcomputer has the same type of the memory cell as the EPROM. The PROM is programmed by applying high voltage to the control gate and drain and injecting hot electrons into the floating gate, in the same way in the EPROM programming. The electrons in the floating gate remains stabilized, surrounded by the energy barrier of SiO_2 film. By this electrons, the threshold voltage in the memory cell changes and the corresponding bit goes to 0.

The hot electrons are reduced as over time. This reduction is caused by:

1. Ultraviolet light ·····The electrons are discharged by the ultraviolet light (erasure principle)
2. Heat ·····The electrons, which are excited by heat, are discharged
3. Application of high voltage···The number of electrons is reduced due to the high voltage which is applied to the control gate and drain

If there is any failure in the oxide film, the charge is markedly reduced; however, in general, such reduction does not occur, since devices which failed are usually excluded during screening tests.

When the memory cell does not have any hot electrons in the floating gate, the corresponding bit goes to 1.

PROM Programming

PROM programming should be performed under specified voltage and timing conditions. The higher the program voltage (V_{PP}) and the longer the program pulse width (t_{PW}), the more electrons will be injected into the memory cell. If an overvoltage is applied, a P-N junction may be permanently damaged. It is especially important to note that an overshoot occurs in the PROM writer. Moreover, negative voltage noise causes a parasitic transistor effect, which can reduce the apparent breakdown voltage.

During PROM programming, the ZTAT microcomputer is electrically connected with the PROM writer via the socket adapter. The user should ensure the following:

1. Confirm that the socket adapter is firmly connected to the PROM writer before beginning PROM programming.
2. Do not touch the socket adapter and the LSI during programming; this can cause faulty contacts, resulting in programming errors.

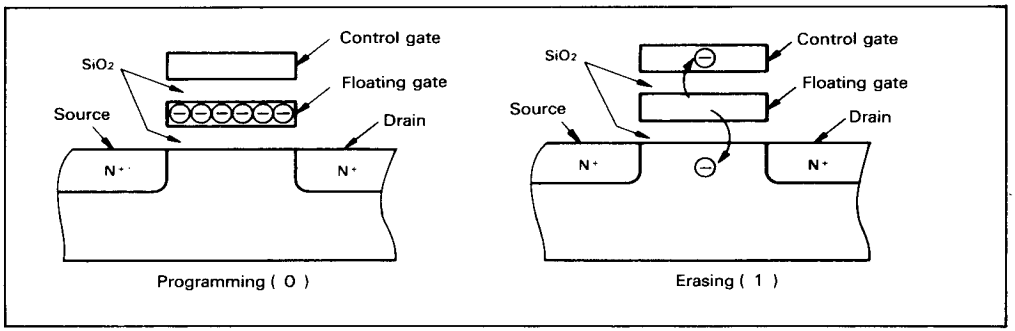


Figure 47. Cross Section of PROM Memory Cell

PROM Reliability after Programming

In general, semiconductor devices retain their reliability, if some initial failures can be rejected. Initial failures can be rejected by adequate screening. Baking the device under high-temperature conditions is a screening method which eliminates initial short-time data hold failures in the memory cell. (See Principles of PROM Programming/Erasing). ZTAT microcomputer devices realize good reliability because they have been subjected to such screening during the water fabrication process. It is recommended that the user expose the device to 150°C at one atmosphere after programming in order to verify device performance.

Figure 48. shows the recommended screening procedure.

Window-Type Package Precautions

Glass Erasure Window: If the glass window comes in contact with plastic or anything with a static charge, the LSI may malfunction due to the electrostatic charge on the surface of the window. If this occurs, exposing the LSI to ultraviolet light for a few minutes neutralizes the charge, and restores the LSI to normal operation. However, charge stored in the floating gate decreases at the same time, so reprogramming is recommended.

Electrostatic charge buildup on the window is a fundamental cause of malfunctions. Measures for its prevention are the same as those for preventing electrostatic breakdown:

1. Operators should be grounded when handling equipment.
2. Do not rub the glass window with plastics.
3. Be careful of coolant sprays, which may contain a few ions.
4. The ultraviolet shading label (which includes conductive material) effectively neutralizes charge.

Ultraviolet Shading Label: If the LSI is exposed to fluorescent light or sunlight, its memory contents may be erased by the small quantity of ultraviolet light in these sources. In strong light, the MCU may fail under the influence of photocurrent. To prevent these problems, it is recommended that the device be used with an ultraviolet shading label covering the erasure window after programming.

Special labels are sold for this purpose. They contain metal to absorb ultraviolet light. When choosing a label, note the following:

1. Adhesion (mechanical intensity)—Re-use and dust reduce adhesion. Peeling off a label may cause static electricity. Therefore, erasing and rewriting is recom-

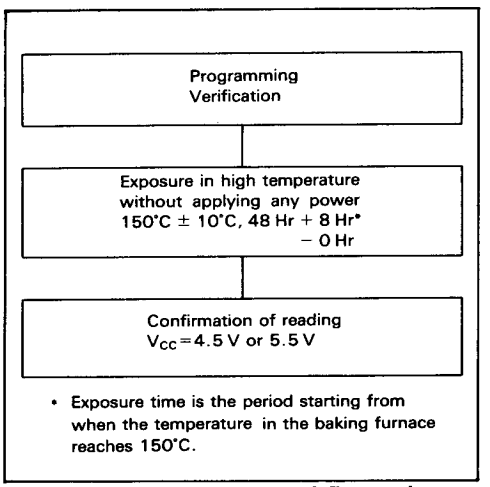


Figure 48. Recommended Screening Procedure

(note) If programming errors occur sequentially during PROM programming, the user should suspend programming and determine whether there is any trouble with the PROM writer or the socket adapter when using the window-package-type of the EPROM. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi of the trouble.

mended after peeling. Sticking a new label over the old one is better than replacing a label.

2. Allowable temperature range—The allowable environmental temperature range of the label should be noted. If it is used under conditions outside this range, the paste may stiffen or adhere to the label, causing paste to remain on the window when the label is removed.
3. Moisture resistance—The allowable moisture range and environmental conditions of the label should be noted. It is difficult to find a shade label applicable to all conditions. The proper label should be selected depending on the intended use of the MCU.

Addressing Mode

RAM Addressing Mode

As shown in figure 49, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

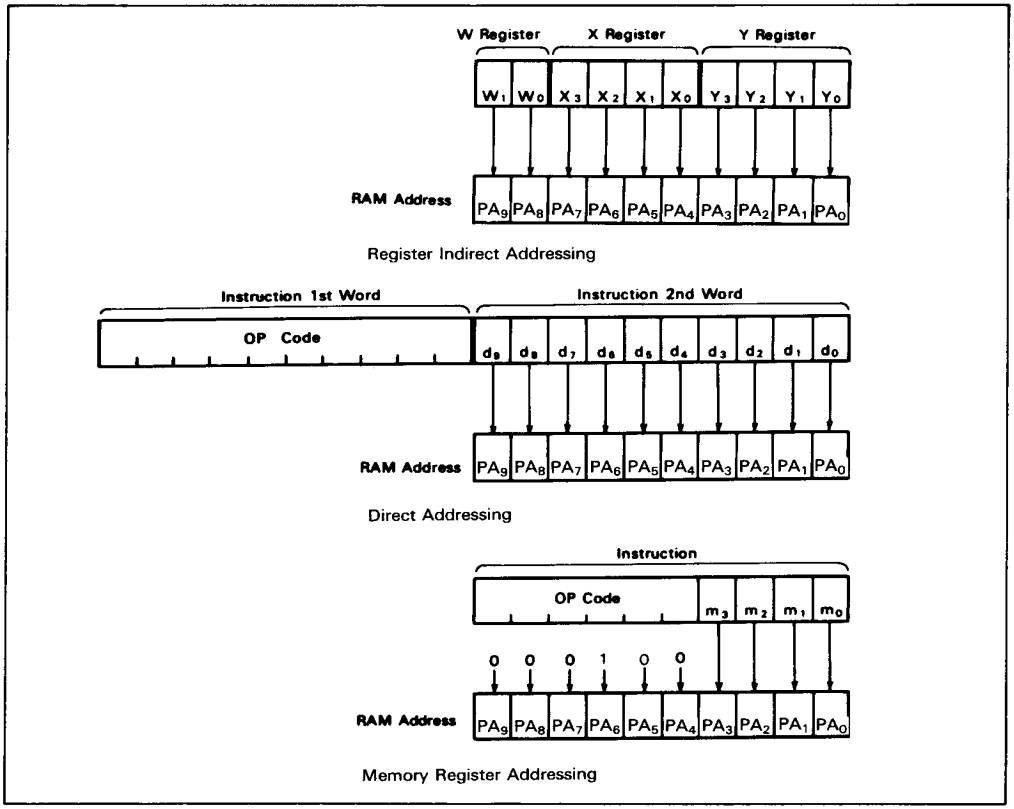


Figure 49. RAM Addressing Modes

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from $040 to $04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 50.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address $0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on page boundary (256n + 255) (figure 52), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at $0000-$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 51). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

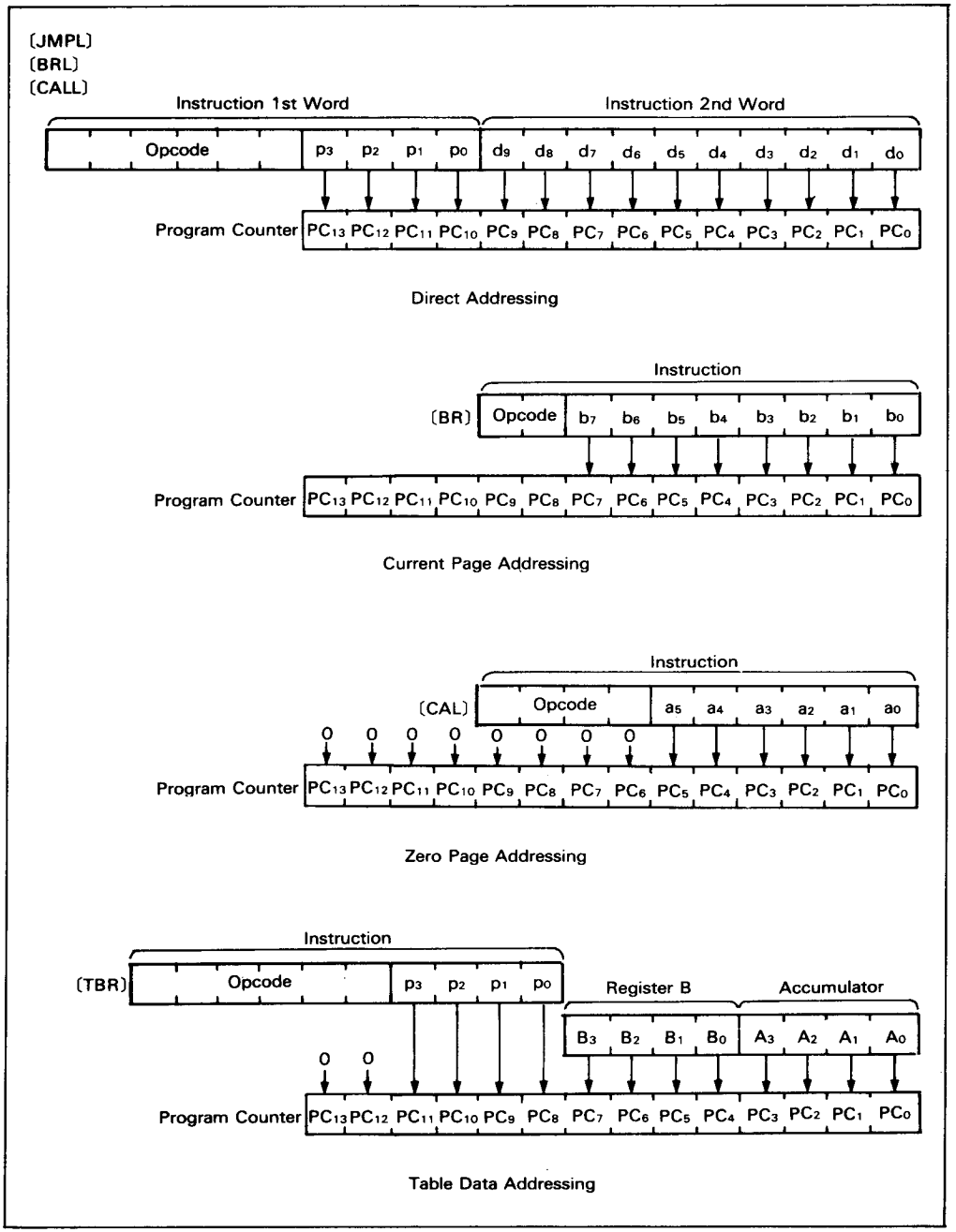


Figure 50. ROM Addressing Modes

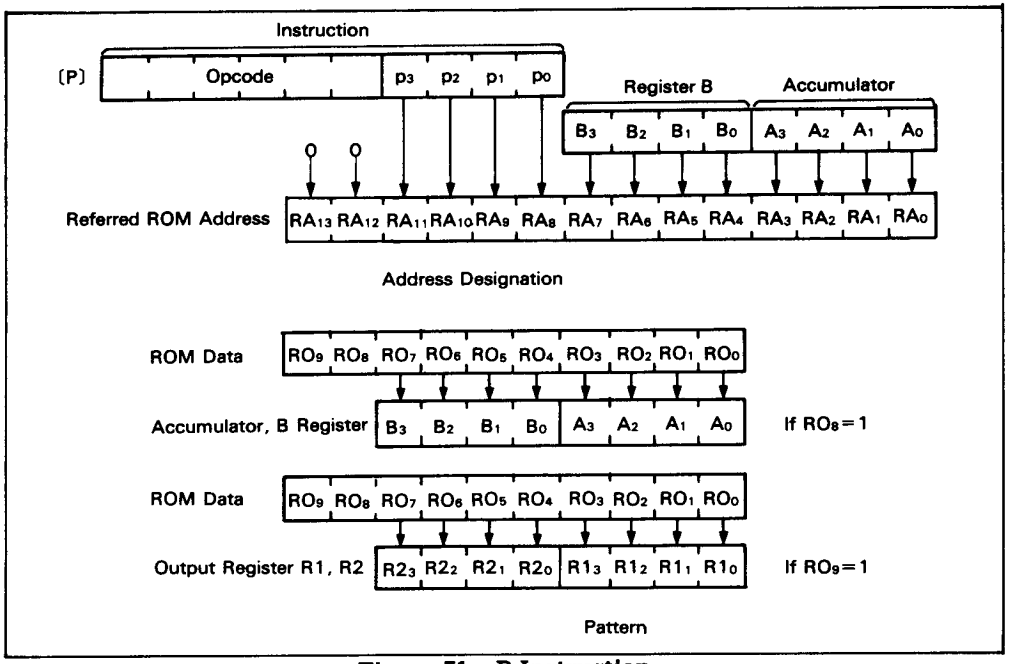


Figure 51. P Instruction

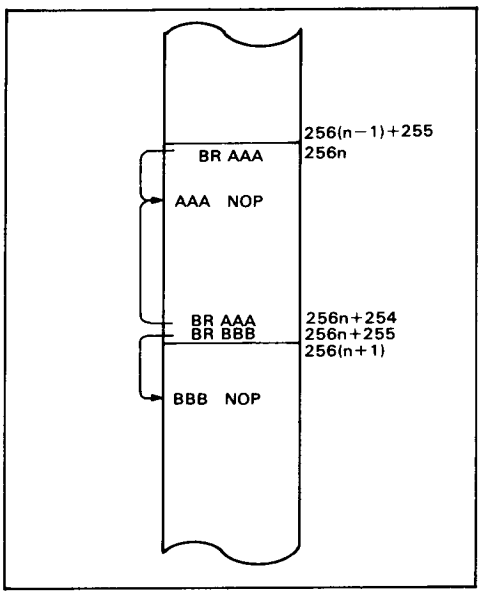


Figure 52. The Branch Destination by BR Instruction on the Boundary Between Pages

Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows:

(1) Immediate instructions
(2) Register-to-register instructions
(3) RAM address instructions
(4) RAM register instructions
(5) Arithmetic instructions
(6) Compare instructions
(7) RAM bit manipulation instructions
(8) ROM address instructions
(9) Input/output instructions
(10) Control instructions

Tables 28-37 list their functions, and table 38 is an opcode map.

Table 28. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M, Y+1→Y	NZ	1/1

Table 29. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 30. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX, Y↔SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 31. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X↔SPX, Y↔SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M↔B, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y−1→Y (X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X↔SPX, Y↔SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X↔SPX, Y↔SPY)		1/1

Note: (XY) and (X) have the following meaning:

(1) The instructions with (XY) have four mnemonics and four object codes for each (example of LAM (XY) is given below).
The op-code X or Y is assembled as follows:

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X↔SPX, Y↔SPY

(2) The instructions with (X) have two mnemonics and two object codes for each (example of LMAIY(X) is given below).
The op-code X is assembled as follows:

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 32. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$+1 →A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$ → B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B→A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∩ M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∪ M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ⊕ M→A	NZ	2/2

Note: ∩ : Logical AND
∪ : Logical OR
⊕ : Exclusive OR

Table 33. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≤ i	NB	1/1

Table 34. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 35. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 →I/E CA recovery	ST	1/3

Table 36. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 37. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode/ Watch mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode/Watch mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Table 38. Opcode Map

R9 \ R8		0																1													
	L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	PXS	PXS	PXS	XSP XY	AN EM			AM				ORM				LAW				ANEMD				AMD				ORMD			
	1	RTN	RTNI			ALEM				AMC				EORM				LWA				ALEMD				AMCD				EORMD			
	2	INEM i(4)																INEMD i(4)															
	3	ILEM i(4)																ILEMD i(4)															
	4	LBM(XY)				BNEM				LAB				IB				COMB				OR				STS				SBY	STOP		
	5	LMAIY(X)				AYY				LASPY				IY				JMPL p(4)															
	6	NEGA				RED				LASPX							TC	CALL p(4)															
	7	YNEI i(4)																BRL p(4)															
	8	XMA(XY)				SEM n(2)				REM n(2)				TM n(2)				XMAD				SEMD n(2)				REMD n(2)				TMD n(2)			
	9	LAM(XY)				LMA(XY)				SMC				ANM				LAMD				LMAD				SMCD				ANMD			
	A	ROTR	ROTL				DAA				DAS						LAY	LMID i(4)															
	B	TBR p(4)																P p(4)															
	C	XMB(XY)				BLEM				LBA							DB	CAL a(6)															
	D	LMADY(X)				SYY				LYA							DY																
	E	TD				SED				LXA				REC			SEC																
	F	LWI i(2)																															
1	0	LBI i(4)																BR b(8)															
	1	LYI i(4)																															
	2	LXI i(4)																															
	3	LAI i(4)																															
	4	LBR m(4)																															
	5	LAR m(4)																															
	6	REDD m(4)																															
	7	LAMR m(4)																															
	8	AI i(4)																															
	9	LMIIY i(4)																															
	A	TDD m(4)																															
	B	ALEI i(4)																															
	C	LRB m(4)																															
	D	LRA m(4)																															
	E	SEDD m(4)																															
	F	XMRA m(4)																															

1-word/2-cycle Instruction

1-word/3-cycle Instruction

RAM Direct Address Instruction (2-word/2-cycle)

2-word/2-cycle Instruction

is not available, the undifined instruction.

Absolute Maximum Ratings

Item	Symbol	Constant	Unit	Notes
Supply Voltage	V_{CC}	−0.3 to + 7.0	V	
Programming Voltage	V_{PP}	−0.3 to + 14.0	V	12
Terminal Voltage	V_T	−0.3 to V_{CC} + 0.3	V	3
		V_{CC} − 42 to V_{CC} + 0.3	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Total Allowance of Output Current	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		30	mA	9, 11
Operating Temperature	T_{opr}	−20 to + 75	°C	
Storage Temperature	T_{stg}	−55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	−25 to + 80	°C	12

Notes:
1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. All voltages are with respect to GND.
3. Standard pins
4. High voltage pins
5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
8. R4-R8
9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
10. R4 − R8
11. $D_0 - D_{15}$, R0 − R3
12. HD4074709

Electrical Characteristics

HD404708, HD404709 Electrical Characteristics

DC Characteristics

(V_{CC} = 3 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, INT_0 − INT_3	0.8 V_{CC}	−	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	−	V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5	−	V_{CC} + 0.3	V	V_{CC} = 3.5V to 6.0V	
			V_{CC} − 0.3	−	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	RESET, SCK, INT_0 − INT_3	− 0.3	−	0.2 V_{CC}	V		
		SI	− 0.3	−	0.3 V_{CC}	V		
		OSC_1	− 0.3	−	0.5	V	V_{CC} = 3.5V to 6.0V	
			− 0.3	−	0.3	V		
Output High Voltage	V_{OH}	SCK, SO, PWM, BUZZ	V_{CC} − 1.0	−	−	V	$-I_{OH}$ = 1.0mA, V_{CC} = 3.5V to 6.0V	
			V_{CC} − 0.5	−	−	V	$-I_{OH}$ = 0.5mA, V_{CC} = 3.5V to 6.0V	
							$-I_{OH}$ = 0.3mA	
Output Low Voltage	V_{OL}	SCK, SO, PWM, BUZZ	−	−	0.4	V	I_{OL} = 1.6mA, V_{CC} = 3.5V to 6.0V	
							I_{OL} = 0.4mA	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, SCK, INT_0 − INT_3 SI, SO, PWM, BUZZ OSC_1	−	−	1	μA	V_{in} = 0V to V_{CC}	1
Power Dissipation in Active Mode	I_{CC}	V_{CC}	−	−	5.0	mA	V_{CC} = 5V, f_{OSC} = 4MHz, Divide-by-4	2,5,8
					8.0	mA		9
			−	−	3.0	mA	V_{CC} = 3V, f_{OSC} = 2MHz, Divide-by-4	2,5,8
					4.5	mA		9
Power Dissipation in Standby Mode	I_{SBY}	V_{CC}	−	−	2.0	mA	V_{CC} = 5V, f_{OSC} = 4MHz, Divide-by-4	3,5
			−	−	1.0	mA	V_{CC} = 3V, f_{OSC} = 2MHz, Divide-by-4	3,5

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Power Dissipation in Subactive Mode	I_{sub}	V_{CC}	–	–	30	μA	V_{CC} = 3V, when using 32.768kHz crystal $V_{in}(\overline{TEST}) = V_{CC}$ – 0.3V to V_{CC}, V_{in}(RESET) = 0V to 0.3V	4,6,8
			–	–	80	μA		9
Power Dissipation in Watch Mode	I_{watch}	V_{CC}	–	–	15	μA	V_{CC} = 3V, when using 32.768kHz crystal, $V_{in}(\overline{TEST}) = V_{CC}$ – 0.3V to V_{CC}, V_{in}(RESET) = 0V to 0.3V	4,6,7
Power Dissipation in Stop Mode	I_{stop}	V_{CC}	–	–	10	μA	$V_{in}(\overline{TEST}) = V_{CC}$ – 0.3V to V_{CC}, V_{in}(RESET) = 0V to 0.3V not using 32.768kHz crystal	4
Watch Mode Retain Voltage	V_{watch}	V_{CC}	3.5	–	6.0	V	V_{CC} = 3.5V to 6V	6,7
			3.0	–	6.0	V		
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2	–	–	V	not using 32.768kHz crystal	

Notes:
1. Excluding pull-up MOS current and output buffer current.
2. The MCU is reset and input/output current does not flow.
   Pin conditions:
   - RESET, $\overline{TEST}$……V_{CC}
   - R4-R9……V_{CC}
   - D_0-D_{15}, R0-R3, RA……V_{disp}
3. The timer/counter is enabled and input/output current does not flow.
   MCU conditions:
   - I/O……same as at reset
   - Serial interface……halt
   - Standby mode

   Pin conditions:
   - $\overline{RESET}$……GND
   - $\overline{TEST}$……V_{CC}
   - R4-R9……V_{CC}
   - D_0-D_{15}, R0-R3, RA……V_{disp}
4. Excluding pull-down MOS current to V_{disp}.
5. Power dissipation in MCU operation or in Standby mode is in proportion to f_{OSC}; each current value when f_{OSC} = x[MHz] is given by the following equation:
   Maximum value (f_{OSC} = x[MHz]) = x/4 x Max. value (f_{OSC} = 4[MHz])
6. Applied to the product with 32 kHz CPU operation selected by optional function.
7. Applied to the product with no 32 kHz CPU operation, TIME-BASE operation selected by optional function.
8. HD404708
9. HD404709

Input/Output Characteristics for Standard Pins

(V_{CC} = 3 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	R4-R9	0.7 V_{CC}	–	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	R4-R9	− 0.3	–	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	R4-R8	V_{CC}−1.0	–	–	V	$-I_{OH}$=1.0mA, V_{CC}=3.5V to 6.0V	
			V_{CC}−0.5	–	–	V	$-I_{OH}$=0.5mA, V_{CC}=3.5V to 6.0V	
							$-I_{OH}$=0.3mA	
Output Low Voltage	V_{OL}	R4-R8	–	–	0.4	V	I_{OL}=1.6mA, V_{CC}=3.5V to 6.0V	
							I_{OL}=0.4mA	
Input/Output Leakage Current	$\|I_{IL}\|$	R4-R9	–	–	1	μA	V_{in}=0V to V_{CC}	1
Pull-Up MOS Current	$-I_P$	R4-R9	30	70	150	μA	V_{CC}=5V, V_{in}=0V	2
			10	20	50	μA	V_{CC}=3V, V_{in}=0V	

Notes: 1. Pull-up MOS current and output buffer current are excluded.
2. Applied to I/O pins with pull-up MOS selected by mask option.

Input/Output Characteristics for High Voltage Pins

(V_{CC} = 3 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	D_0-D_{15},RA, R0-R3	0.7 V_{CC}	–	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_0-D_{15},RA, R0-R3	V_{CC}−40V	–	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D_0-D_{15}, R0-R3	V_{CC}−3.0	–	–	V	$-I_{OH}$=15mA, V_{CC}=5V±20%	
			V_{CC}−2.0	–	–	V	$-I_{OH}$=10mA, V_{CC}=5V±20%	
			V_{CC}−1.0	–	–	V	$-I_{OH}$=4mA	
Output Low Voltage	V_{OL}	D_0-D_{15}, R0-R3	–	–	V_{CC}−34	V	V_{disp}=V_{CC}−40V	1
		D_0-D_{15}, R0-R3	–	–	V_{CC}−37	V	150kΩ to V_{CC}−40V	2
Input/Output Leakage Current	$\|I_{IL}\|$	D_0-D_{15},RA R0-R3	–	–	20	μA	V_{in}=V_{CC}−40V to V_{CC}	3
Pull-Down MOS Current	I_d	D_0-D_{15},RA, R0-R3	200	400	800	μA	V_{disp}=V_{CC}−35V V_{in}=V_{CC}	4

Notes: 1. Applied to I/O pins with pull-down MOS selected by mask option.
Applied to I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
2. Pull-down MOS current and output buffer current are excluded.
Applied to I/O pins with pull-down MOS selected by mask option.

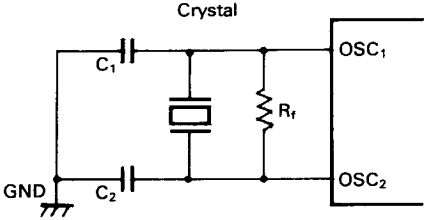
AC Characteristics

(V_{CC} = 3 V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Oscillation Frequency (Divide-by-4)	f_{OSC}	OSC_1,OSC_2	0.4	4	4.5	MHz	V_{CC}=3.5V to 6V	7
			1.6	4	4.5	MHz		
			0.4	2	2.25	MHz		7
			1.6	2	2.25	MHz		
Oscillation Frequency (Divide-by-8)	f_{CL}	CL_1,CL_2	–	32.768	–	kHz		
Instruction Cycle Time	t_{cyc}		0.89	1	10	μs	V_{CC}=3.5V to 6V	7
			0.89	1	2.5	μs		
			1.78	2	10	μs		7
			1.78	2	2.5	μs		
Instruction Cycle Time	t_{SUBcyc}		–	244.14	–	μs		8
Oscillation Stabilization (Crystal)	t_{RC}	OSC_1,OSC_2	–	–	40	ms	V_{CC}=3.5V to 6V	1
			–	–	60	ms		
Oscillation Stabilization (Ceramic Filter)	t_{RC}	OSC_1,OSC_2	–	–	20	ms	V_{CC}=3.5V to 6V	1
			–	–	60	ms		
Oscillation Stabilization	t_{RC}	CL_1,CL_2	–	–	2	s		2,8,9
External Clock High, Low Level Width	t_{CPH}, t_{CPL}	OSC_1	92	–	–	ns	V_{CC}=3.5V to 6V	3
			203	–	–	ns		
External Clock Rising, Falling Time	t_{CPr}, t_{CPf}	OSC_1	–	–	20	ns	V_{CC}=3.5V to 6V	3
			–	–	20	ns		
$\overline{INT_0}$ High, Low Level Width	t_{I0H}, t_{I0L}	$\overline{INT_0}$	2	–	–	t_{cyc}/ t_{SUBcyc}		4,6,8,9
$\overline{INT_1}$ High, Low Level Width	t_{I1H}, t_{I1L}	$\overline{INT_1}$-$\overline{INT_3}$	2	–	–	t_{cyc}		4
RESET High Level Width	t_{RSTH}	RESET	2	–	–	t_{cyc}		5
Input Capacitance	C_{in}	All pins	–	–	30	pF	f=1MHz, V_{in}=0V	
RESET Falling Time	t_{RSTf}	RESET	–	–	20	ms		5

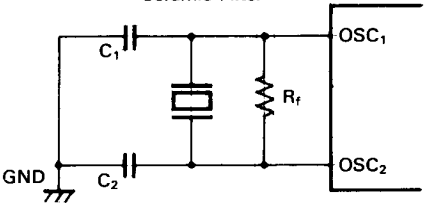
Notes: 1. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V (3.5V, in case of V_{CC}=3.5V−6.0V) after Power on, or after RESET goes high. RESET must be kept high for at least t_{RC} to obtain oscillation time.
Oscillation stabilization time depends on the crystal or ceramic filter's circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal or ceramic filter marker to determine the circuit parameter.

Crystal

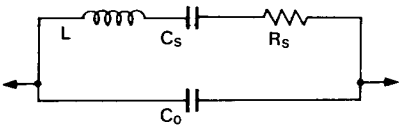


Xtal: Under the equivalent circuit
R_f: 1MΩ±20%
C_1: 10pF±20%
C_2: 10pF±20%

Ceramic Filter

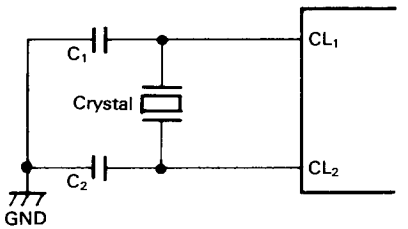


Ceramic Filter: CSA4.00MG (MURATA)
R_f: 1MΩ±20%
C_1: 30pF±20%
C_2: 30pF±20%

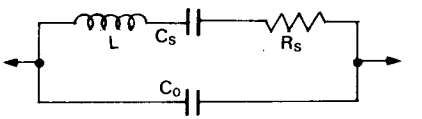


C_0=7pF max
R_S=100Ω max
f =1.0–4.5MHz

2. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V after power on.
   Oscillation stabilization time depends on the crystal circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal maker to determine the circuit parameter.



Xtal: MX38T (Nihon denpa kogyo)
Right the equivalent circuit
C_1: 15pF±5%
C_2: 15pF±5%



C_0=1.5pF typ
R_S=14kΩ typ
f =32.768kHz

3. See figure 53.
4. See figure 54. Unit t_{cyc} is applied when MCU is Standby or Active mode.
5. See figure 55.
6. See figure 54. Unit t_{SUBcyc} is applied when MCU is in Watch or Sub-Active mode.
   t_{SUBcyc}=244.14μs (when using 32.768kHz crystal oscillator)
7. Apply the data in parenthesis when subsystem oscillator is not used.
8. Applied to the product with 32kHz CPU operation selected by optional function.
9. Applied to the product with no 32kHz CPU operation, TIME-BASE operation selected by optional function.

Serial Interface Timing Characteristics

(V_{CC} = 3V to 6 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	1	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	80	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t_{SCKHD}	$\overline{SCK}$	1	–	–	t_{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{cyc}		1
Input Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	80	ns		1
Serial Output Data Delay Time	t_{DSO}	SO	–	–	600	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t_{SSI}	SI	200	–	–	ns		1
Serial Input Data Hold Time	t_{HSI}	SI	400	–	–	ns		1

Notes: 1. See figure 56.
2. See figure 57.
3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

(V_{CC} = 3.5 V to 6 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	1	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	40	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t_{SCKHD}	$\overline{SCK}$	1	–	–	t_{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{cyc}		1
Input Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	40	ns		1
Serial Output Data Delay Time	t_{DSO}	SO	–	–	300	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t_{SSI}	SI	100	–	–	ns		1
Serial Input Data Hold Time	t_{HSI}	SI	200	–	–	ns		1

Notes: 1. See figure 56.
2. See figure 57.
3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

Electrical Characteristics

HD4074709 Electrical Characteristics

DC Characteristics

(V_{CC} = 3 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, INT_0 − INT_3	0.8 V_{CC}	–	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	–	V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5		V_{CC} + 0.3	V	V_{CC}=3.5V to 5.5V	
			V_{CC} − 0.3	–	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	RESET, SCK, INT_0 − INT_3	− 0.3	–	0.2 V_{CC}	V		
		SI	− 0.3	–	0.3 V_{CC}	V		
		OSC_1	− 0.3	–	0.5	V	V_{CC}=3.5V to 5.5V	
			− 0.3	–	0.3	V		
Output High Voltage	V_{OH}	SCK, SO, PWM, BUZZ	V_{CC}−1.0	–	–	V	$-I_{OH}$=1.0mA V_{CC}=3.5V to 5.5V	
			V_{CC}−0.5	–	–	V	$-I_{OH}$=0.5mA V_{CC}=3.5V to 5.5V	
							$-I_{OH}$=0.3mA	
Output Low Voltage	V_{OL}	SCK, SO, PWM, BUZZ	–	–	0.4	V	I_{OL}=1.6mA V_{CC}=3.5V to 5.5V	
							I_{OL}=0.4mA	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, SCK, INT_0 − INT_3 SI, SO, PWM, BUZZ OSC_1	–	–	1	μA	V_{in}=0V to V_{CC}	1
Power Dissipation in Active Mode	I_{CC}	V_{CC}	–	–	8.0	mA	V_{CC}=5V, f_{OSC}=4MHz Divide-by-4	2,4
			–	–	4.5	mA	V_{CC}=3V, f_{OSC}=2MHz Divide-by-4	2,4
Power Dissipation in Standby Mode	I_{SBY}	V_{CC}	–	–	2.0	mA	V_{CC}=5V, f_{OSC}=4MHz Divide-by-4	3,4
			–	–	1.0	mA	V_{CC}=3V, f_{OSC}=2MHz Divide-by-4	3,4

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Power Dissipation in Subactive Mode	I_{sub}	V_{CC}	–	–	150	μA	V_{CC}=3V, when using 32.768kHz crystal, $V_{in}(\overline{TEST})=V_{CC}-0.3V$ to V_{CC}, V_{in}(RESET)=0V to 0.3V	
Power Dissipation in Watch Mode	I_{watch}	V_{CC}	–	–	15	μA	V_{CC}=3V, when using 32.768kHz crystal, $V_{in}(\overline{TEST})=V_{CC}-0.3V$ to V_{CC}, V_{in}(RESET)=0V to 0.3V	
Power Dissipation in Stop Mode	I_{stop}	V_{CC}	–	–	10	μA	$V_{in}(\overline{TEST}, R9_0)=V_{CC}-0.3V$ to V_{CC}, V_{in}(RESET)=0V to 0.3V not using 32.768kHz crystal	
Watch Mode Retain Voltage	V_{watch}	V_{CC}	3.5	–	5.5	V	V_{CC}=3.5V to 5.5V	
			3.0	–	5.5	V		
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2	–	–	V	not using 32.768kHz crystal	

Notes:
1. Excluding Pull-up MOS current and output buffer current
2. The MCU is reset and input/output current does not flow.
   Pin conditions:
   - RESET, $\overline{TEST}$……V_{CC}
   - R4-R9……V_{CC}
   - D_0-D_{15}, R0-R3, RA……V_{disp}
3. The timer/counter is enabled and input/output current does not flow.
   MCU Conditions:
   - I/O……same as at reset
   - Serial interface……halt
   - Standby mode

   Pin conditions:
   - RESET……GND
   - $\overline{TEST}$……V_{CC}
   - R4-R9……V_{CC}
   - D_0-D_{15}, R0-R3, RA……V_{disp}
4. Power dissipation in MCU operation or in Standby mode is in proportion to f_{OSC}; each current value when f_{OSC}=x[MHz] is given by the following equation:
   Maximum value (f_{OSC}=x[MHz])=x/4 × Max. value (f_{OSC}=4[MHz])

Input/Output Characteristics for Standard Pins

(V_{CC} = 3 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	R4-R9	0.7 V_{CC}	–	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	R4-R9	− 0.3	–	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	R4-R8	V_{CC}−1.0	–	–	V	$-I_{OH}$=1.0mA V_{CC}=3.5V to 5.5V	
			V_{CC}−0.5	–	–	V	$-I_{OH}$=0.5mA V_{CC}=3.5V to 5.5V	
							$-I_{OH}$=0.3mA	
Output Low Voltage	V_{OL}	R4-R8	–	–	0.4	V	I_{OL}=1.6mA V_{CC}=3.5V to 5.5V	
							I_{OL}=0.4mA	
Input/Output Leakage Current	$\|I_{IL}\|$	R4-R8, $R9_1$-$R9_3$	–	–	1	μA	V_{in}=0V to V_{CC}	1
		$R9_0$	–	–	20	μA	V_{in}=0V to V_{CC}	

Note: 1. Output buffer current are excluded.

Input/Output Characteristics for High Voltage Pins

(V_{CC} = 3 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	D_0-D_{15},RA, R0-R3	0.7 V_{CC}	–	V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_0-D_{15},RA, R0-R3	V_{CC}−40	–	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D_0-D_{15}, R0-R3	V_{CC}−3.0	–	–	V	$-I_{OH}$=15mA V_{CC}=4V to 5.5V	
			V_{CC}−2.0	–	–	V	$-I_{OH}$=10mA V_{CC}=4V to 5.5V	
			V_{CC}−1.0	–	–	V	$-I_{OH}$=4mA	
Output Low Voltage	V_{OL}	D_0-D_{15}, R0-R3	–	–	V_{CC}−37	V	150kΩ to V_{CC}−40V	
Input/Output Leakage Current	$\|I_{IL}\|$	D_0-D_{15},RA, R0-R3	–	–	20	μA	V_{in}=V_{CC}−40V to V_{CC}	1

Note: 1. Output buffer current are excluded.

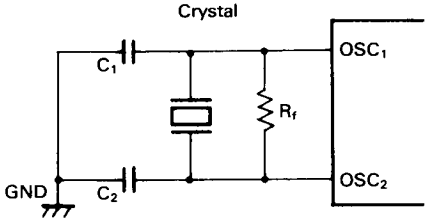
AC Characteristics

(V_{CC} = 3 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Oscillation Frequency Divide-by-4	f_{OSC}	OSC_1,OSC_2	0.4	4	4.5	MHz	V_{CC}=3.5 to 5.5V	7
			1.6	4	4.5	MHz		
			0.4	2	2.25	MHz		7
			1.6	2	2.25	MHz		
Oscillation Frequency (Divide-by-8)	f_{CL}	CL_1,CL_2	–	32.768	–	kHz		
Instruction Cycle Time	t_{cyc}		0.89	1	10	μs	V_{CC}=3.5 to 5.5V	7
			0.89	1	2.5	μs		
			1.78	2	10	μs		7
			1.78	2	2.5	μs		
Instruction Cycle Time	t_{SUBcyc}		–	244.14	–	μs		
Oscillation Stabilization (Crystal)	t_{RC}	OSC_1,OSC_2	–	–	40	ms	V_{CC}=3.5 to 5.5V	1
			–	–	60	ms		1
Oscillation Stabilization (Ceramic Filter)	t_{RC}	OSC_1,OSC_2	–	–	20	ms	V_{CC}=3.5 to 5.5V	1
			–	–	60	ms		1
Oscillation Stabilization	t_{RC}	CL_1,CL_2	–	–	2	s		2
External Clock High, Low Level Width	t_{CPH}, t_{CPL}	OSC_1	92	–	–	ns	V_{CC}=3.5 to 5.5V	3
			203	–	–	ns		3
External Clock Rising, Falling Time	t_{CPr}, t_{CPf}	OSC_1	–	–	20	ns	V_{CC}=3.5 to 5.5V	3
			–	–	20	ns		3
$\overline{INT_0}$ High, Low Level Width	t_{IOH}, t_{IOL}	$\overline{INT_0}$	2	–	–	t_{cyc}/ t_{SUBcyc}		4,6
$\overline{INT_1}$ High, Low Level Width	t_{I1H}, t_{I1L}	$\overline{INT_1}$-$\overline{INT_3}$	2	–	–	t_{cyc}		4
RESET High Level Width	t_{RSTH}	RESET	2	–	–	t_{cyc}		5
Input Capacitance	C_{in}	Except $R9_0$	–	–	30	pF	f=1MHz,V_{in}=0V	
		$R9_0$	–	–	180	pF	f=1MHz,V_{in}=0V	
RESET Falling Time	t_{RSTf}	RESET	–	–	20	ms		5

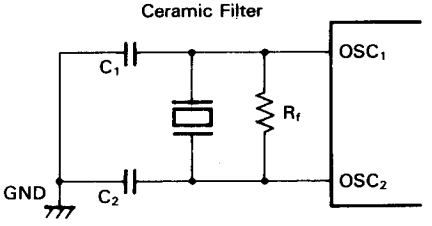
Notes: 1. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V (3.5V, in case of V_{CC}=3.5V-5.5V) after Power on, or after RESET goes high. RESET must be kept high for at least t_{RC} to obtain oscillation time.
Oscillation stabilization time depends on the crystal or ceramic filter's circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal or ceramic filter marker to determine the circuit parameter.

Crystal

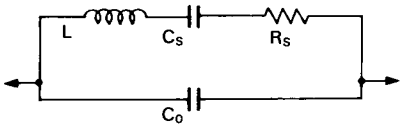


Xtal: Under the equivalent circuit
R_f: 1MΩ ±20%
C_1: 10pF±20%
C_2: 10pF±20%

Ceramic Filter

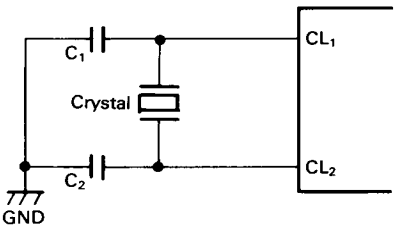


Ceramic Filter: CSA4.00MG (MURATA)
R_f: 1MΩ ±20%
C_1: 30pF±20%
C_2: 30pF±20%

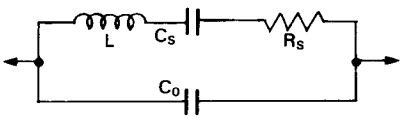


C_0=7pF max
R_S=100Ω max
f =1.0−4.5MHz

2. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V after power on.
Oscillation stabilization time depends on the crystal circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal maker to determine the circuit parameter.



Xtal: MX38T (Nihon denpa kogyo)
Right the equivalent circuit
C_1: 15pF±5%
C_2: 15pF±5%



C_0=1.5pF typ
R_S=14kΩ typ
f =32.768kHz

3. See figure 53.
4. See figure 54. Unit t_{cyc} is applied when MCU is Standby or Active mode.
5. See figure 55.
6. See figure 54. Unit t_{SUBcyc} is applied when MCU is in Watch or Sub-Active mode.
t_{SUBcyc}=244.14μs (When using 32.768kHz crystal oscillator)
7. Apply the data in parenthesis when subsystem oscillator is not used.

Serial Interface Timing Characteristics

(V_{CC} = 3 V to 5.5 V, GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20 to + 75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	1	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	80	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t_{SCKHD}	$\overline{SCK}$	1	–	–	t_{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{cyc}		1
Input Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	80	ns		1
Serial Output Data Delay Time	t_{DSO}	SO	–	–	600	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t_{SSI}	SI	200	–	–	ns		1
Serial Input Data Hold Time	t_{HSI}	SI	400	–	–	ns		1

Notes: 1. See figure 56.
2. See figure 57.
3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

(V_{CC} = 3.5 V to 5.5 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	1	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	40	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t_{SCKHD}	$\overline{SCK}$	1	–	–	t_{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t_{SCKH}, t_{SCKL}	$\overline{SCK}$	0.4	–	–	t_{cyc}		1
Input Transfer Clock Rising, Falling Time	t_{SCKr}, t_{SCKf}	$\overline{SCK}$	–	–	40	ns		1
Serial Output Data Delay Time	t_{DSO}	SO	–	–	300	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t_{SSI}	SI	100	–	–	ns		1
Serial Input Data Hold Time	t_{HSI}	SI	200	–	–	ns		1

Notes: 1. See figure 55.
2. See figure 56.
3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

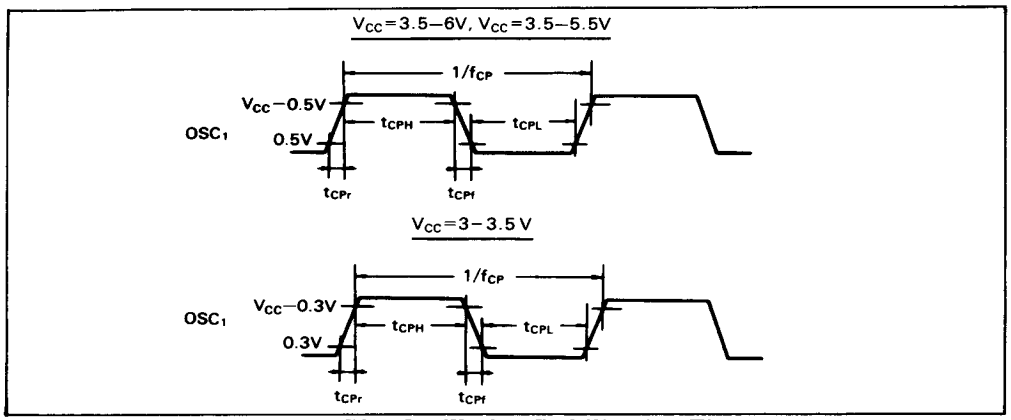


Figure 53. Oscillation Stabilization Time

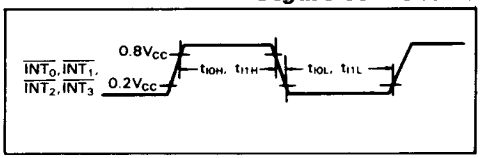


Figure 54. Interrupt Timing

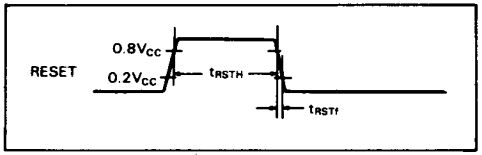


Figure 55. Reset Timing

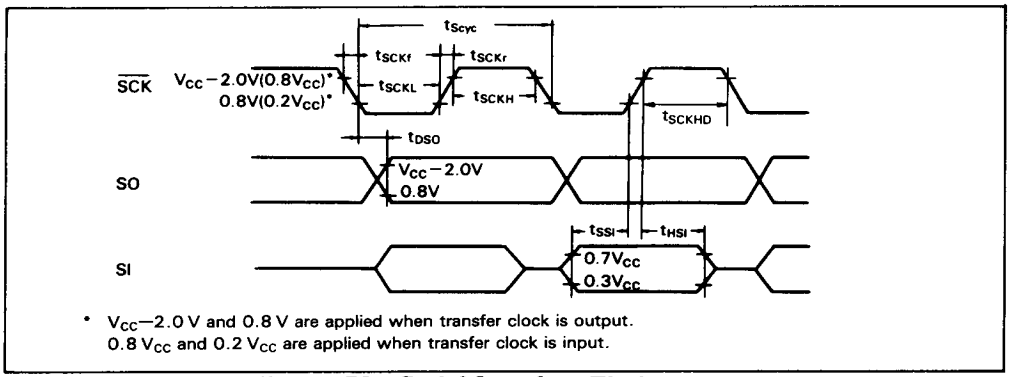


Figure 56. Serial Interface Timing

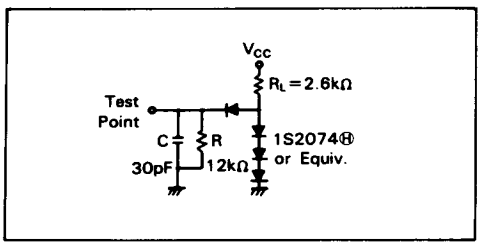


Figure 57. Timing Load Circuit

HD404708/HD404709
Option List

Order date	
Company name	
Department	
Name	
ROM code	
LSI type	HD40470

* Please enter check marks in ☐, for example ■, x or ✓.

(1) ROM size

☐ HD404708
☐ HD404709

(2) Package type

☐ DP-64S
☐ FP-64B

(3) Optional Function

☐ 32kHz CPU operation
☐ no 32kHz CPU operation

(4) ZTAT compatibility

☐ I/O circuit compatibility with the HD4074709
☐ No I/O circuit compatibility with the HD4074709

(5) ROM media

☐ EPROM: emulator type
☐ HD4074709

(Note) ZTAT comapatibility is enabled only when all pins use C or D type circuit. In this case do not check the list item (6) and (7).

(6) I/O option (I/O options masked by ▨ are not available)

Pin name		I/O		I/O option B	C	D	E
D_0		High-voltage pins	I/O				
D_1			I/O				
D_2			I/O				
D_3			I/O				
D_4			I/O				
D_5			I/O				
D_6			I/O				
D_7			I/O				
D_8			I/O				
D_9			I/O				
D_{10}			I/O				
D_{11}			I/O				
D_{12}			I/O				
D_{13}			I/O				
D_{14}			I/O				
D_{15}			I/O				
R0	$R0_0$		I/O				
	$R0_1$		I/O				
	$R0_2$		I/O				
	$R0_3$		I/O				
R1	$R1_0$		I/O				
	$R1_1$		I/O				
	$R1_2$		I/O				
	$R1_3$		I/O				
R2	$R2_0$		I/O				
	$R2_1$		I/O				
	$R2_2$		I/O				
	$R2_3$		I/O				

Pin name		I/O		I/O option B	C	D	E
R3	$R3_0$	High-voltage pins	I/O				
	$R3_1$		I/O				
	$R3_2$		I/O				
	$R3_3$		I/O				
R4	$R4_0$	Standard pins	I/O				
	$R4_1$		I/O				
	$R4_2$		I/O				
	$R4_3$		I/O				
R5	$R5_0$		I/O				
	$R5_1$		I/O				
	$R5_2$		I/O				
	$R5_3$		I/O				
R6	$R6_0$		I/O				
	$R6_1$		I/O				
	$R6_2$		I/O				
	$R6_3$		I/O				
R7	$R7_0$		I/O				
	$R7_1$		I/O				
	$R7_2$		I/O				
	$R7_3$		I/O				
R8	$R8_0$		I/O				
	$R8_1$		I/O				
R9	$R9_0$		I				
	$R9_1$		I				
	$R9_2$		I				
	$R9_3$		I				
RA	RA_0	High-voltage pins	I				
	RA_1		I	Check (7)			

Check I/O option you select.
B: with pull-up MOS C: without pull-up MOS
D: without pull-down MOS E: with pull-down MOS

(7) RA_1/V_{disp}

☐ RA_1: without pull-down MOS (D)
☐ V_{disp}

Note: RA_1/V_{disp} has to be selected as V_{disp} pin exept the case that all high voltage pins are option D.

Condition

(1) OSC_1 and OSC_2 oscillator

☐ Ceramic filter	f=	MHz
☐ Crystal	f=	MHz
☐ External clock	f=	MHz

(2) CL_1 and CL_2 oscillator

☐ Not used	—
☐ Crystal	f=32.768 kHz