# HD404328 Series

## Description

The HD404328 Series is an HMCS400-Series microcomputer designed to increase program productivity and also to incorporate large-capacity memory. Each microcomputer has an LCD controller/driver, A/D converter, and zero-crossing detection circuit. Each also has a 32.768-kHz oscillator and low-power dissipation modes.

The HD404328 Series includes four chips: the HD404328 and HD404328U with 8-kword ROM; the HD4074329 and HD4074329U with 16-kword PROM. The HD404328U and HD4074329U are designed to reduce current dissipation in subactive mode and watch mode.

The HD4074329 and HD4074329U, which include PROM, are ZTAT™ microcomputers that can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

## Features

- 8,192-word × 10-bit ROM (HD404328, HD404328U)
  16,384-word × 10-bit PROM (HD4074329, HD4074329U)
- 280-digit × 4-bit RAM (HD404328, HD404328U)
  536-digit × 4-bit RAM (HD4074329, HD4074329U)
- 35 I/O pins
  — 2 input pins
  — 33 input/output pins, including 8 high-current pins (15 mA, max.) and 16 pins multiplexed with LCD segment pins
- Three timer/counters
- 8-bit clock-synchronous serial interface
- 8-bit × 4-channel A/D converter
- 12-digit LCD controller/driver (24 SEG × 4 COM) (HD404328U, HD4074329U: External LCD voltage division resistors are required)
- Zero-crossing detection circuit
- Eight interrupt sources
  — Two external sources, including one double-edge function
  — Six internal sources
- Subroutine stack
  — Up to 16 levels, including interrupts
- Four low-power dissipation modes
  — Subactive mode
  — Standby mode
  — Watch mode
  — Stop mode
- Built-in oscillator
  — Crystal or ceramic oscillator (external clock also enabled)
  — 32.768 kHz crystal subclock
- Instruction cycle time: 2 μs ($f_{OSC}$ = 4 MHz)
- Two operating modes
  — MCU mode
  — PROM mode (HD4074329, HD4074329U)

## Ordering Information

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|------|-------------|------------|-------------|--------------|---------|
| Mask ROM | HD404328 | HD404328S | 8,192 | 280 | DP-64S |
| | | HD404328FS | | | FP-64B |
| | | HD404328H | | | FP-64A |
| | HD404328U | HD404328US | | | DP-64S |
| | | HD404328UFS | | | FP-64B |
| | | HD404328UH | | | FP-64A |
| ZTAT™ | HD4074329 | HD4074329S | 16,384 | 536 | DP-64S |
| | | HD4074329FS | | | FP-64B |
| | | HD4074329C | | | DC-64S* |
| | HD4074329U | HD4074329US | | | DP-64S |
| | | HD4074329UFS | | | FP-64B |

Note: * Available as a sample.

## Pin Arrangement

**DP-64S / DC-64S**

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | $V_1$ | | 64 | $V_{CC}$ |
| 2 | $V_2$ | | 63 | COM4 |
| 3 | $V_3$ | | 62 | COM3 |
| 4 | $AV_{CC}$ | | 61 | COM2 |
| 5 | $AN_0$ | | 60 | COM1 |
| 6 | $AN_1$ | | 59 | SEG24 |
| 7 | $AN_2$ | | 58 | SEG23 |
| 8 | $AN_3$ | | 57 | SEG22 |
| 9 | $AV_{SS}$ | | 56 | SEG21 |
| 10 | $\overline{TEST}$ | | 55 | SEG20 |
| 11 | $OSC_1$ | | 54 | SEG19 |
| 12 | $OSC_2$ | | 53 | SEG18 |
| 13 | RESET | | 52 | SEG17 |
| 14 | X1 | | 51 | $R5_3/SEG16$ |
| 15 | X2 | | 50 | $R5_2/SEG15$ |
| 16 | GND | | 49 | $R5_1/SEG14$ |
| 17 | $D_0$ | | 48 | $R5_0/SEG13$ |
| 18 | $D_1$ | | 47 | $R4_3/SEG12$ |
| 19 | $D_2$ | | 46 | $R4_2/SEG11$ |
| 20 | $D_3$ | | 45 | $R4_1/SEG10$ |
| 21 | $D_4$ | | 44 | $R4_0/SEG9$ |
| 22 | $D_5$ | | 43 | $R3_3/SEG8$ |
| 23 | $D_6$ | | 42 | $R3_2/SEG7$ |
| 24 | $D_7$ | | 41 | $R3_1/SEG6$ |
| 25 | * | | 40 | $R3_0/SEG5$ |
| 26 | $D_9/\overline{INT_0}$ | | 39 | $R2_3/SEG4$ |
| 27 | $D_{10}/\overline{INT_1}$ | | 38 | $R2_2/SEG3$ |
| 28 | $R0_0$ | | 37 | $R2_1/SEG2$ |
| 29 | $R0_1$ | | 36 | $R2_0/SEG1$ |
| 30 | $R0_2$ | | 35 | $R1_3/BUZZ$ |
| 31 | $R0_3$ | | 34 | $R1_2/SO$ |
| 32 | $R1_0/\overline{SCK}$ | | 33 | $R1_1/SI$ |

**FP-64B**

Top row (64–52): $AN_1$, $AN_0$, $AV_{CC}$, $V_3$, $V_2$, $V_1$, $V_{CC}$, COM4, COM3, COM2, COM1, SEG24, SEG23

Left side (1–19): $AN_2$ (1), $AN_3$ (2), $AV_{SS}$ (3), $\overline{TEST}$ (4), $OSC_1$ (5), $OSC_2$ (6), RESET (7), X1 (8), X2 (9), GND (10), $D_0$ (11), $D_1$ (12), $D_2$ (13), $D_3$ (14), $D_4$ (15), $D_5$ (16), $D_6$ (17), $D_7$ (18), * (19)

Bottom row (20–32): $D_9/\overline{INT_0}$, $D_{10}/\overline{INT_1}$, $R0_0$, $R0_1$, $R0_2$, $R0_3$, $R1_0/\overline{SCK}$, $R1_1/SI$, $R1_2/SO$, $R1_3/BUZZ$, $R2_0/SEG1$, $R2_1/SEG2$, $R2_2/SEG3$

Right side (51–33): SEG22 (51), SEG21 (50), SEG20 (49), SEG19 (48), SEG18 (47), SEG17 (46), $R5_3/SEG16$ (45), $R5_2/SEG15$ (44), $R5_1/SEG14$ (43), $R5_0/SEG13$ (42), $R4_3/SEG12$ (41), $R4_2/SEG11$ (40), $R4_1/SEG10$ (39), $R4_0/SEG9$ (38), $R3_3/SEG8$ (37), $R3_2/SEG7$ (36), $R3_1/SEG6$ (35), $R3_0/SEG5$ (34), $R2_3/SEG4$ (33)

Note: * $D_8/ZCD/\overline{EVENT}$

**FP-64A**

Top row (64–49): $AN_3$, $AN_2$, $AN_1$, $AN_0$, $AV_{CC}$, $V_3$, $V_2$, $V_1$, $V_{CC}$, COM4, COM3, COM2, COM1, SEG24, SEG23, SEG22

Left side (1–16): $AV_{SS}$ (1), $\overline{TEST}$ (2), $OSC_1$ (3), $OSC_2$ (4), RESET (5), X1 (6), X2 (7), GND (8), $D_0$ (9), $D_1$ (10), $D_2$ (11), $D_3$ (12), $D_4$ (13), $D_5$ (14), $D_6$ (15), $D_7$ (16)

Bottom row (17–32): * , $D_9/\overline{INT_0}$, $D_{10}/\overline{INT_1}$, $R0_0$, $R0_1$, $R0_2$, $R0_3$, $R1_0/\overline{SCK}$, $R1_1/SI$, $R1_2/SO$, $R1_3/BUZZ$, $SEG1/R2_0$, $SEG2/R2_1$, $SEG3/R2_2$, $SEG4/R2_3$, $SEG5/R3_0$

Right side (48–33): SEG21 (48), SEG20 (47), SEG19 (46), SEG18 (45), SEG17 (44), $SEG16/R5_3$ (43), $SEG15/R5_2$ (42), $SEG14/R5_1$ (41), $SEG13/R5_0$ (40), $SEG12/R4_3$ (39), $SEG11/R4_2$ (38), $SEG10/R4_1$ (37), $SEG9/R4_0$ (36), $SEG8/R3_3$ (35), $SEG7/R3_2$ (34), $SEG6/R3_1$ (33)

(top view)

## Pin Description

| Item | Symbol | DP-64S DC-64S | FP-64B | FP-64A | I/O | Function |
|---|---|---|---|---|---|---|
| Power supply | $V_{CC}$ | 64 | 58 | 56 | | Applies power voltage |
| | GND | 16 | 10 | 8 | | Connected to ground |
| Test | TEST | 10 | 4 | 2 | I | Used for factory testing only; connect this pin to $V_{CC}$ |
| Reset | RESET | 13 | 7 | 5 | I | Resets the MCU |
| Oscillator | $OSC_1$ | 11 | 5 | 3 | I | Input/output pins for the internal oscillator circuit; connect them to a crystal, ceramic, or external oscillator circuit |
| | $OSC_2$ | 12 | 6 | 4 | O | |
| | X1 | 14 | 8 | 6 | I | Used for a 32.768-kHz crystal for clock purposes; if not used, fix X1 to $V_{CC}$ and leave X2 open |
| | X2 | 15 | 9 | 7 | O | |
| Port | $D_0–D_8$ | 17–25 | 11–19 | 9–17 | I/O | Input/output ports addressed by individual bits; pins $D_0–D_7$ are high-current pins that can each supply up to 15 mA |
| | $D_9, D_{10}$ | 26, 27 | 20, 21 | 18, 19 | I | Input ports addressable by individual bits |
| | $R0_0–R5_3$ | 28–51 | 22–45 | 20–43 | I/O | Input/output ports addressable in 4-bit units |
| Interrupt | $INT_0, INT_1$ | 26, 27 | 20, 21 | 18, 19 | I | Input pins for external interrupts |
| Serial interface | SCK | 32 | 26 | 24 | I/O | Serial interface clock input/output pin |
| | SI | 33 | 27 | 25 | I | Serial interface receive data input pin |
| | SO | 34 | 28 | 26 | O | Serial interface transmit data output pin |
| Buzzer | BUZZ | 35 | 29 | 27 | O | Buzzer signal output pin |
| LCD | $V_1, V_2, V_3$ | 1–3 | 59–61 | 57–59 | | Power pins for LCD driver; can be left open in operation because they are connected by internal voltage division resistors (except for HD404328U and HD4074329U) Voltage conditions are: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ |
| | COM1–COM4 | 60–63 | 54–57 | 52–55 | O | Common signal pins for LCD |
| | SEG1–SEG24 | 36–59 | 30–53 | 28–51 | O | Segment signal pins for LCD |
| A/D converter | $AV_{CC}$ | 4 | 62 | 60 | | Power pin for A/D converter; connect it to the same potential as $V_{CC}$, as physically close as possible to the power source |
| | $AV_{SS}$ | 9 | 3 | 1 | | Ground for $AV_{CC}$; connect it to the same potential as GND, as physically close as possible to the power source |
| | $AN_0–AN_3$ | 5–8 | 63, 64, 1, 2 | 61–64 | I | Analog input pins for 4-channel A/D converter |
| Zero-crossing detection | ZCD | 25 | 19 | 17 | I | Zero-crossing detection input pin |
| Counter | EVENT | 25 | 19 | 17 | I | Event count input pin |

## Block Diagram

700 Hitachi
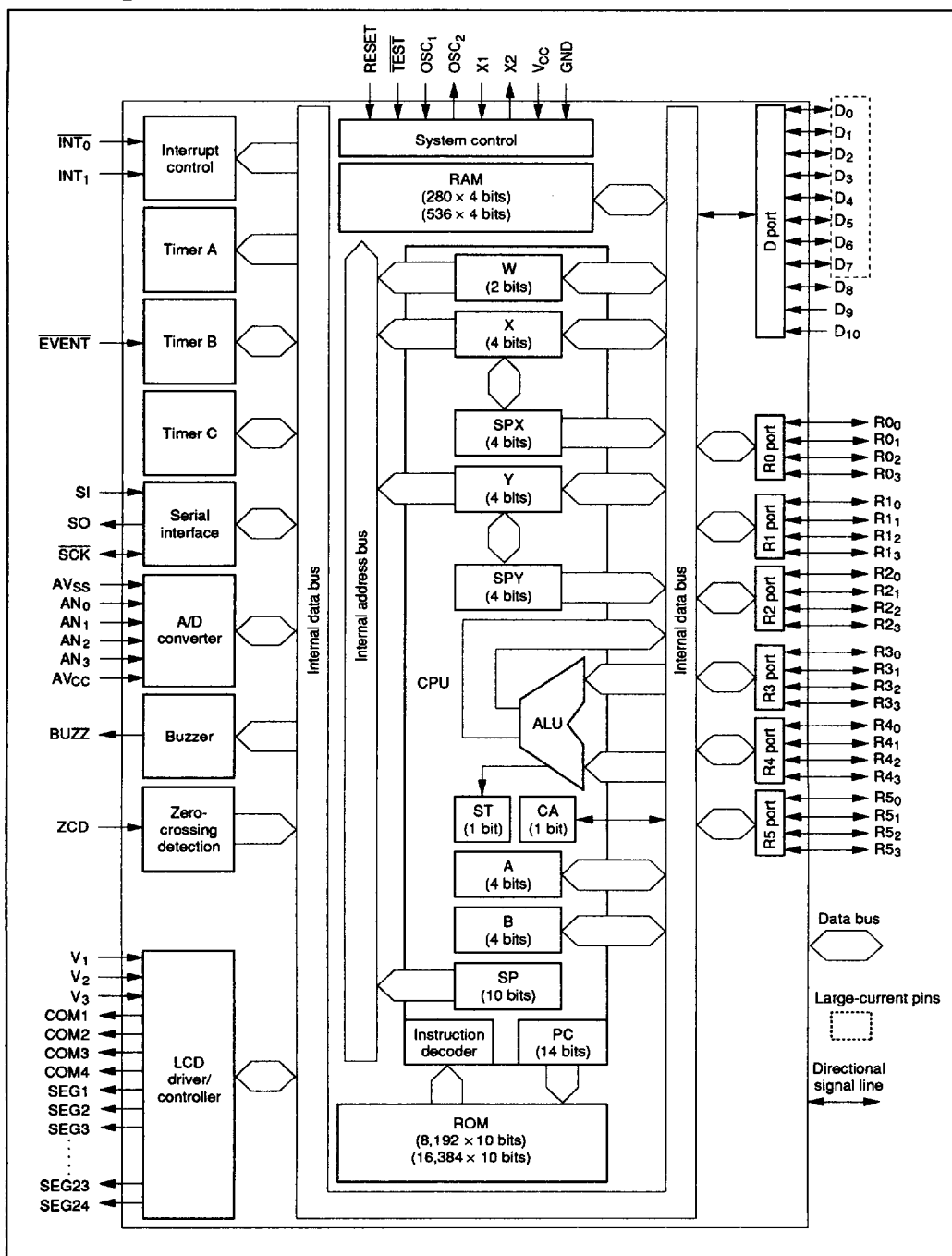
# Memory Map

## ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

**Vector Address Area ($0000–$000F):** Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

**Zero-Page Subroutine Area ($0000–$003F):** Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

**Pattern Area ($0000–$0FFF):** Contains ROM data that can be referenced with the P instruction.

**Program Area (HD404328, HD404328U: $0000–$1FFF, HD4074329, HD4074329U: $0000–$3FFF):** Used for program coding.

## RAM Memory Map

The MPU contains a 280-digit × 4-bit (HD404328, HD404328U) or 536-digit × 4-bit (HD4074329, HD4074329U) RAM area consisting of a data area and a stack area. In addition, interrupt control bits and special registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and described below.
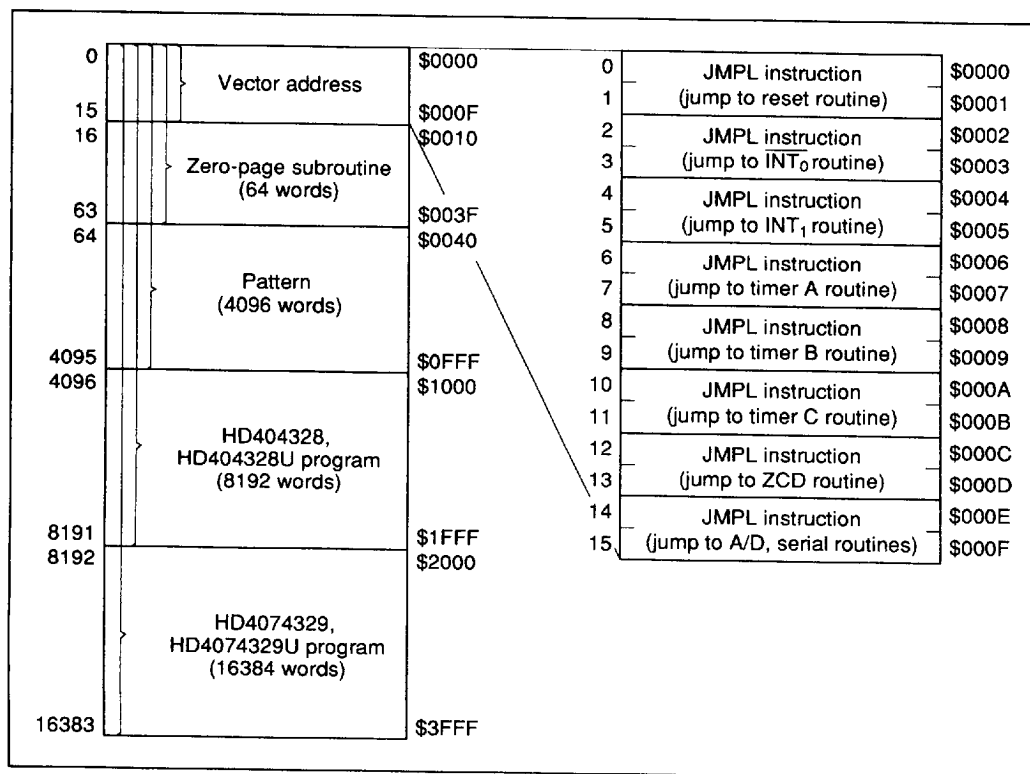


**Figure 1   ROM Memory Map**

**Interrupt Control Bits Area and Register Flag Area ($000–$003, $020–$023):** Used for interrupt control bits and the bit register (figure 3). This area can be accessed only by RAM bit manipulation instructions. In addition, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer, and the WDON flag can be set only by the SEM and SEMD instructions.

**Special Function Registers Area ($004–$01F, $024–$03F):** Used as mode registers for external interrupts, serial interface, and timer/counters, and as data registers and as data control registers for I/O ports. As shown in figure 2, these registers can be classified into three types: write-only, read-only, and read/write. The SEM, SEMD, REM, and REMD instructions can be used for the LCD control register (LCR), but RAM bit manipulation instructions cannot be used for other registers.

**LCD Data Area ($050–$067):** Used for storing LCD data which is automatically output to LCD segments as display data. Data 1 lights the corresponding LCD segment; data 0 extinguishes it.

**Data Area (HD404328, HD404328U: $040–$04F and $070–$11F, HD4074329, HD4074329U: $040–$04F and $070–$21F):** The memory registers (MR), which consist of 16 digits ($040–$04F), can be accessed by the LAMR and XMRA instructions. Its structure is shown in figure 4.

**Stack Area ($3C0–$3FF):** Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine calls (CAL, CALL) and interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 4.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

| | RAM-mapped registers (64 digits) | |
|---|---|---|
| 0 | | $000 |
| 63 | | $03F |
| 64 | Memory registers (MR) (16 digits) | $040 |
| 79 | | $04F |
| 80 | LCD display area (24 digits) | $050 |
| 103 | | $067 |
| 104 | Not used | $068 |
| 111 | | $06F |
| 112 | Data (176 digits) | $070 |
| 287 | | $11F |
| 288 | Data (256 digits) | $120 |
| 543 | | $21F |
| 544 | Not used | $220 |
| 959 | | $3BF |
| 960 | Stack (64 digits) | $3C0 |
| 1023 | | $3FF |

Shaded area can only be used by the HD4074329, and HD4074329U

R: Read only
W: Write only
R/W: Read/write

Note: * Two registers mapped on the same area

| | | | | |
|---|---|---|---|---|
| 0 | Interrupt control bits area | | | $000 |
| 1 | | | | $001 |
| 2 | | | | $002 |
| 3 | | | | $003 |
| 4 | Port mode register A | (PMRA) | W | $004 |
| 5 | Serial mode register | (SMR) | W | $005 |
| 6 | Serial data register, lower | (SRL) | R/W | $006 |
| 7 | Serial data register, upper | (SRU) | R/W | $007 |
| 8 | Timer mode register A | (TMA) | W | $008 |
| 9 | Timer mode register B | (TMB) | W | $009 |
| 10 | *Timer B | (TCBL/TLRL) | R/W | $00A |
| 11 | | (TCBU/TLRU) | R/W | $00B |
| 12 | Miscellaneous register | (MIS) | W | $00C |
| 13 | Timer mode register C | (TMC) | W | $00D |
| 14 | *Timer C | (TCCL/TCRL) | R/W | $00E |
| 15 | | (TCCU/TCRU) | R/W | $00F |
| 16 | Interrupt mode register | (IMR) | W | $010 |
| 17 | Port mode register B | (PMRB) | W | $011 |
| 18 | Port mode register C | (PMRC) | W | $012 |
| 19 | LCD control register | (LCR) | W | $013 |
| 20 | LCD mode register | (LMR) | W | $014 |
| 21 | LCD output register | (LOR) | W | $015 |
| 22 | A/D mode register | (AMR) | W | $016 |
| 23 | A/D data register, lower | (ADRL) | R | $017 |
| 24 | A/D data register, upper | (ADRU) | R | $018 |
| | Not used | | | |
| 32 | Register flag area | | | $020 |
| 35 | | | | $023 |
| | Not used | | | |
| 48 | Port R0 DCR | (DCR0) | W | $030 |
| 49 | Port R1 DCR | (DCR1) | W | $031 |
| 50 | Port R2 DCR | (DCR2) | W | $032 |
| 51 | Port R3 DCR | (DCR3) | W | $033 |
| 52 | Port R4 DCR | (DCR4) | W | $034 |
| 53 | Port R5 DCR | (DCR5) | W | $035 |
| | Not used | | | |
| 59 | Port $D_0$–$D_3$ DCR | (DCRB) | W | $03B |
| 60 | Port $D_4$–$D_7$ DCR | (DCRC) | W | $03C |
| 61 | Port $D_8$ DCR | (DCRD) | W | $03D |
| 62 | Not used | | | $03E |
| 63 | | | | $03F |

| | | | | |
|---|---|---|---|---|
| Timer/event counter B, lower (TCBL) | R | Timer load register B, lower (TLRL) | W | $00A |
| Timer/event counter B, upper (TCBU) | R | Timer load register B, upper (TLRU) | W | $00B |
| Timer counter C, lower (TCCL) | R | Timer load register C, lower (TCRL) | W | $00E |
| Timer counter C, upper (TCCU) | R | Timer load register C, upper (TCRU) | W | $00F |

**Figure 2   RAM Memory Map**

|  | Bit 3 | Bit 2 | Bit 1 | Bit 0 |  |
|---|---|---|---|---|---|
| 0 | IM0 (IM of $\overline{INT_0}$) | IF0 (IF of $\overline{INT_0}$) | RSP (Reset SP bit) | IE (Interrupt enable flag) | $000 |
| 1 | IMTA (IM of timer A) | IFTA (IF of timer A) | IM1 (IM of $INT_1$) | IF1 (IF of $INT_1$) | $001 |
| 2 | IMTC (IM of timer C) | IFTC (IF of timer C) | IMTB (IM of timer B) | IFTB (IF of timer B) | $002 |
| 3 | IMAD (IM of A/D) | IFAD (IF of A/D) | IMZC (IM of ZCD) | IFZC (IF of ZCD) | $003 |

|  | Bit 3 | Bit 2 | Bit 1 | Bit 0 |  |
|---|---|---|---|---|---|
| 32 | DTON (Direct transfer on flag) | ADSF (A/D start flag) | WDON (Watchdog on flag) | LSON (Low speed on flag) | $020 |
| 33 | Not used | | | | $021 |
| 34 | | | | | $022 |
| 35 | IMS (IM of serial interface) | IFS (IF of serial interface) | | | $023 |

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
However, note the following usage limitations of RAM bit manipulation instructions.

|  | SEM/SEMD | REM/REMD | TM/TMD |
|---|---|---|---|
| IF | Not executed | Allowed | Allowed |
| RSP | Not executed | Allowed | Inhibited |
| WDON | Allowed | Not executed | Inhibited |
| DTON | Not executed in active mode | Allowed | Allowed |
|  | Used in subactive mode | | |

Note: WDON is reset by MCU reset.
DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

**Figure 3   Configuration of Interrupt Control Bits and Register Flag Areas**

Memory registers

| | | |
|---|---|---|
| 64 | MR (0) | $040 |
| 65 | MR (1) | $041 |
| 66 | MR (2) | $042 |
| 67 | MR (3) | $043 |
| 68 | MR (4) | $044 |
| 69 | MR (5) | $045 |
| 70 | MR (6) | $046 |
| 71 | MR (7) | $047 |
| 72 | MR (8) | $048 |
| 73 | MR (9) | $049 |
| 74 | MR (10) | $04A |
| 75 | MR (11) | $04B |
| 76 | MR (12) | $04C |
| 77 | MR (13) | $04D |
| 78 | MR (14) | $04E |
| 79 | MR (15) | $04F |

Stack area

| | | |
|---|---|---|
| 960 | Level 16 | $3C0 |
| | Level 15 | |
| | Level 14 | |
| | Level 13 | |
| | Level 12 | |
| | Level 11 | |
| | Level 10 | |
| | Level 9 | |
| | Level 8 | |
| | Level 7 | |
| | Level 6 | |
| | Level 5 | |
| | Level 4 | |
| | Level 3 | |
| | Level 2 | |
| 1023 | Level 1 | $3FF |

| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---|---|---|---|---|---|
| 1020 | ST | $\overline{PC_{13}}$ | $\overline{PC_{12}}$ | $\overline{PC_{11}}$ | $3FC |
| 1021 | $\overline{PC_{10}}$ | $\overline{PC_9}$ | $\overline{PC_8}$ | $\overline{PC_7}$ | $3FD |
| 1022 | CA | $\overline{PC_6}$ | $\overline{PC_5}$ | $\overline{PC_4}$ | $3FE |
| 1023 | $\overline{PC_3}$ | $\overline{PC_2}$ | $\overline{PC_1}$ | $\overline{PC_0}$ | $3FF |

$PC_{13}$–$PC_0$: Program counter
ST: Status flag
CA: Carry flag

**Figure 4   Configuration of Memory Registers and Stack Area, and Stack Position**

## Functional Description

### Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 5 and described below.

**Accumulator (A), B Register (B):** Four-bit registers used to hold results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

**W Register (W), X Register (X), Y Register (Y):** Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

**SPX Register (SPX), SPY Register (SPY):** Four-bit registers used to supplement the X and Y registers.

**Carry Flag (CA):** One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.
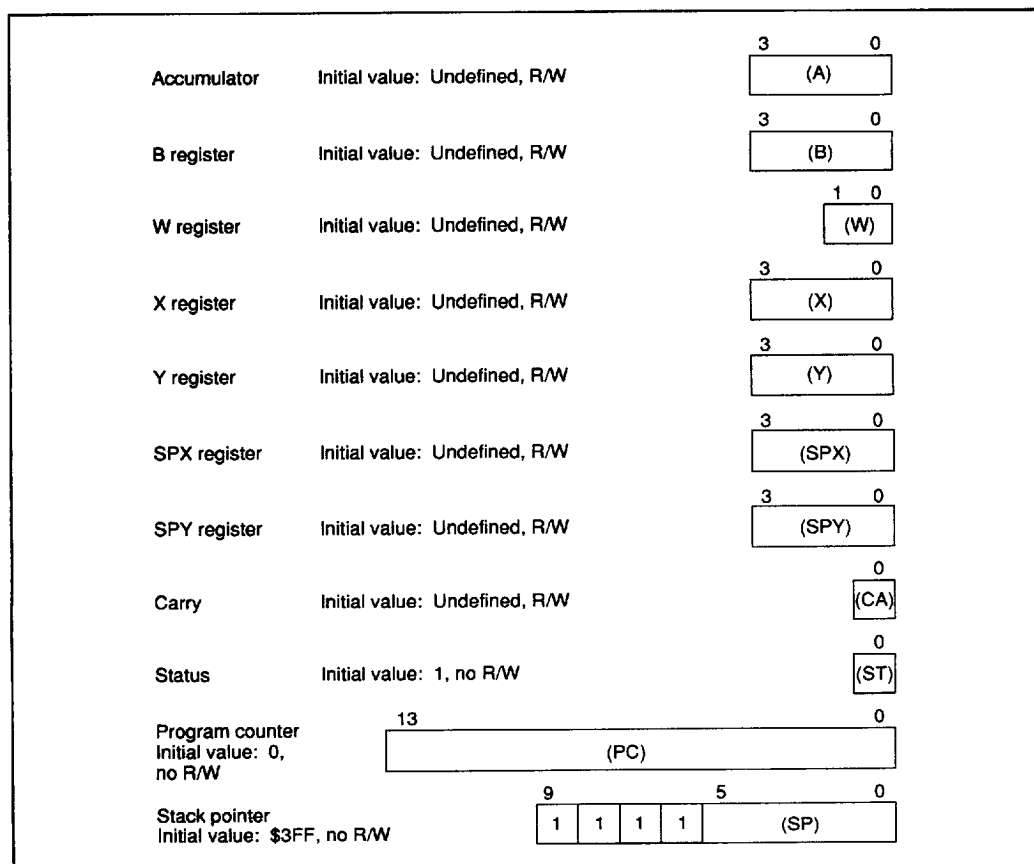


**Figure 5  Registers and Flags**

**Status Flag (ST):** One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

**Program Counter (PC):** A 14-bit counter that points to the ROM address of the instruction being executed.

**Stack Pointer (SP):** Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top four bits of the SP are fixed at 1111, a stack of up to 16 levels can be used.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

### Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power-on or when stop mode is cancelled, RESET must be high for at least one $t_{RC}$ to enable the oscillator to stabilize. During operation, RESET must be high for at least two instruction cycles.

Initial values after MCU reset are shown in table 1.

### Interrupts

The MCU has eight interrupt sources: two external signals ($\overline{INT_0}$ and $INT_1$), three timer/counters (timer A, timer B, and timer C), serial interface, zero-crossing detection, and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Vector addresses are shared by serial interface and A/D converter interrupt causes, so software must first check which type of request has occurred.

**Interrupt Control Bits and Interrupt Servicing:** Locations $000–$003 and $020–$023 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 6, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the eight interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. Priority control logic generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 7 and an interrupt processing flowchart is shown in figure 8. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

# HD404328 Series

## Table 1   Initial Values After MCU Reset

| Item | | Abbr. | Initial Value | Contents |
|---|---|---|---|---|
| Program counter | | (PC) | $0000 | Indicates program execution point from start address of ROM area |
| Status flag | | (ST) | 1 | Enables conditional branching |
| Stack pointer | | (SP) | $3FF | Stack level 0 |
| Interrupt flags/mask | Interrupt enable flag | (IE) | 0 | Inhibits all interrupts |
| | Interrupt request flag | (IF) | 0 | Indicates there is no interrupt request |
| | Interrupt mask | (IM) | 1 | Prevents (masks) interrupt requests |
| I/O | Port data register | (PDR) | All bits 1 | Enables output at level 1 |
| | Data control register | (DCR) | All bits 0 | Turns output buffer off (to high impedance) |
| | Port mode register A | (PMRA) | 0000 | Refer to description of port mode register A |
| | Port mode register B | (PMRB) | 0000 | Refer to description of port mode register B |
| | Port mode register C | (PMRC) | 0000 | Refer to description of port mode register C |
| | Interrupt mode register | (IMR) | 0000 | Refer to description of interrupt mode register |
| Timer/ counters, serial interface | Timer mode register A | (TMA) | 0000 | Refer to description of timer mode register A |
| | Timer mode register B | (TMB) | 0000 | Refer to description of timer mode register B |
| | Timer mode register C | (TMC) | 0000 | Refer to description of timer mode register C |
| | Serial mode register | (SMR) | 0000 | Refer to description of serial mode register |
| | Prescaler S | | $000 | — |
| | Prescaler W | | $00 | — |
| | Timer counter A | (TCA) | $00 | — |
| | Timer counter B | (TCB) | $00 | — |
| | Timer counter C | (TCC) | $00 | — |
| | Timer load register B | (TLR) | $00 | — |
| | Timer load register C | (TCR) | $00 | — |
| | Octal counter | | 000 | — |
| A/D | A/D mode register | (AMR) | 0000 | Refer to description of A/D mode register |
| LCD | LCD control register | (LCR) | 000 | Refer to description of LCD control register |
| | LCD mode register | (LMR) | 0000 | Refer to description of LCD duty cycle/clock control register |
| | LCD output register | (LOR) | 0000 | Refer to description of LCD output register |
| Bit register | Low speed on flag | (LSON) | 0 | Refer to description of low-power dissipation modes |
| | Watchdog timer on flag | (WDON) | 0 | Refer to description of timer C |
| | A/D start flag | (ADSF) | 0 | Refer to description of A/D converter |
| | Direct transfer on flag | (DTON) | 0 | Refer to description of low-power dissipation modes |
| Miscellaneous register | | (MIS) | 0000 | Refer to description of miscellaneous register |

Note:  The statuses of other registers and flags after MCU reset are as follows:

| Item | Abbr. | Status After Cancellation of Stop Mode by MCU Reset | Status After Cancellation of all Other Types of Modes by MCU Reset |
|---|---|---|---|
| Carry flag | (CA) | Pre-MCU-reset values are not guaranteed:  values must be initialized by program | Pre-MCU-reset values are not guaranteed:  values must be initialized by program |
| Accumulator | (A) | | |
| B register | (B) | | |
| W register | (W) | | |
| X/SPX register | (X/SPX) | | |
| Y/SPY register | (Y/SPY) | | |
| Serial data register | (SR) | | |
| A/D data register | (ADRL, ADRU) | | |
| RAM | | Pre-MCU-reset (pre-STOP-instruction) values are retained | |
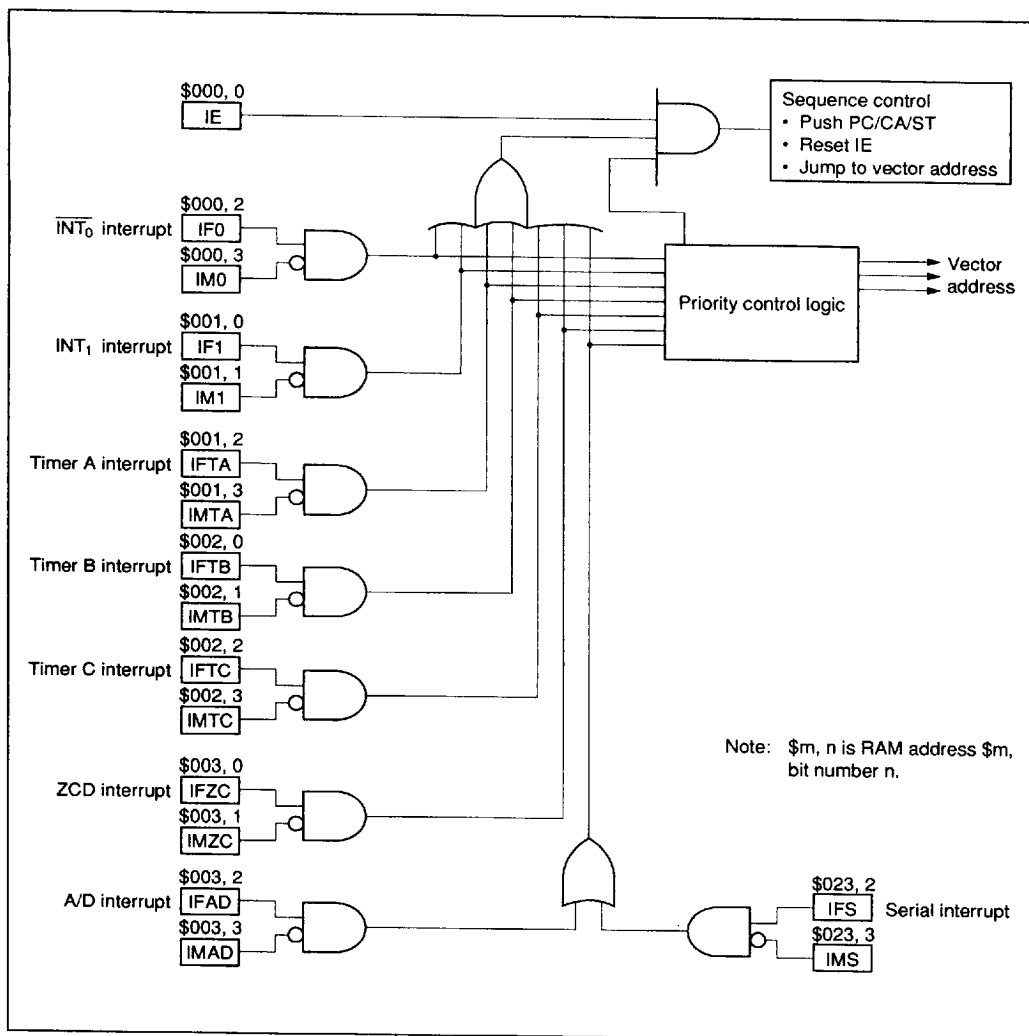
**Figure 6   Block Diagram of Interrupt Control Circuit**

**Table 2   Vector Addresses and Interrupt Priorities**

| Reset/Interrupt | Priority | Vector Address |
|---|---|---|
| RESET | — | $0000 |
| INT$_0$ | 1 | $0002 |
| INT$_1$ | 2 | $0004 |
| Timer A | 3 | $0006 |
| Timer B | 4 | $0008 |
| Timer C | 5 | $000A |
| ZCD | 6 | $000C |
| A/D, Serial | 7 | $000E |

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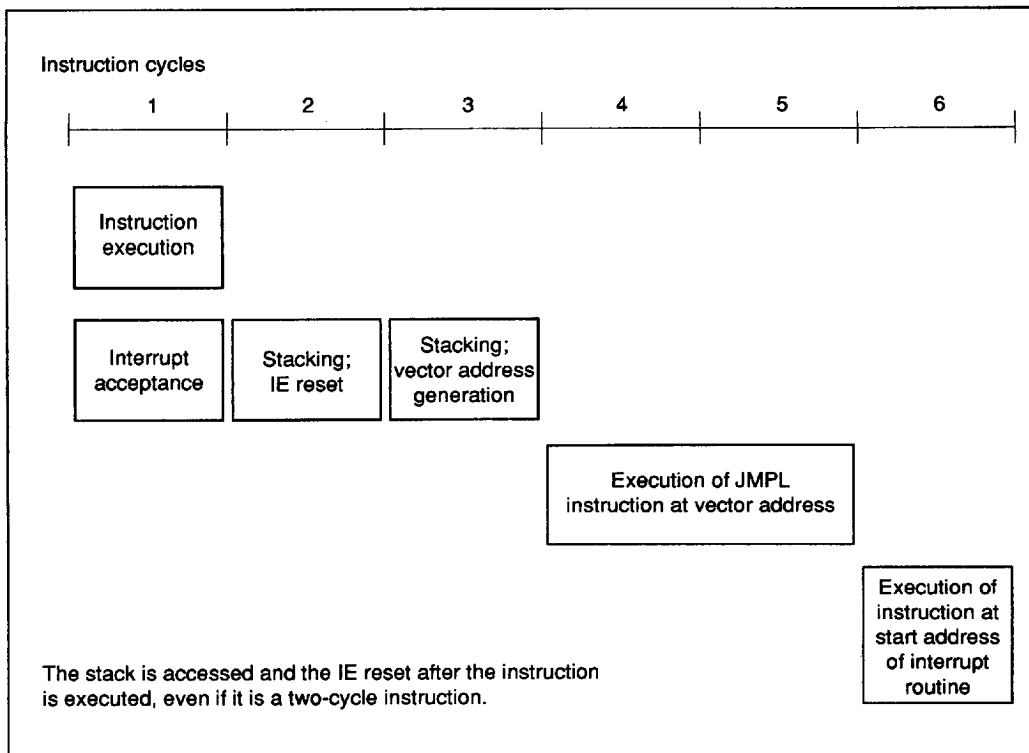
**Figure 7   Interrupt Processing Sequence**

**Table 3   Interrupt Processing and Activation Conditions**

| Interrupt Control Bit | Interrupt Cause | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | $\overline{INT_0}$ | $INT_1$ | Timer A | Timer B | Timer C | ZCD | A/D, Serial |
| IE | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| IF0·$\overline{IM0}$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| IF1·$\overline{IM1}$ | * | 1 | 0 | 0 | 0 | 0 | 0 |
| IFTA·$\overline{IMTA}$ | * | * | 1 | 0 | 0 | 0 | 0 |
| IFTB·$\overline{IMTB}$ | * | * | * | 1 | 0 | 0 | 0 |
| IFTC·$\overline{IMTC}$ | * | * | * | * | 1 | 0 | 0 |
| IFZC·$\overline{IMZC}$ | * | * | * | * | * | 1 | 0 |
| IFAD·$\overline{IMAD}$ + IFS·$\overline{IMS}$ | * | * | * | * | * | * | 1 |

Note:  Bits marked * can be either 0 or 1.  Their values have no effect on operation.
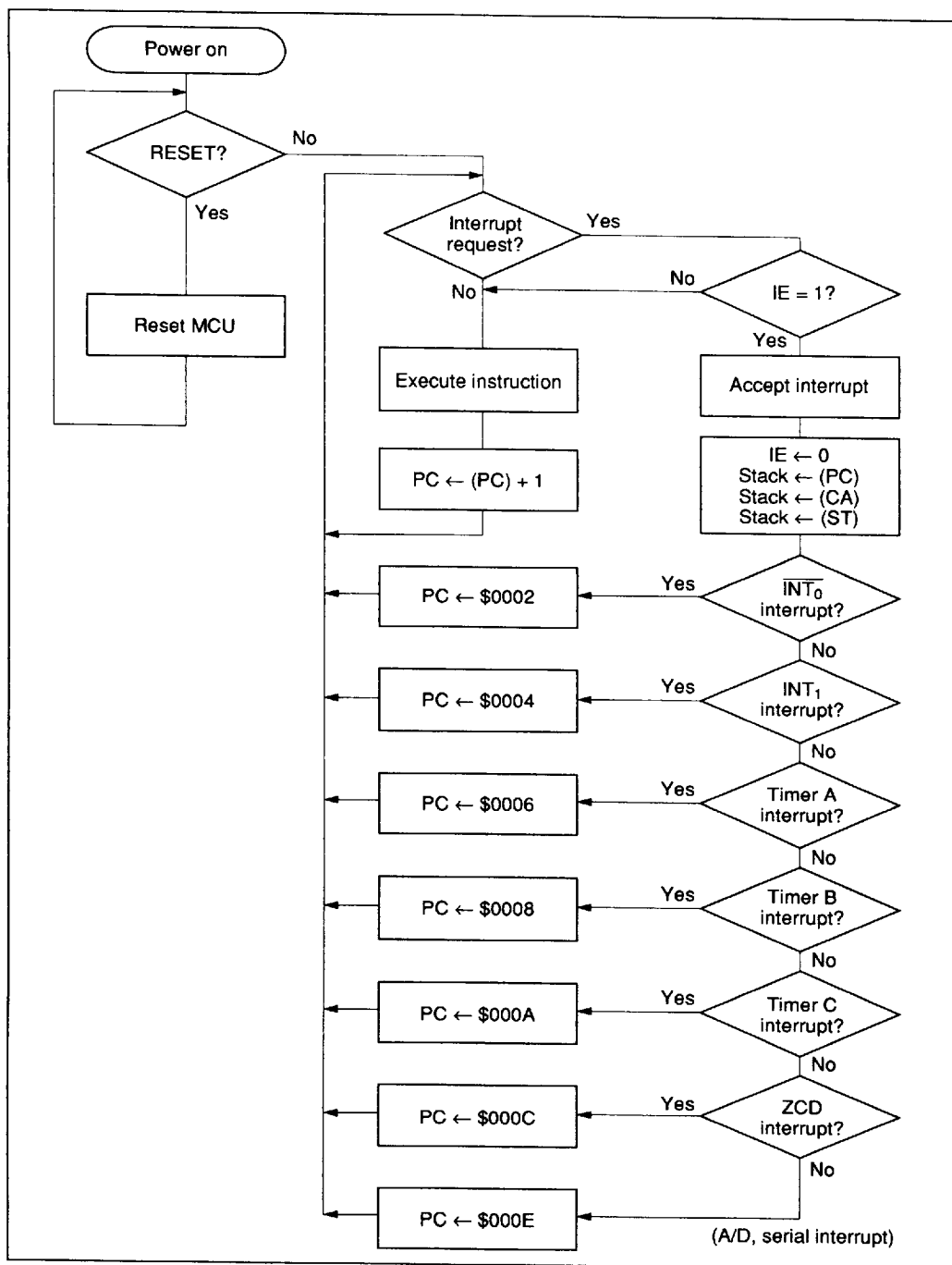
**Figure 8  Interrupt Processing Flowchart**

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**Interrupt Enable Flag (IE: $000, Bit 0):** Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as shown in table 4.

**External Interrupts ($\overline{INT_0}$, $INT_1$):** Specified by port mode register A (PMRA: $004).

**External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0):** Set at the rising or falling edges of the $\overline{INT_0}$ and $INT_1$ inputs, as shown in table 5.

IF0 is set at the falling edge of signals input to $\overline{INT_0}$, and IF1 is set at the rising and falling edges of signals input to $INT_1$. The $INT_1$ interrupt edge is selected by the interrupt mode register (IMR: $010), as shown in figure 9.

**External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1):** Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as shown in table 6.

**Table 4   Interrupt Enable Flag**

| IE | Interrupt Enabled/Disabled |
|----|----------------------------|
| 0  | Disabled                   |
| 1  | Enabled                    |

**Table 6   External Interrupt Masks**

| IM0, IM1 | Interrupt Request  |
|----------|--------------------|
| 0        | Enabled            |
| 1        | Disabled (Masked)  |

**Table 5   External Interrupt Request Flags**

| IF0, IF1 | Interrupt Request |
|----------|-------------------|
| 0        | No                |
| 1        | Yes               |

Interrupt mode register (IMR): $010

| 3 | 2 | 1 | 0 | Initial value: 0000, R/W: W |

$INT_1$ detection edge selection

ZCD detection edge selection

| IMR | | ZCD Detection Edge |
|-----|-----|--------------------|
| Bit 3 | Bit 2 | |
| 0 | 0 | No detection |
| 0 | 1 | Falling-edge detection |
| 1 | 0 | Rising-edge detection |
| 1 | 1 | Double-edge detection |

| IMR | | $INT_1$ Detection Edge |
|-----|-----|------------------------|
| Bit 1 | Bit 0 | |
| 0 | 0 | No detection |
| 0 | 1 | Falling-edge detection |
| 1 | 0 | Rising-edge detection |
| 1 | 1 | Double-edge detection |

**Figure 9   Interrupt Mode Register**

**Timer A Interrupt Request Flag (IFTA: $001, Bit 2):** Set by overflow output from timer A, as shown in table 7.

**Timer A Interrupt Mask (IMTA: $001, Bit 3):** Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as shown in table 8.

**Timer B Interrupt Request Flag (IFTB: $002, Bit 0):** Set by overflow output from timer B, as shown in table 9.

**Timer B Interrupt Mask (IMTB: $002, Bit 1):** Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as shown in table 10.

**Timer C Interrupt Request Flag (IFTC: $002, Bit 2):** Set by overflow output from timer C, as shown in table 11.

**Timer C Interrupt Mask (IMTC: $002, Bit 3):** Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as shown in table 12.

**Zero-Crossing Interrupt Request Flag (IFZC: $003, Bit 0):** Set by a zero crossing of an AC input signal, as shown in table 13. The interrupt edge is selected by the interrupt mode register (IMR: $010), as shown in figure 9.

**Zero-Crossing Interrupt Mask (IMZC: $003, Bit 1):** Prevents (masks) an interrupt request caused by the zero-crossing interrupt request flag, as shown in table 14.

**Table 7   Timer A Interrupt Request Flag**

| IFTA | Interrupt Request |
|------|-------------------|
| 0 | No |
| 1 | Yes |

**Table 8   Timer A Interrupt Mask**

| IMTA | Interrupt Request |
|------|-------------------|
| 0 | Enabled |
| 1 | Disabled (Masked) |

**Table 9   Timer B Interrupt Request Flag**

| IFTB | Interrupt Request |
|------|-------------------|
| 0 | No |
| 1 | Yes |

**Table 10   Timer B Interrupt Mask**

| IMTB | Interrupt Request |
|------|-------------------|
| 0 | Enabled |
| 1 | Disabled (Masked) |

**Table 11   Timer C Interrupt Request Flag**

| IFTC | Interrupt Request |
|------|-------------------|
| 0 | No |
| 1 | Yes |

**Table 12   Timer C Interrupt Mask**

| IMTC | Interrupt Request |
|------|-------------------|
| 0 | Enabled |
| 1 | Disabled (Masked) |

**Table 13   Zero-Crossing Interrupt Request Flag**

| IFZC | Interrupt Request |
|------|-------------------|
| 0 | No |
| 1 | Yes |

**Table 14   Zero-Crossing Interrupt Mask**

| IMZC | Interrupt Request |
|------|-------------------|
| 0 | Enabled |
| 1 | Disabled (Masked) |

**A/D Interrupt Request Flag (IFAD: $003, Bit 2):** Set at the completion of A/D conversion, as shown in table 15.

**A/D Interrupt Mask (IMAD: $003, Bit 3):** Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as shown in table 16.

**Serial Interrupt Request Flag (IFS: $023, Bit 2):** Set when the octal counter counts the eighth transmit clock signal or when data transfer is discontinued by resetting the octal counter (table 17).

**Serial Interrupt Mask (IMS: $023, Bit 3):** Prevents (masks) an interrupt request caused by the serial interrupt request flag, as shown in table 18.

**Table 15   A/D Interrupt Request Flag**

| IFAD | Interrupt Request |
| --- | --- |
| 0 | No |
| 1 | Yes |

**Table 16   A/D Interrupt Mask**

| IMAD | Interrupt Request |
| --- | --- |
| 0 | Enabled |
| 1 | Disabled (Masked) |

**Table 17   Serial Interrupt Request Flag**

| IFS | Interrupt Request |
| --- | --- |
| 0 | No |
| 1 | Yes |

**Table 18   Serial Interrupt Mask**

| IMS | Interrupt Request |
| --- | --- |
| 0 | Enabled |
| 1 | Disabled (Masked) |

## Operating Modes

The MCU has five operating modes that are specified by how the clock is used. The functions available in each mode are listed in table 19, and operations are shown in table 20. Transitions between operating modes are shown in figure 10.

**Active Mode:** The MCU operates according to the clock generated by the system oscillators $OSC_1$ and $OSC_2$.

**Table 19   Functions Available in Each Operating Mode**

| | | Mode Name | | | | |
|---|---|---|---|---|---|---|
| | | **Active** | **Standby** | **Stop** | **Watch** | **Subactive**[4] |
| Activation method | | RESET cancellation, interrupt request | SBY instruction | TMA3 = 0 STOP instruction | TMA3 = 1 STOP instruction | $\overline{INT}_0$ or timer A interrupt request from watch mode |
| Status | System oscillator | | | Stopped | Stopped | Stopped |
| | Subsystem oscillator | | | [1] | | |
| | Instruction execution ($\varnothing_{CPU}$) | | Stopped | Stopped | Stopped | |
| | Interrupt function interrupt ($\varnothing_{PER}$) | | | Stopped | Stopped | [5] |
| | Clock function interrupt ($\varnothing_{CLK}$) | | | Stopped | [2] | [2] |
| | RAM | | Retained | Retained | Retained | |
| | Registers/flags | | Retained | Reset[6] | Retained | Retained/ operating |
| | I/O | | Retained | Reset[3] | Retained | |
| Cancellation method | | RESET input, STOP/SBY instruction | RESET input, interrupt request | RESET input | RESET input, $\overline{INT}_0$ or timer A interrupt request | RESET input, STOP/SBY instruction |

Notes:   ▓▓▓ indicates in operation.
1. To reduce current dissipation, stop all oscillation in external circuits.
2. Refer to the Interrupt Frame section for details.
3. Output pins are at high impedance.
4. Subactive mode is an optional function;  specify it on the function option list.
5. The A/D converter does not operate.
6. Port mode register B retains the contents it had in active mode.

| | | System Clock ($\varnothing_{CPU}$) | |
|---|---|---|---|
| | | **Operating** | **Stopped** |
| **Non-Time-Base Peripheral Function Clock ($\varnothing_{PER}$)** | **Operating** | Active mode | Standby mode |
| | | Subactive mode | |
| | **Stopped** | — | Watch mode (TMA3 = 1) |
| | | | Stop mode (TMA3 = 0) |

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# HD404328 Series

**Standby Mode:** The MCU enters standby mode when the SBY instruction is executed from active mode. In this mode, the oscillators, interrupts, timer/counters, and serial interface continue to operate, but all instruction execution-related clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

The standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and resumes, executing the next instruction after the SBY instruction. If the interrupt enable flag is 1, that interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 11.

**Stop Mode:** The MCU enters stop mode if the STOP instruction is executed in active mode when TMA3 = 0. In this mode, the system oscillator stops, which stops all MCU functions as well.

The stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one $t_{RC}$ to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

**Watch Mode:** The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

The watch mode is terminated by a RESET input or a timer-A/$\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. After an interrupt request is generated, the time required to enter active mode is $t_{RC}$ for a timer A interrupt, and $T_X$ (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{INT_0}$ interrupt, as shown in figures 13 and 14.

**Table 20  Operations in Low-Power Dissipation Modes**

| Function | Stop Mode | Watch Mode | Standby Mode | Subactive Mode[*3] |
|---|---|---|---|---|
| CPU | Reset | Retained | Retained | |
| RAM | Retained | Retained | Retained | |
| Timer A | Reset | | | |
| Timer B | Reset | Stopped | | |
| Timer C | Reset | Stopped | | |
| Serial interface | Reset | Stopped[*3] | | |
| LCD | Reset | | | |
| I/O | Reset[*1] | Retained | Retained | |
| A/D | Reset | Stopped | | Stopped |
| Zero-crossing detection | Stopped[*4] | Stopped[*4] | | |

Notes: ▓ indicates in operation.
1. Output pins are at high impedance.
2. Subactive mode is an optional function specified on the function option list.
3. Transmission/reception is activated if a clock is input in external clock mode. (However interrupts stop.)
4. The bias circuits still operate when the $D_8$/ZCD/$\overline{EVENT}$ pin is set to ZCD.

Operation during mode transition is the same as that at standby mode cancellation (figure 11).

**Subactive Mode:** The CPU operates with a clock generated by the X1 and X2 oscillation circuits. Functions that can operate in subactive mode are listed in table 20. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

The subactive mode is an optional function that the user must specify on the function option list.
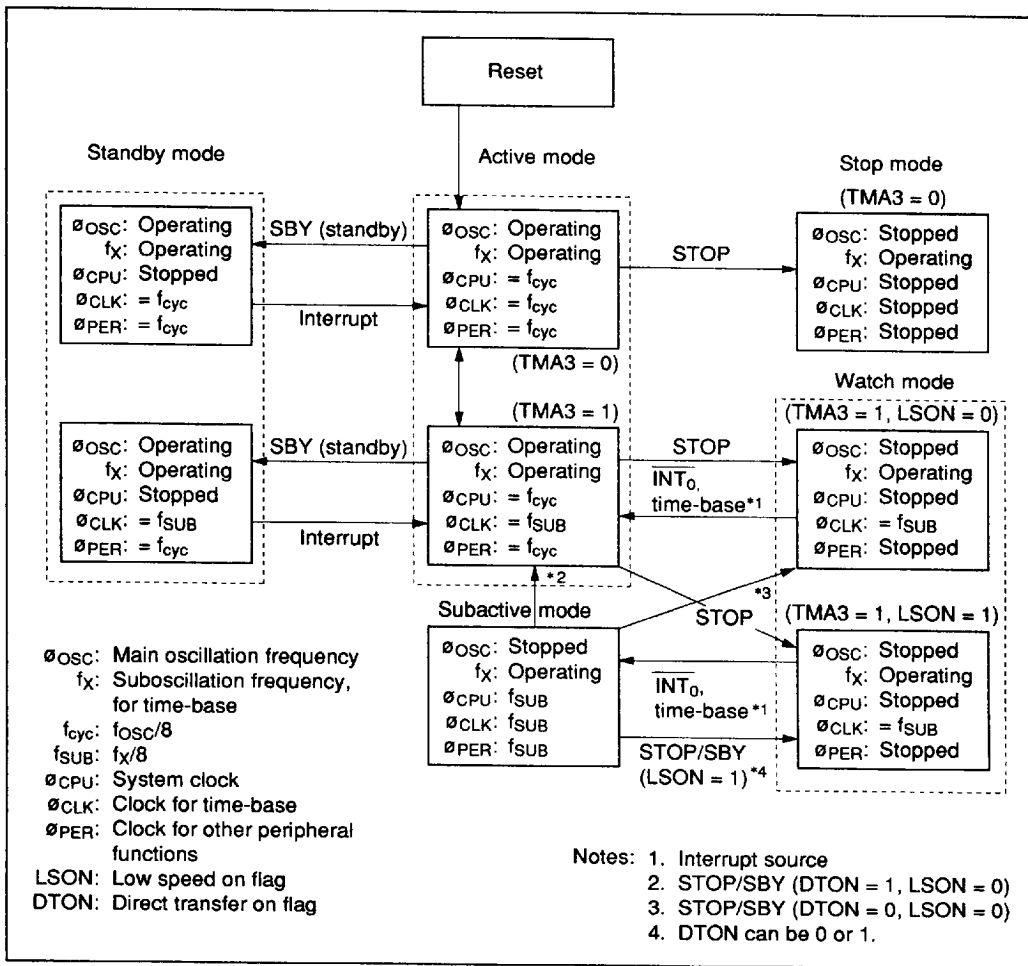


**Figure 10  MCU Status Transitions**
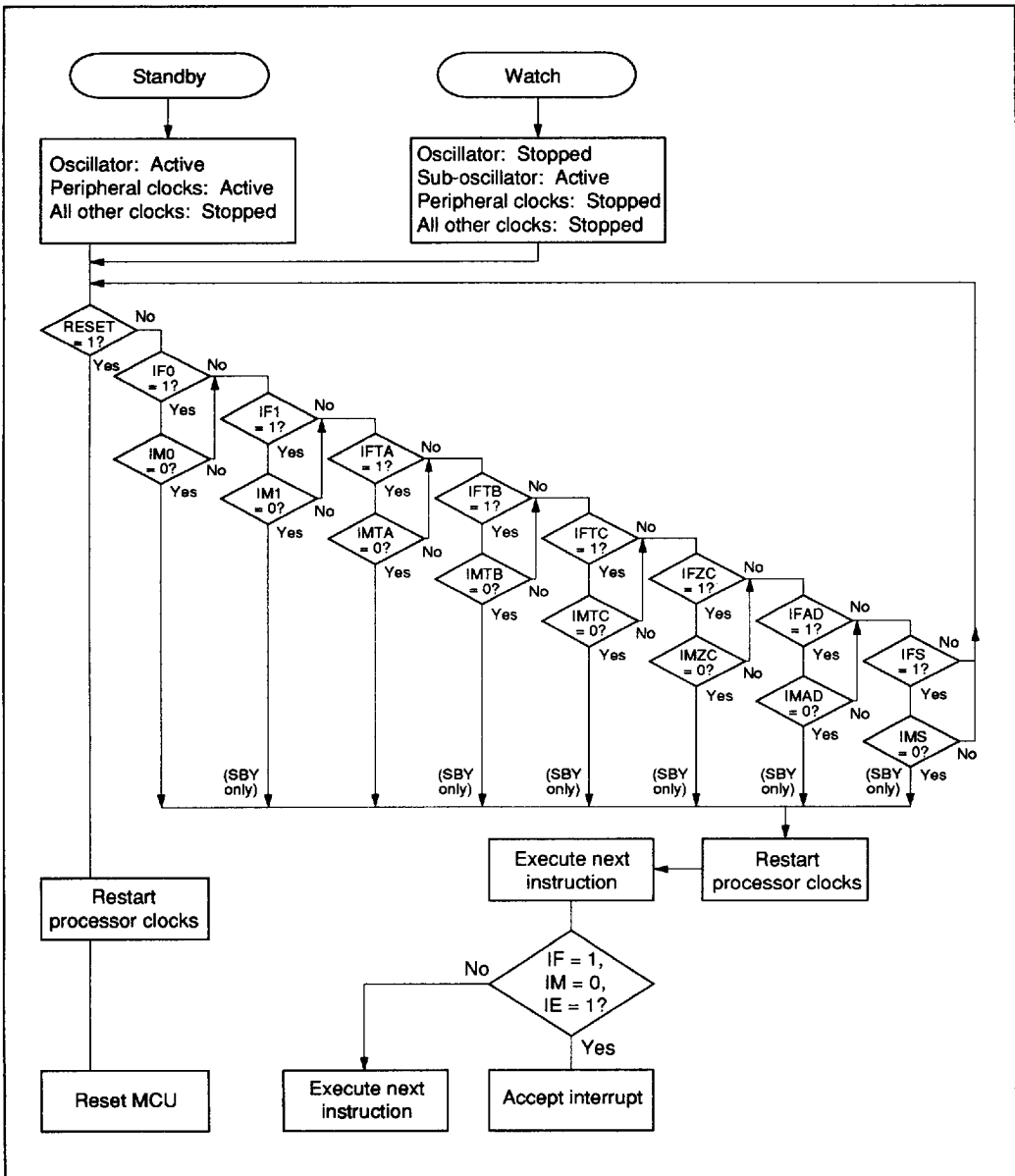
**Figure 11   MCU Operation Flowchart**

**Interrupt Frame:** In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. Three interrupt frame lengths (T) can be selected by the settings of the miscellaneous register, as shown in figure 14.

The time from an interrupt strobe to interrupt request generation is the oscillation stabilization period ($t_{RC}$), as shown in figure 13.

The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. The falling edge of the $\overline{INT_0}$ signal is input asynchronously with the interrupt frame timing, but it is regarded as input synchronously with the second interrupt strobe clock after the falling edge. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

Operation during the transition from watch mode to active mode is the same as that at standby mode cancellation (figure 11).
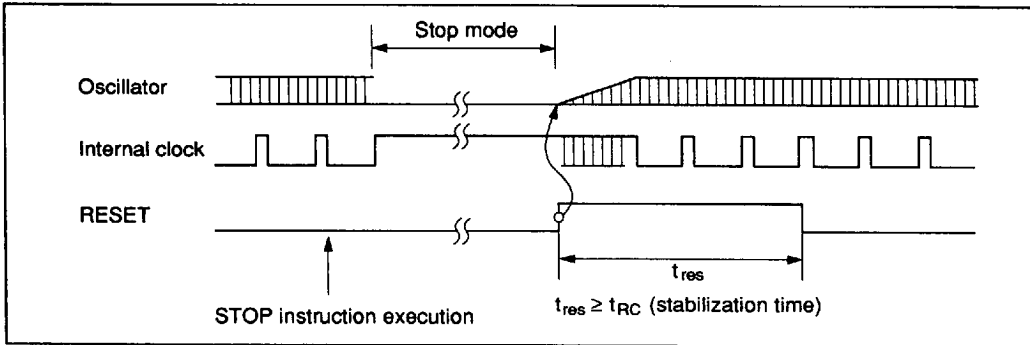
**Figure 12  Timing of Stop Mode Cancellation**
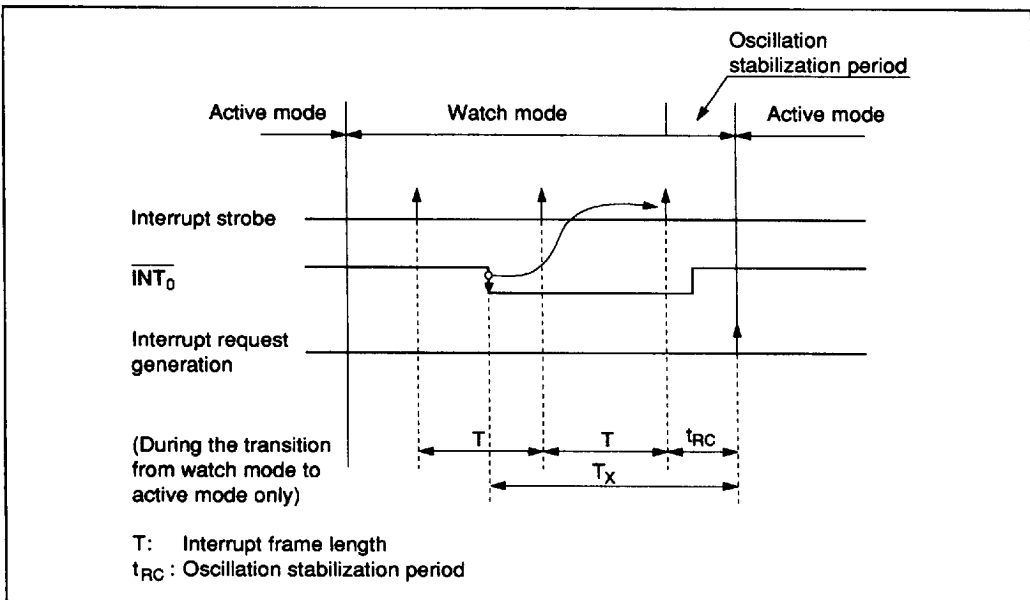
**Figure 13  Interrupt Frame**

**Direct Transfer:** By controlling the DTON flag, the MCU will be placed directly from subactive to active mode. The detailed procedure is as follows:
- Set the DTON flag in subactive mode while LSON = 0 and DTON = 1.
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode (see figure 15).

Note that DTON ($020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time ($t_D$) from subactive to active mode is $t_{RC} < t_D < T + t_{RC}$.

Miscellaneous register (MIS): $00C

| 3 | 2 | 1 | 0 |
|---|---|---|---|

Initial value: 0000,
R/W: W

$t_{RC}$ selection

R1$_2$/SO PMOS off

Setting for switching the system oscillator's frequency

| MIS | | T[*1] | $t_{RC}$[*1] |
|---|---|---|---|
| Bit 1 | Bit 0 | | |
| 0 | 0 | 0.24414 ms | 0.12207 ms |
| | | | 0.24414[*2] ms |
| 0 | 1 | 15.625 ms | 7.8125 ms |
| 1 | 0 | 125 ms | 62.5 ms |
| 1 | 1 | Not used | |

T: Interrupt frame length
$t_{RC}$: Oscillation stabilization period

Notes: 1. The value of $t_{RC}$ applies only when using a 32.768-kHz crystal oscillator.
2. Only direct transfer.

**Figure 14   Miscellaneous Register**

STOP/SBY execution

Subactive mode
(LSON = 0, DTON = 1)

Internal execution time

Oscillation stabilization time

Active mode

Interrupt strobe

Direct transfer timing

T

$t_{RC}$

T: Interrupt frame length
$t_{RC}$: Oscillation stabilization period
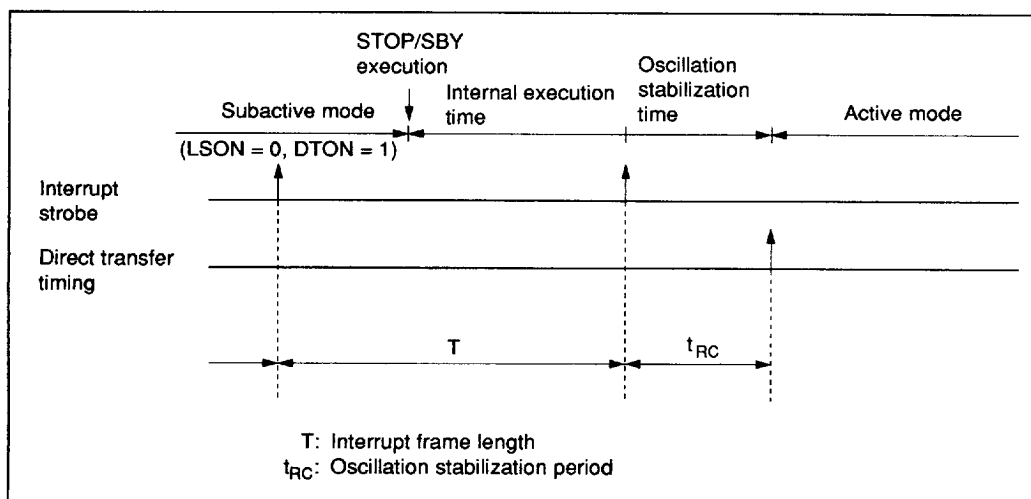
**Figure 15   Direct Transfer Timing**

**MCU Operation Sequence:** The MCU operates in the sequence shown in figures 16 to 18. It is reset by an asynchronous RESET input, regardless of its state.

The low-power mode operation sequence is shown in figure 18. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.
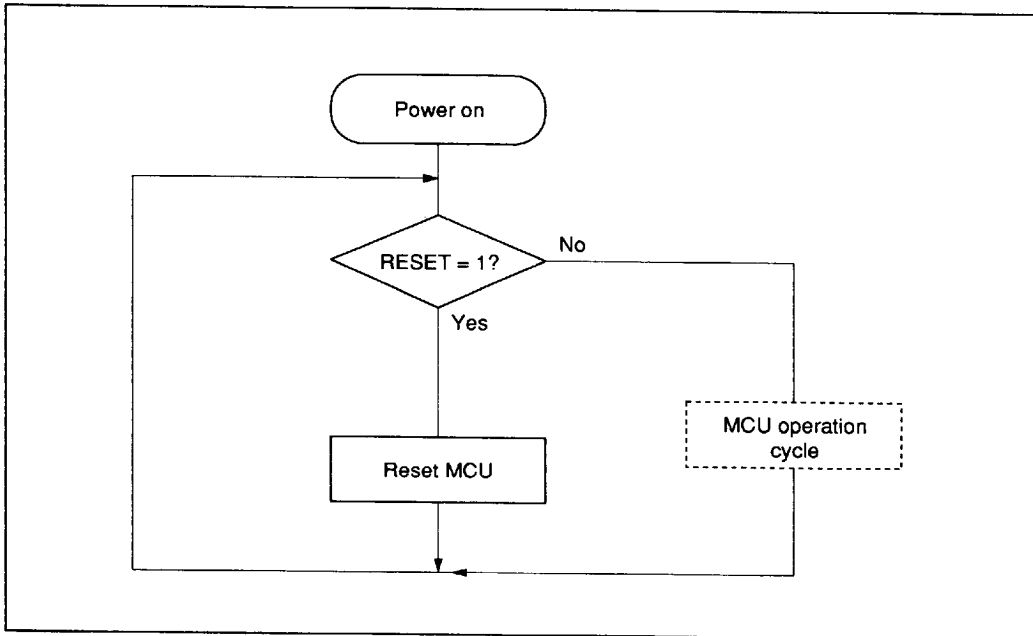


**Figure 16   MCU Operating Sequence (Power On)**
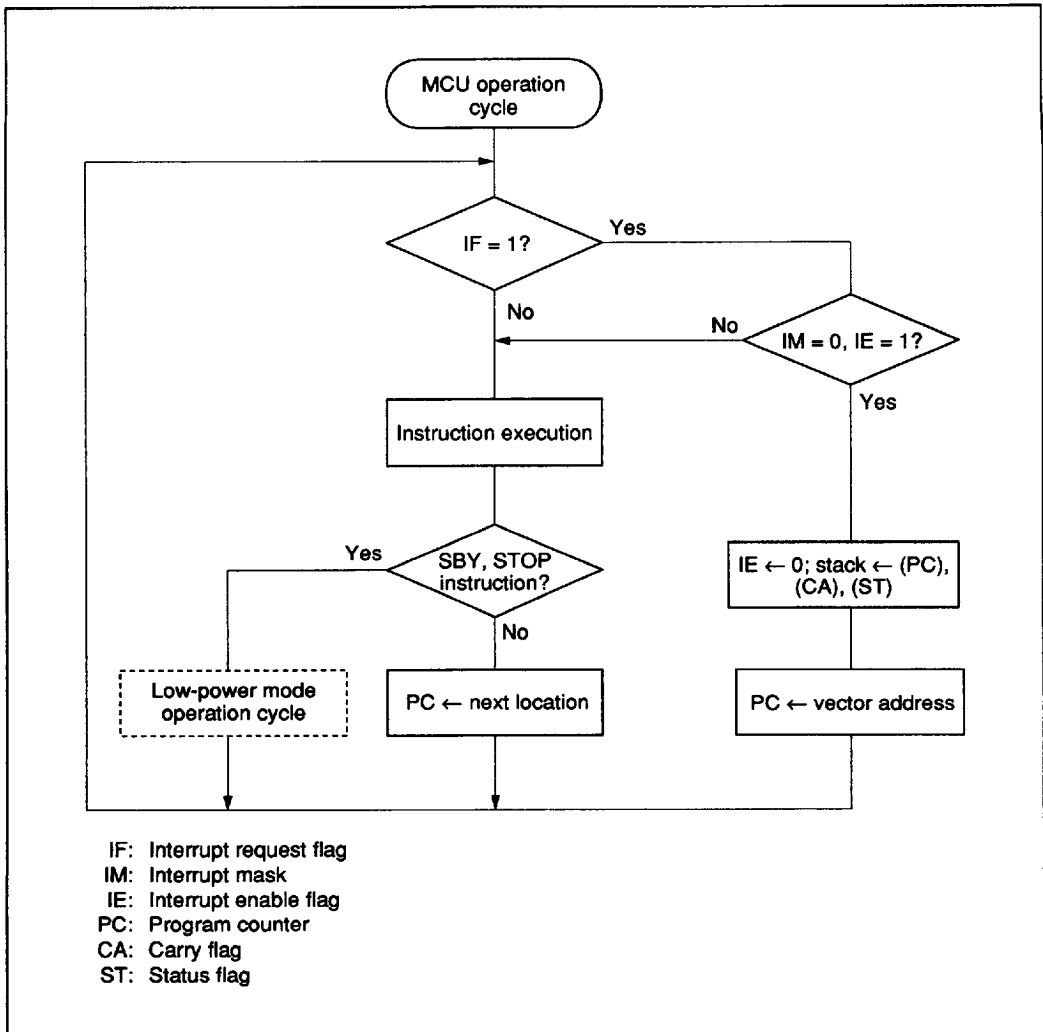
**Figure 17  MCU Operating Sequence (MCU Operation Cycle)**
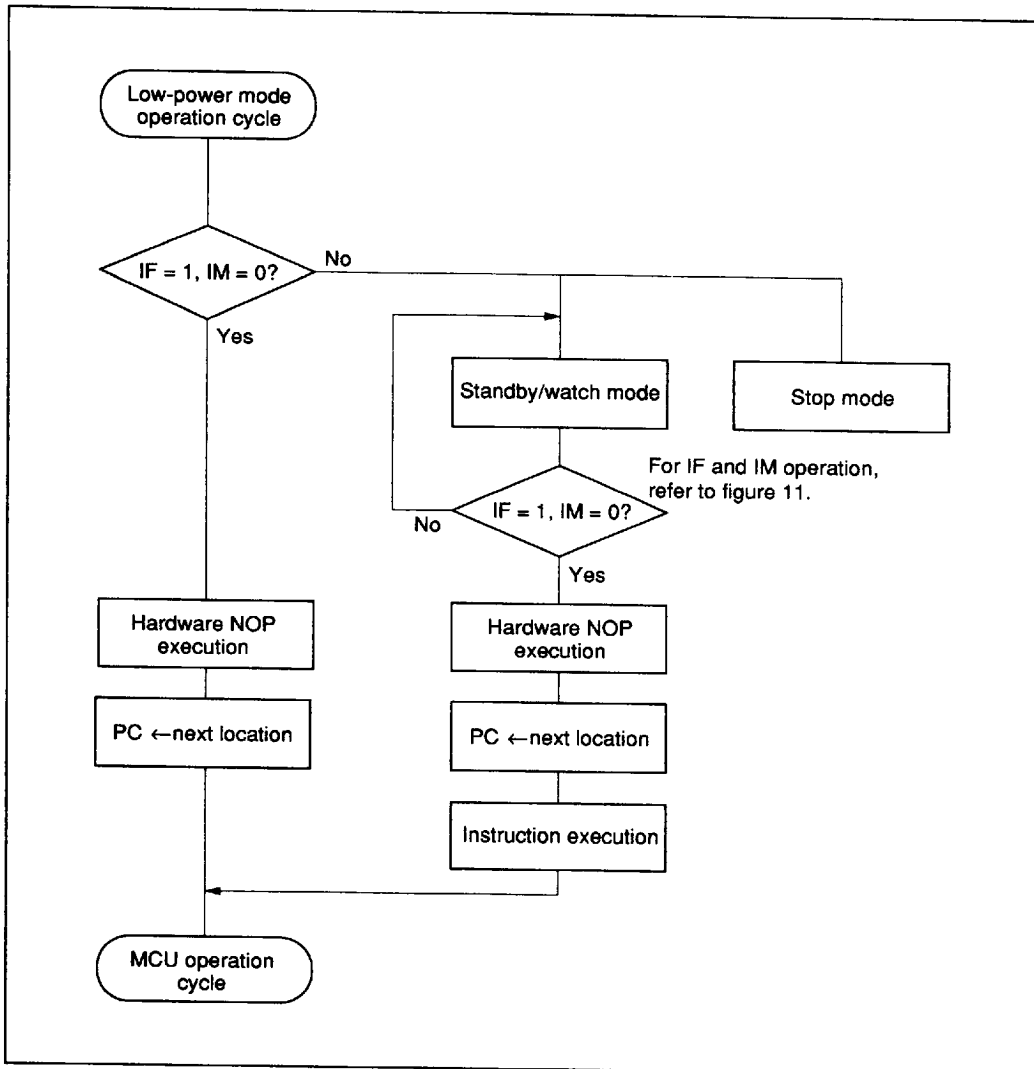
**Figure 18  MCU Operating Sequence (Low-Power Mode Operation)**

## Limitation on Use

- In subactive mode, the timer A interrupt request or the external interrupt request ($\overline{INT_0}$) occurs in synchronism with the interrupt strobe. If the STOP or SBY instruction is executed at the same time with the interrupt strobe, these interrupt requests will be cancelled and its corresponding interrupt request flags (IFTA, IF0) will be not set.

  In subactive mode, do not use the STOP or SBY instruction at the time of the interrupt strobe.

- When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Also, if the low level period after the falling edge of $\overline{INT_0}$ is shorter

than the interrupt frame, $\overline{INT_0}$ is not detected.

Edge detection is shown in figure 19. The level of the $\overline{INT_0}$ signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected.

In figure 20, the level of the $\overline{INT_0}$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either.

When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{INT_0}$ longer than interrupt frame.
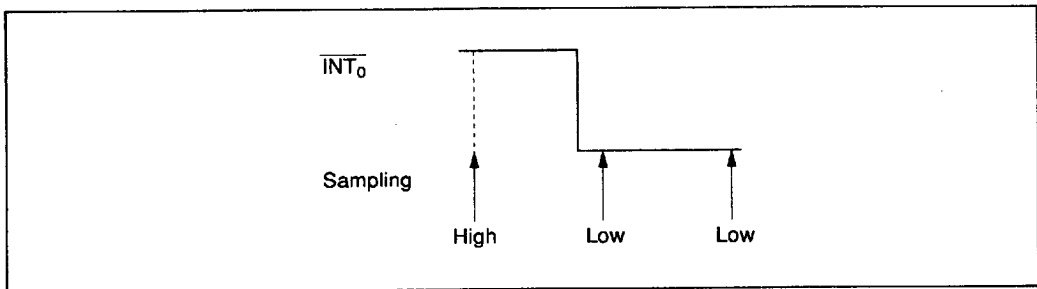


**Figure 19   Edge Detection**
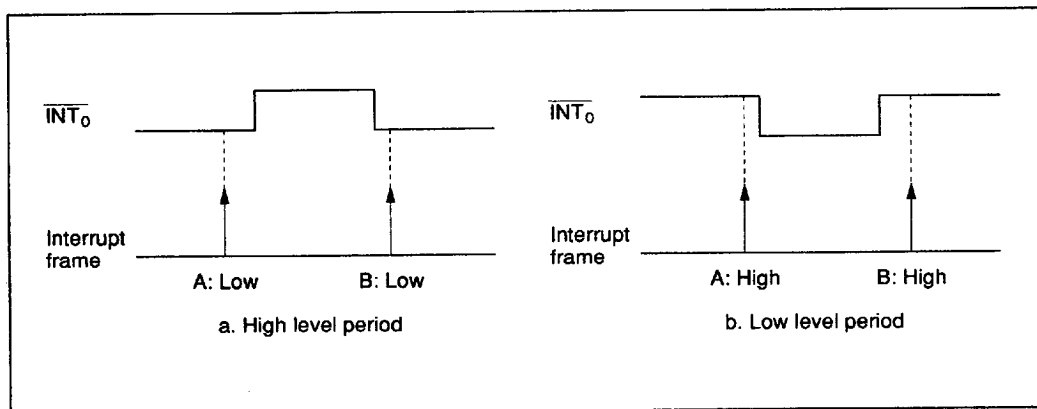


**Figure 20   Sampling Example**

## Internal Oscillator Circuit

A block diagram of the internal oscillator circuit is shown in figure 22. As shown in table 21, crystal and ceramic oscillators can be connected to $OSC_1$ and $OSC_2$, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock. Bit 3 of the miscellaneous register (MIS: $00C) must be set according to the frequency of the oscillator connected to $OSC_1$ and $OSC_2$.

Note: If the MIS register setting does not match the oscillator frequency, subsystems using 32-kHz oscillation will malfunction. Set the system oscillator frequency to anything outside the range of 1.0 MHz to 1.6 MHz when using 32-kHz oscillation.

Miscellaneous register (MIS): $00C

Initial value: 0000, R/W: W

| 3 | 2 | 1 | 0 |
|---|---|---|---|

$t_{RC}$ selection

R$l_2$/SO PMOS off

Setting for switching the system oscillator's frequency

| MIS Bit 3 | System Oscillator's Frequency |
|---|---|
| 0 | 1.6 MHz to 4.5 MHz |
| 1 | 0.4 MHz to 1.0 MHz |
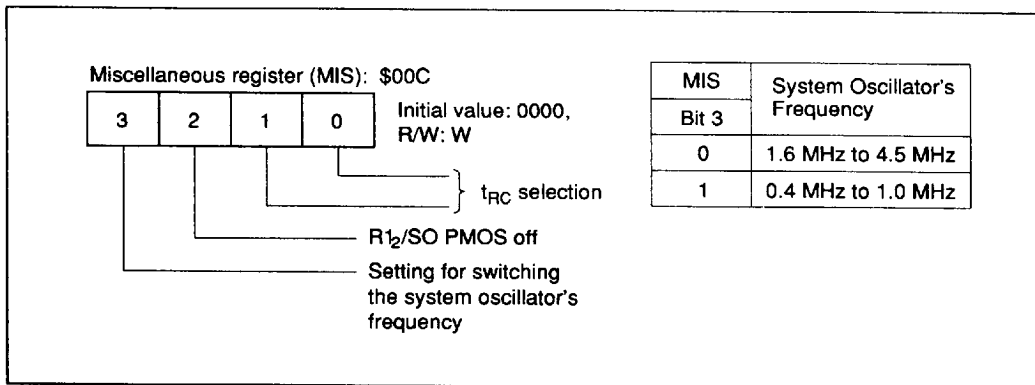
**Figure 21   Miscellaneous Register**
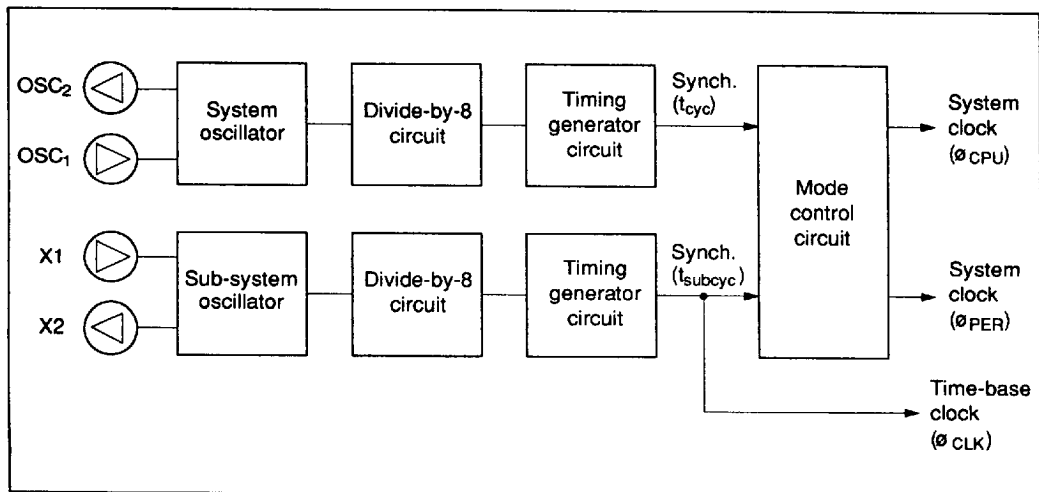


**Figure 22   Internal Oscillator Circuit**
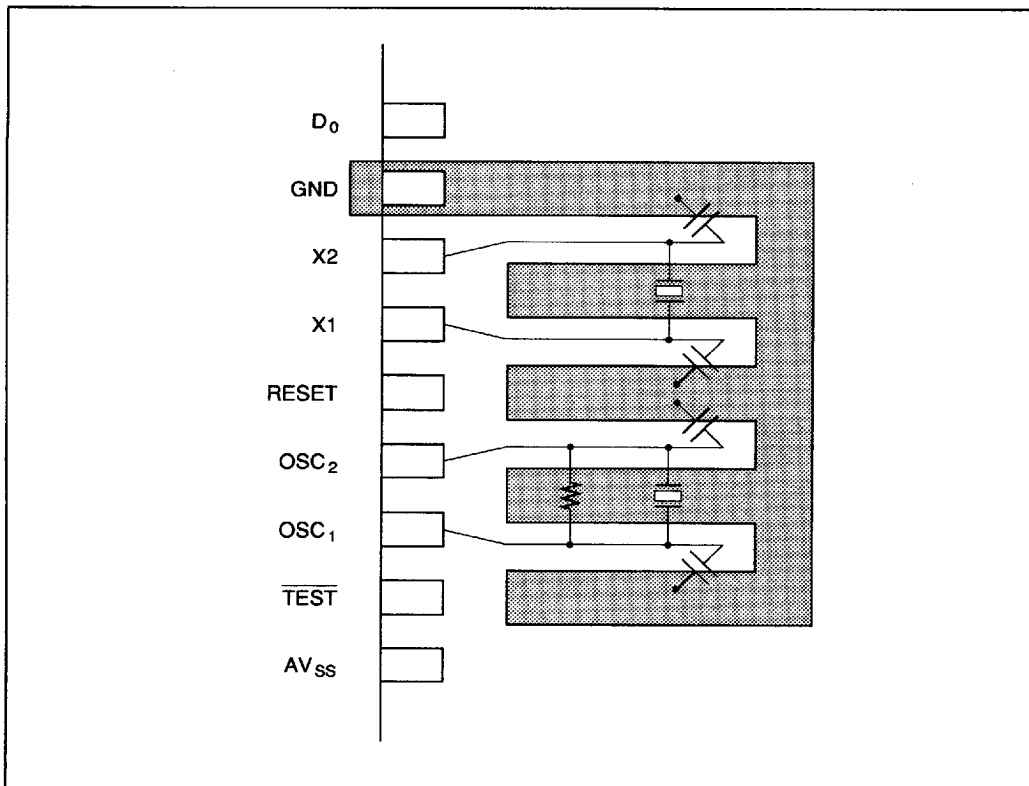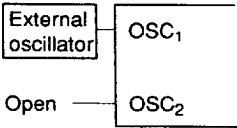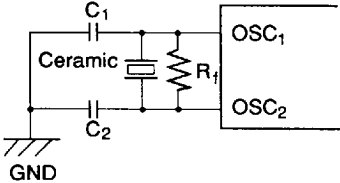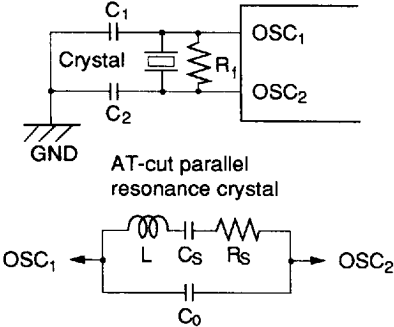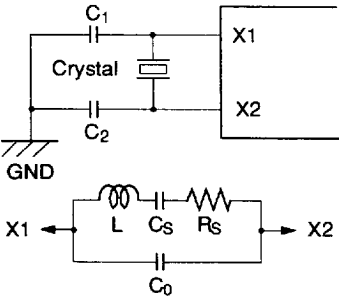
**Figure 23   Typical Layout of Crystal and Ceramic Oscillators**

**Table 21  Oscillator Circuit Examples**

| | Circuit Configuration | Circuit Constants |
|---|---|---|
| **External Clock Operation** ($OSC_1$, $OSC_2$) | External oscillator — $OSC_1$<br>Open — $OSC_2$ | |
| **Ceramic Oscillator** ($OSC_1$, $OSC_2$) | $C_1$, Ceramic, $R_f$, $OSC_1$, $OSC_2$, $C_2$, GND | Ceramic: CSA4.00MG (Murata)<br>$R_f = 1\ M\Omega\ \pm20\%$<br>$C_1 = C_2 = 30\ pF\ \pm20\%$ |
| **Crystal Oscillator** ($OSC_1$, $OSC_2$) | $C_1$, Crystal, $R_f$, $OSC_1$, $OSC_2$, $C_2$, GND<br>AT-cut parallel resonance crystal<br>$OSC_1 \leftarrow$ L $C_S$ $R_S$ $\rightarrow OSC_2$, $C_0$ | $R_f$: $1\ M\Omega\ \pm20\%$<br>$C_1 = C_2 = 10\ pF\ \pm10\%$<br>Crystal: Equivalent to circuit shown at bottom left<br>$C_0 = 7\ pF$, max.<br>$R_S = 100\ \Omega$, max.<br>$f = 1.0\ MHz$ to $4.5\ MHz$ |
| **Crystal Oscillator** (X1, X2) | $C_1$, Crystal, X1, X2, $C_2$, GND<br>X1 $\leftarrow$ L $C_S$ $R_S$ $\rightarrow$ X2, $C_0$ | $C_1 = C_2 = 15\ pF\ \pm5\%$<br>Crystal: 32.768 kHz, MX38T (Nippon Denpa)<br>$C_0 = 1.5\ pF$, typ.<br>$R_S = 14\ k\Omega$, typ. |

Notes:  1.  Circuit constants differ with different types of crystal and ceramic oscillators, and with the stray capacitance of the board, so consult the manufacturer of the oscillator to determine the circuit parameters.
2.  The wiring between the $OSC_1$ and $OSC_2$ pins (X1 and X2 pins) and the other elements should be as short as possible, and must not cross other wiring.  Refer to figure 23.
3.  If not using a 32.768-kHz crystal oscillator, fix the X1 pin to $V_{CC}$ and leave the X2 pin open.

## Input/Output

The MCU has 2 input pins and 33 input/output pins, 8 of the input/output pins being large-current pins (15 mA, max.). A program-controlled pull-up MOS transistor is provided for each input/output pin.

The output buffer is turned on and off by the data control register (DCR) during input through an input/output pin.

I/O pin circuit types are shown in table 22.

**Table 22 Circuit Configurations of I/O Pins**

| I/O Pin Type | Circuit | Applicable Pins |
|---|---|---|
| Common I/O Pin (with pull-up MOS transistor) |  Pull-up control signal — DCR — Output data PDR — Input data — Input control | $D_0$–$D_8$ $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$ $R4_0$–$R4_3$ $R5_0$–$R5_3$ |
| |  Pull-up control signal — DCR — Output data $\overline{SCK}$ (internal) — SCK | $\overline{SCK}$ |
| Output Pin (with pull-up MOS transistor) |  Pull-up control signal — DCR — Output data SO or BUZZ | SO BUZZ |
| Input Pin |  | $\overline{INT_0}$ $\overline{INT_1}$ |
| |  Pull-up control signal — PDR | SI $\overline{EVENT}$ |
| |  Input data — Input control | $D_9$ $D_{10}$ |
| | AC input signal — External capacitor — Zero-crossing detection circuit | ZCD |

Note: For details of the $R1_2$/SO pin, refer to note 2 of table 23.

**D Port ($D_0$–$D_{10}$):** Consist of 9 input/output pins and 2 input pins. Pins $D_0$–$D_7$ are high-current I/O pins, $D_8$ is an ordinary input/output pin, and $D_9$ and $D_{10}$ are input-only pins. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions.

The operating modes of $D_8$–$D_{10}$ are set by bits 2 and 3 of port mode register A (PMRA) and bits 0 and 1 of port mode register B (PMRB), as shown in figure 24. The on/off status of the output buffer is controlled by D port data control registers (DCRB, DCRC, and DCRD) that are mapped to memory addresses.

**R Ports:** Accessed in 4-bit units. Data is input to these ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions. The on/off status of the output buffers of the R ports are controlled by R port data control registers (DCR0–DCR5) that are mapped to memory addresses.

Pins $R1_0$–$R1_3$ are multiplexed with pins $\overline{SCK}$, SI, SO, and BUZZ, respectively. The operating modes of these pins are controlled by bit 3 of the serial mode register (SMR), bits 1 and 0 of port mode register A (PMRA), and bit 2 of port mode register C (PMRC), as shown in figure 24.

Ports R2–R5 are multiplexed with SEG1–SEG16. The functions of these pins must be specified by the LCD output register (LOR: $015).

**Pull-Up MOS Transistor Control:** A program-controlled pull-up MOS transistor is provided for each input/output pin. The on/off status of all these transistors is controlled by bit 3 of port mode register C (PMRC), and the on/off status of an individual transistor can also be controlled by the port data register of the corresponding pin—enabling on/off control of that pin alone.

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

The configuration of the I/O buffer is shown in figure 25, and the configurations of various program-controlled I/O circuits are given in table 23.

**How to Deal with Unused I/O Pins:** I/O pins that are not needed by the user system (floating) must be connected to $V_{CC}$ to prevent LSI malfunctions due to noise. These pins must either be pulled up to $V_{CC}$ by their pull-up MOS transistors or by resistors of about 100 k$\Omega$.

**Serial mode register (SMR):  $005**

| 3 | 2 | 1 | 0 |

Initial value: 0000, R/W: W

R1$_0$ /$\overline{\text{SCK}}$ pin mode selection

| SMR | Port |
|-----|------|
| Bit 3 | Selection |
| 0 | R1$_0$ |
| 1 | $\overline{\text{SCK}}$ |

**Port mode register A (PMRA):  $004**

| 3 | 2 | 1 | 0 |

Initial value: 0000, R/W: W

R1$_2$ /SO pin mode selection
R1$_1$ /SI pin mode selection
D$_9$ /$\overline{\text{INT}_0}$ pin mode selection
D$_{10}$/INT$_1$ pin mode selection

| PMRA | Port | PMRA | Port | PMRA | Port | PMRA | Port |
|------|------|------|------|------|------|------|------|
| Bit 3 | Selection | Bit 2 | Selection | Bit 1 | Selection | Bit 0 | Selection |
| 0 | D$_{10}$ | 0 | D$_9$ | 0 | R1$_1$ | 0 | R1$_2$ |
| 1 | INT$_1$ | 1 | $\overline{\text{INT}_0}$ | 1 | SI | 1 | SO |

**Port mode register B (PMRB):  $011**

| 3 | 2 | 1 | 0 |

Initial value: 0000, R/W: W

} D$_8$/ZCD/$\overline{\text{EVENT}}$ pin mode selection

} Not used

| PMRB | | Port |
|------|------|------|
| Bit 1 | Bit 0 | Selection |
| 0 | 0 | ZCD (low sensitivity) |
| | 1 | ZCD (high sensitivity)* |
| 1 | 0 | D$_8$ |
| | 1 | $\overline{\text{EVENT}}$ |

Note:* Becomes low sensitivity in subactive mode.

**Figure 24  I/O Switching Mode Registers**

**Port mode register C (PMRC): $012**

| 3 | 2 | 1 | 0 |
|---|---|---|---|

Initial value: 0000, R/W: W

} BUZZ output frequency selection

$R1_3$/BUZZ pin mode selection

Pull-up MOS transistor on/off selection
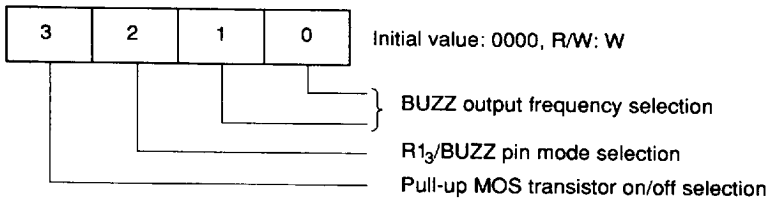
| PMRC Bit 3 | Pull-Up MOS On/Off Selection | PMRC Bit 3 | Port Selection |
|---|---|---|---|
| 0 | Off | 0 | $R1_3$ |
| 1 | On | 1 | BUZZ |

**LCD output register (LOR): $015**

| 3 | 2 | 1 | 0 |
|---|---|---|---|

Initial value: 0000, R/W: W

R2/SEG1–SEG4 pin mode selection
R3/SEG5–SEG8 pin mode selection
R4/SEG9–SEG12 pin mode selection
R5/SEG13–SEG16 pin mode selection

| LOR Bit 3 | Port Selection | LOR Bit 2 | Port Selection | LOR Bit 1 | Port Selection | LOR Bit 0 | Port Selection |
|---|---|---|---|---|---|---|---|
| 0 | R5 | 0 | R4 | 0 | R3 | 0 | R2 |
| 1 | SEG13–SEG16 | 1 | SEG9–SEG12 | 1 | SEG5–SEG8 | 1 | SEG1–SEG4 |

**Figure 24   I/O Switching Mode Registers (cont)**
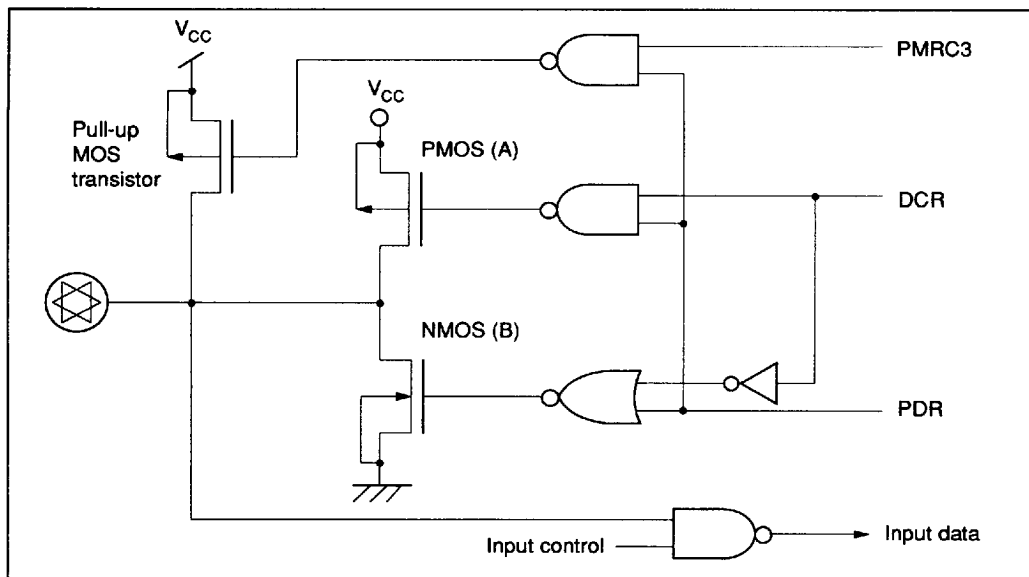
**Figure 25 I/O Buffer Configuration**

**Table 23 Programmable I/O Circuits**

| PMRC, Bit 3 | | 0 | | | | 1 | | |
|---|---|---|---|---|---|---|---|---|
| DCR | | 0 | | 1 | | 0 | | 1 |
| PDR | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| CMOS Buffer | PMOS (A) | Off | Off | Off | On | Off | Off | Off | On |
| | NMOS (B) | Off | Off | On | Off | Off | Off | On | Off |
| Pull-Up MOS Transistor | | Off | Off | Off | Off | Off | On | Off | On |

Notes:
1. Various I/O methods can be selected by different combinations of settings of the above mode registers (PMRC3, DCR, PDR).
2. The PMOS (A) transistor of the $R1_2$/SO pin can be turned off by setting bit 2 of the miscellaneous register (MIS) to 1.

| MIS | $R1_2$/SO Pin |
|---|---|
| Bit 2 | PMOS (A) |
| 0 | On |
| 1 | Off |

3. The relationships between DCRs and pins are as shown on the right.

| DCR | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| DCR0 | $R0_3$ | $R0_2$ | $R0_1$ | $R0_0$ |
| DCR1 | $R1_3$ | $R1_2$ | $R1_1$ | $R1_0$ |
| DCR2 | $R2_3$ | $R2_2$ | $R2_1$ | $R2_0$ |
| DCR3 | $R3_3$ | $R3_2$ | $R3_1$ | $R3_0$ |
| DCR4 | $R4_3$ | $R4_2$ | $R4_1$ | $R4_0$ |
| DCR5 | $R5_3$ | $R5_2$ | $R5_1$ | $R5_0$ |
| DCRB | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| DCRC | $D_7$ | $D_6$ | $D_5$ | $D_4$ |
| DCRD | — | — | — | $D_8$ |

# Timers

The MCU has two prescalers (S and W) and three timer/counters (A, B, and C).

**Prescaler S:** Eleven-bit counter that inputs a system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and stop modes, and at MCU reset. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and the serial mode register (SMR).

**Prescaler W:** Five-bit counter that inputs the X1 input clock signal divided by eight. Prescaler W output can be selected as a timer A input clock by timer mode register A (TMA).

**Timer A:** Eight-bit timer that can be used as a clock time-base (figure 26). It is initialized to $00 and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $001, bit 2) is generated, and timer A restarts from $00.

Timer A is used to generate regular interrupts (every 256 clocks) for measuring times between events. It can also be used as a clock time-base when bit 3 of timer mode register A (TMA) is set to 1. The timer is driven by the 32-kHz oscillator clock frequency divided by prescaler W, and the clock input to timer A is controlled by TMA. In this case, prescaler W and timer A can be initialized to $00 by software.
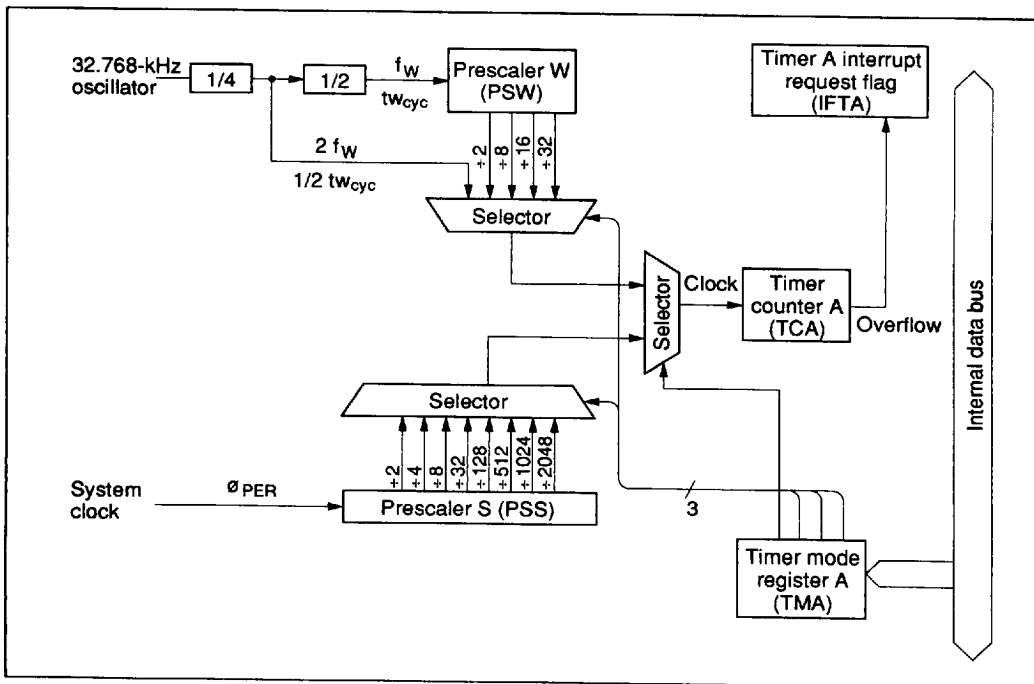


**Figure 26   Timer A Block Diagram**

**Timer B (TCBL and TLRL: $00A, TCBU and TLRU: $00B):** Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same addresses. The eight-bit configuration consists of lower and upper digits located at sequential addresses. A block diagram of timer B is shown in figure 27.

Timer counter B is initialized by writing to timer load register B (TLR). In this case, the lower nibble must be written to first. The contents of TLR are loaded into the timer counter at the same time the upper nibble is written to, initializing the timer counter. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched when the upper nibble is read.

An auto-reload function, input clock source, and prescaler division ratio of timer B depend on the state of timer mode register B (TMB). When an external event input is used as the input clock source of TMB, the $D_8$/ZCD/$\overline{EVENT}$ pin must be set to function as the ZCD or $\overline{EVENT}$ pin by setting port mode register B (PMRB: $011).

Timer B is initialized to the value set in TMB by software, and is then incremented by one by each clock input. If an input is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer B is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0).
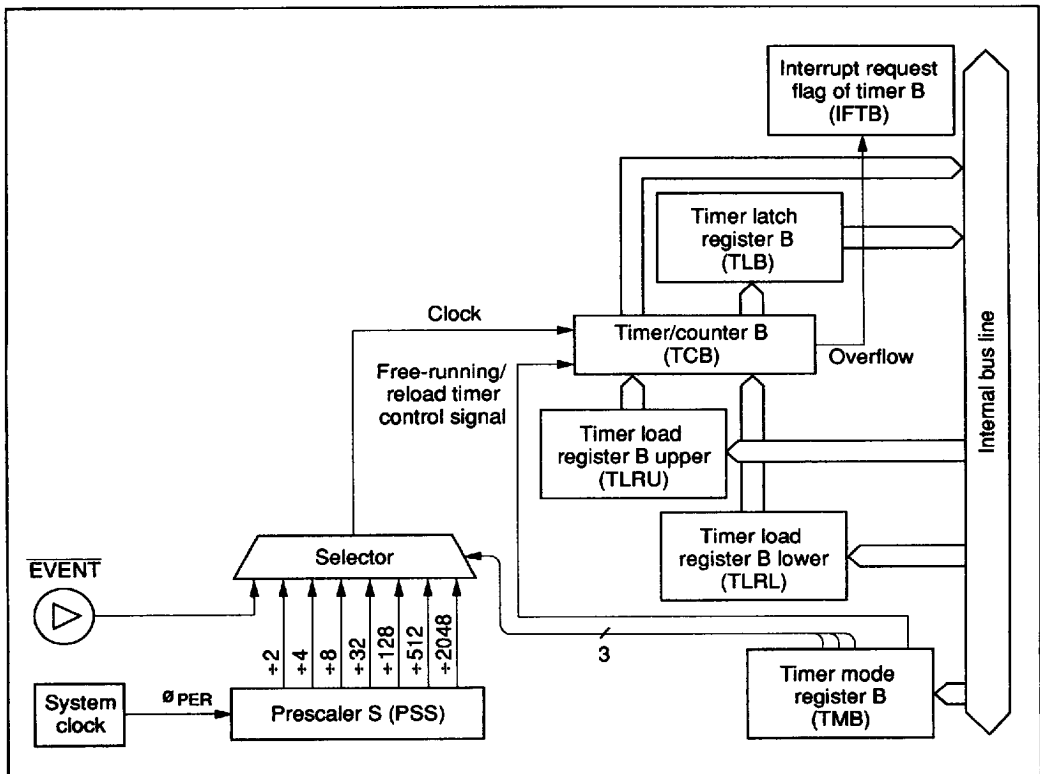


**Figure 27   Timer B Free-Running and Reload Operation Block Diagram**

**Timer C (TCCL and TCRL: $00A, TCCU and TCRU: $00B):** Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same addresses. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B. A block diagram of timer C is shown in figure 28.

The auto-reload function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in TMC by software, then is incremented by one at each clock input. If an input is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer C is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2).

Timer C also functions as a watchdog timer. If a program routine runs out of control and an overflow is generated while the watchdog on (WDON) flag is set, the MCU is reset. This error can be detected by having the program control timer C reset before timer C reaches $FF.

The WDON can only have 1 written to it; it is cleared to 0 only by MCU reset.
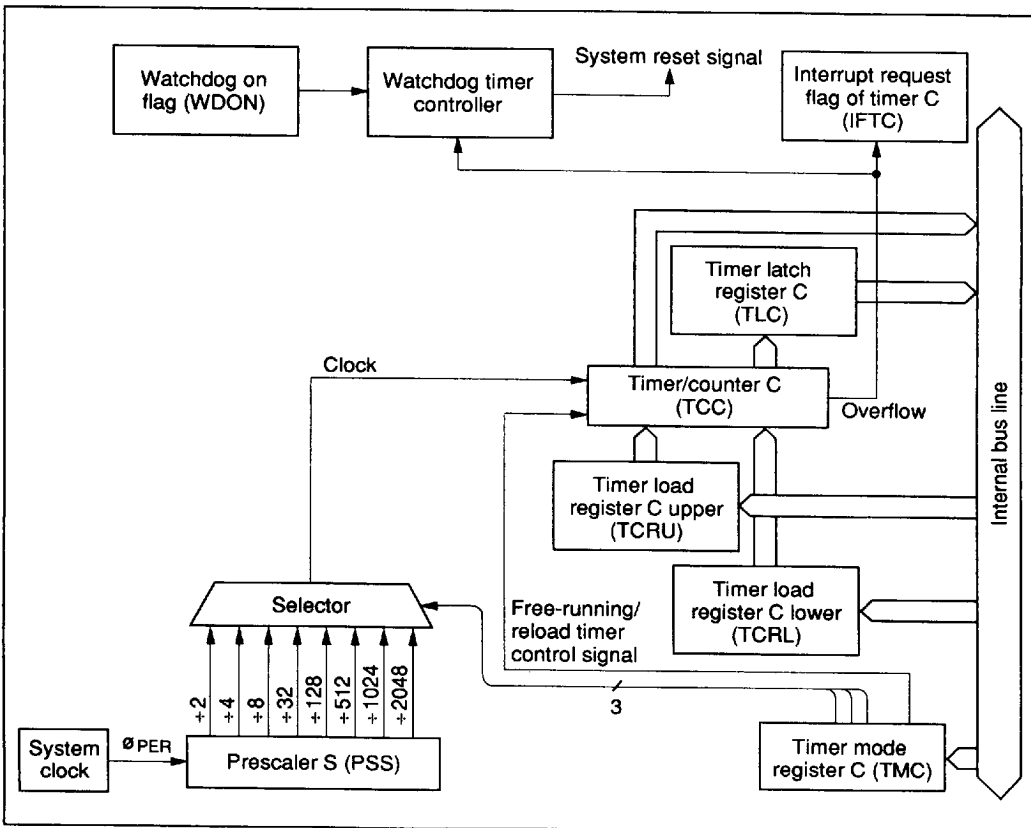


**Figure 28   Timer C Block Diagram**

**Timer Mode Register A (TMA: $008):** Four-bit write-only register that controls timer A as shown in table 24.

**Timer Mode Register B (TMB: $009):** Four-bit write-only register that selects the auto-reload function, input clock source, and the prescaler division ratio as shown in table 25. It is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer B initialization set by writing to TMB must be done after a mode change becomes valid.

**Timer Mode Register C (TMC: $00D):** Four-bit write-only register that selects the auto-reload function and prescaler division ratio as shown in table 26. It is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer C initialization set by writing to TMC must be done after a mode change becomes valid.

**Table 24  Timer Mode Register A**

| TMA | | | | Source Prescaler, Input Clock Period, Operating Mode | |
|---|---|---|---|---|---|
| Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
| 0 | 0 | 0 | 0 | PSS, 2048 $t_{cyc}$ | Timer A mode |
| | | | 1 | PSS, 1024 $t_{cyc}$ | |
| | | 1 | 0 | PSS, 512 $t_{cyc}$ | |
| | | | 1 | PSS, 128 $t_{cyc}$ | |
| | 1 | 0 | 0 | PSS, 32 $t_{cyc}$ | |
| | | | 1 | PSS, 8 $t_{cyc}$ | |
| | | 1 | 0 | PSS, 4 $t_{cyc}$ | |
| | | | 1 | PSS, 2 $t_{cyc}$ | |
| 1 | 0 | 0 | 0 | PSW, 32 $t_{subcyc}$ | Time-base mode |
| | | | 1 | PSW, 16 $t_{subcyc}$ | |
| | | 1 | 0 | PSW, 8 $t_{subcyc}$ | |
| | | | 1 | PSW, 2 $t_{subcyc}$ | |
| | 1 | 0 | 0 | PSW, 1/2 $t_{subcyc}$ | |
| | | | 1 | Do not use | |
| | | 1 | 0 | PSW, TCA reset | |
| | | | 1 | | |

Notes: 1. $t_{subcyc}$ = 244.14 μs (when 32.768-kHz crystal oscillator is used)
2. $t_{cyc}$ = 1.9074 μs (when 4.1943-MHz crystal oscillator is used)
3. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
4. If PSW or TCA reset is selected while the LCD is operating, LCD operation halts (power switch goes off and all SEG and COM pins are grounded).
   When an LCD is connected for display, the PSW and TCA reset periods must be set in the program to the minimum.
5. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

## Pulse Output

The MCU has a built-in pulse output function called BUZZ. The pulse frequency can be selected from the prescaler S's outputs, and the output frequency depends on the state of port mode register C (PMRC: $012), as shown in table 27. The duty cycle of the pulse output is fixed at 50%. When the pulse output function is used, the $R1_3$/BUZZ pin must be specified as BUZZ by PMRC.

**Table 25   Timer Mode Register B**

**TMB**

| Bit 3 | Auto Reload Function |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| TMB | | | Input Clock Period/ |
|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | Input Clock Source |
| 0 | 0 | 0 | 2048 $t_{cyc}$ |
| | | 1 | 512 $t_{cyc}$ |
| | 1 | 0 | 128 $t_{cyc}$ |
| | | 1 | 32 $t_{cyc}$ |
| 1 | 0 | 0 | 8 $t_{cyc}$ |
| | | 1 | 4 $t_{cyc}$ |
| | 1 | 0 | 2 $t_{cyc}$ |
| | | 1 | ZCD/EVENT (external event input) |

**Table 26   Timer Mode Register C**

**TMC**

| Bit 3 | Auto Reload Function |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| TMC | | | Input Clock Period |
|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 2048 $t_{cyc}$ |
| | | 1 | 1024 $t_{cyc}$ |
| | 1 | 0 | 512 $t_{cyc}$ |
| | | 1 | 128 $t_{cyc}$ |
| 1 | 0 | 0 | 32 $t_{cyc}$ |
| | | 1 | 8 $t_{cyc}$ |
| | 1 | 0 | 4 $t_{cyc}$ |
| | | 1 | 2 $t_{cyc}$ |

**Table 27   Port Mode Register C**

**PMRC**

| Bit 1 | Bit 0 | Prescaler Division Ratio |
|---|---|---|
| 0 | 0 | ÷ 1024 |
| | 1 | ÷ 512 |
| 1 | 0 | ÷ 256 |
| | 1 | ÷ 128 |

## Serial Interface

The MCU has a clock-synchronous serial interface which transmits and receives 8-bit data.

The serial interface consists of a serial data register (SR), serial mode register (SMR), port mode register A (PMRA), octal counter, and selector, as shown in figure 29. The $R1_0/\overline{SCK}$ pin and the transmit clock are controlled by writing data to the SMR. The transmit clock shifts the contents of the SR, which can be read and written to by software, before transmission starts between two MCUs.

The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, it starts counting at the falling edge of the transmit clock ($\overline{SCK}$), and it increments at the rising edge of the clock. A serial interrupt request flag is set when the eighth transmit clock signal is input (the serial interface is reset) or when serial transmission is discontinued (the octal counter is reset).

**Serial Mode Register (SMR: $005):** Four-bit write-only register that controls the $R1_0/\overline{SCK}$ pin, transmit clock, and prescaler division ratio as shown in figure 30. Writing to this register initializes the serial interface.

A write signal input to the serial mode register discontinues the input of the transmit clock to the serial data register and octal counter. Therefore, if a write is performed during data transmission, the octal counter is reset to 000 to stop transmission, and, at the same time, the serial interrupt request flag is set.

Write operations are valid from the second instruction execution cycle, so the STS instruction must be executed after at least two cycles have been executed. The serial mode register is initialized to $0 by MCU reset.
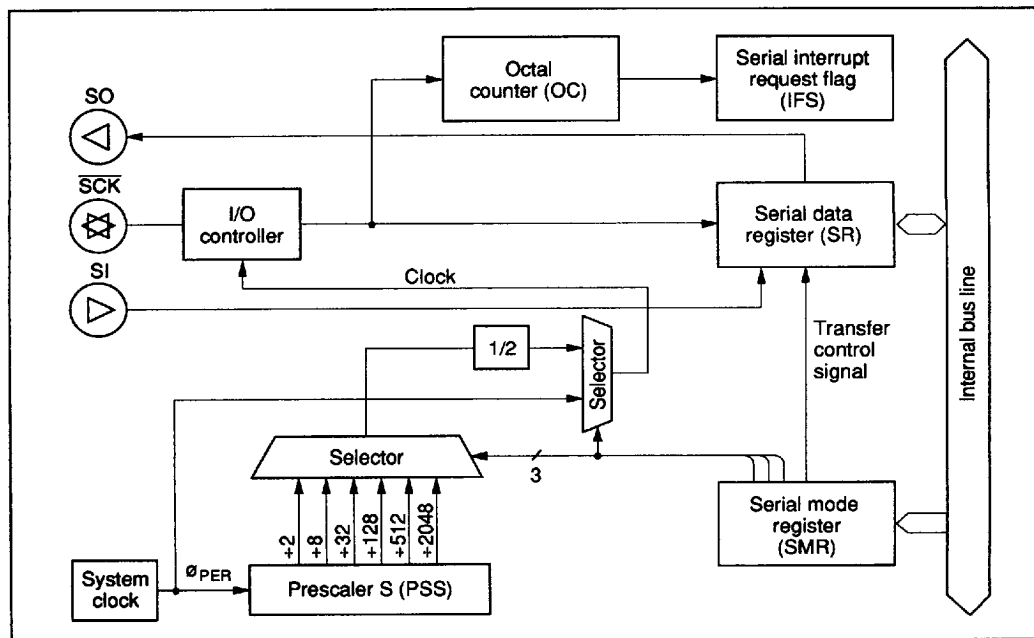


**Figure 29  Serial Interface Block Diagram**

**Serial Data Register (SRL: $006, SRU: $007):** Eight-bit read/write register separated into upper and lower digits located at sequential addresses. Data in this register is output from the SO pin, LSB first, in synchronism with the falling edge of the transmit clock; and data is input, LSB first, through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 31.

Data cannot be read or written during serial data transmission. If a read/write occurs during transmission, the accuracy of the resultant data cannot be guaranteed.

**Selecting and Changing Operating Mode:** Table 28 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of PMR and SMR settings; to change the operating mode, always initialize the serial interface internally by writing data to the SMR.

**Serial Interface Operation:** Three operating modes are provided for the serial interface; transitions between them are shown in figure 32.

In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed, the serial interface enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal clock, shifts the serial clock register, and activates serial transmission. However, note that if clock output mode is selected, the transmit clock is continuously output but data is not transmitted.

During transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters transmit clock wait state. If the state changes from transmit to another state, the serial interrupt request flag is set by the octal counter reaching 000.
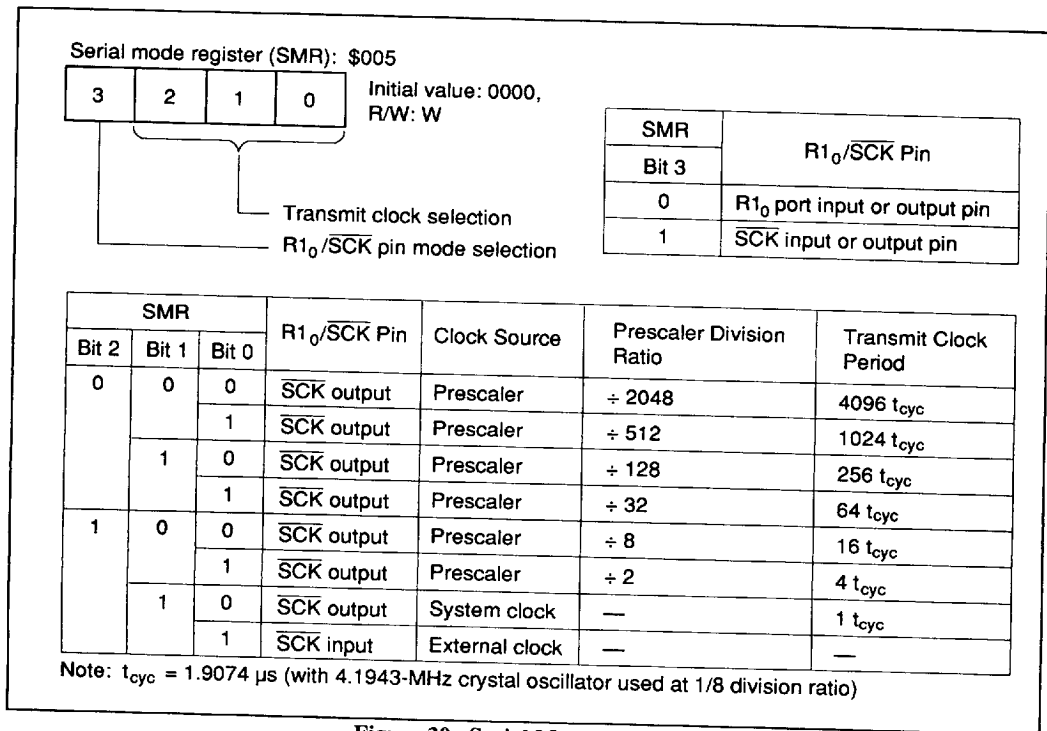
Serial mode register (SMR): $005

Initial value: 0000,
R/W: W

| 3 | 2 | 1 | 0 |
|---|---|---|---|

Transmit clock selection

$R1_0$/$\overline{SCK}$ pin mode selection

| SMR | $R1_0$/$\overline{SCK}$ Pin |
|-----|------------------------------|
| Bit 3 | |
| 0 | $R1_0$ port input or output pin |
| 1 | $\overline{SCK}$ input or output pin |

| SMR | | | $R1_0$/$\overline{SCK}$ Pin | Clock Source | Prescaler Division Ratio | Transmit Clock Period |
|-------|-------|-------|------------------------|--------------|--------------------------|------------------------|
| Bit 2 | Bit 1 | Bit 0 | | | | |
| 0 | 0 | 0 | $\overline{SCK}$ output | Prescaler | ÷ 2048 | 4096 $t_{cyc}$ |
| | | 1 | $\overline{SCK}$ output | Prescaler | ÷ 512 | 1024 $t_{cyc}$ |
| | 1 | 0 | $\overline{SCK}$ output | Prescaler | ÷ 128 | 256 $t_{cyc}$ |
| | | 1 | $\overline{SCK}$ output | Prescaler | ÷ 32 | 64 $t_{cyc}$ |
| 1 | 0 | 0 | $\overline{SCK}$ output | Prescaler | ÷ 8 | 16 $t_{cyc}$ |
| | | 1 | $\overline{SCK}$ output | Prescaler | ÷ 2 | 4 $t_{cyc}$ |
| | 1 | 0 | $\overline{SCK}$ output | System clock | — | 1 $t_{cyc}$ |
| | | 1 | $\overline{SCK}$ input | External clock | — | — |

Note: $t_{cyc}$ = 1.9074 µs (with 4.1943-MHz crystal oscillator used at 1/8 division ratio)

**Figure 30   Serial Mode Register**

4496204 0047664 T18

In this state, if the internal clock has been selected, the transmit clock is output in answer to the execution of the STS instruction, but serial transmission is inhibited after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or transfer state, the serial mode register (SMR) must be written to, to initialize the serial interface. The serial interface then enters STS wait state.

If the serial interface shifts from transfer state to another state, the octal counter returns to 000, setting the serial interrupt request flag.

**Transmit Clock Error Detection:** The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 33.

If more than eight transmit clocks are input in transmit clock wait state, the serial interface's state changes to transfer, transmit clock wait, then back to transfer.

If the serial interface is set to STS wait state by writing data to the SMR after the serial interrupt request flag has been reset, the flag is reset again.

**Note on Use:** The serial interrupt request flag might not be set if the status is changed from transfer by the execution of an SMR write or STS instruction during the first period that the transmit clock is low. To prevent this, program a check that the SCK pin is at 1 (by executing an input instruction for the R1 port) before the execution of an SMR write or STS instruction, to ensure that the serial interrupt request flag is set.
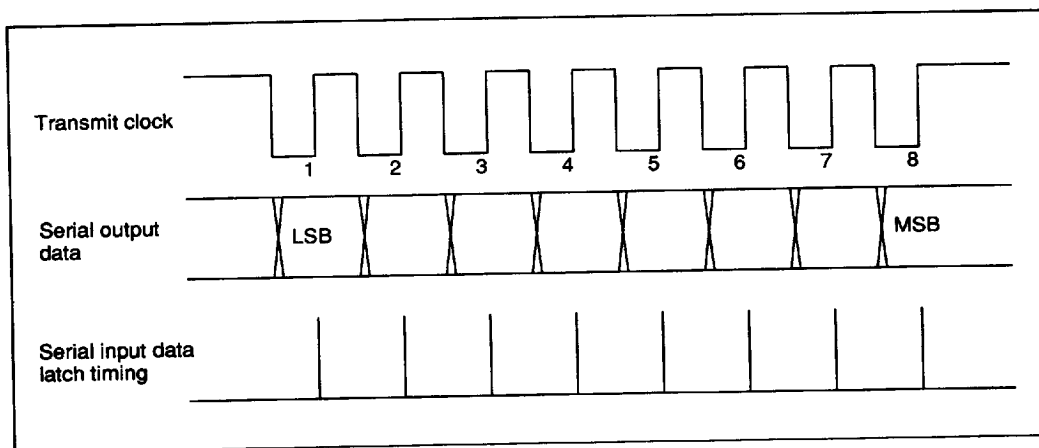


**Figure 31   Timing of Serial Interface Output**

**Table 28   Serial Interface Operating Modes**

| SMR | PMRA | | |
|---|---|---|---|
| Bit 3 | Bit 1 | Bit 0 | Operating Mode |
| 1 | 0 | 0 | Continuous clock output mode |
| | | 1 | Transmit mode |
| | 1 | 0 | Receive mode |
| | | 1 | Transmit/receive mode |

STS instruction wait state
(octal counter = 000,
transmit clock disabled)

SMR write

STS instruction

8 transmit clocks
(internal clock)
(IFS ← 1)

SMR write (IFS ← 1)

Transmit clock

Transmit clock wait state
(octal counter = 000)

8 transmit clocks (external clock)
STS instruction
(IFS ← 1)

Transfer state
(octal counter ≠ 000)
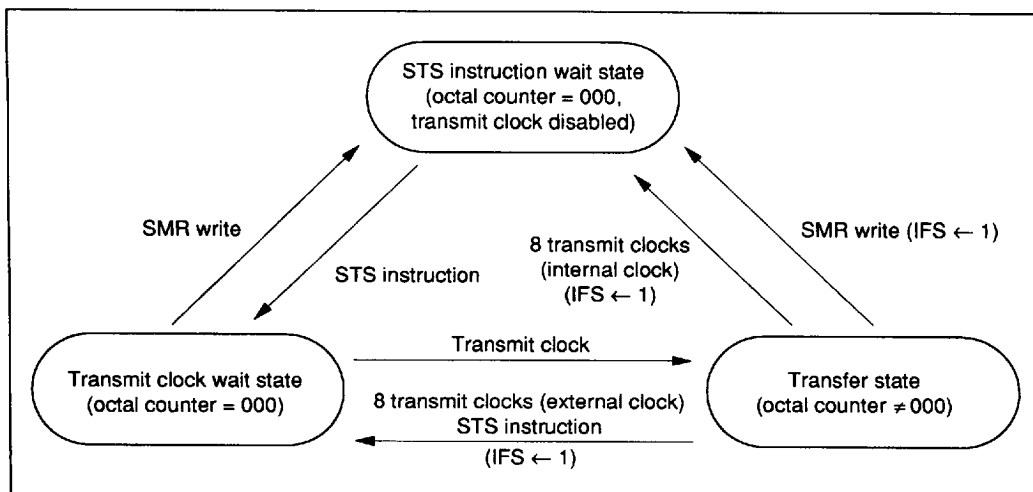
**Figure 32   Serial Interface Mode Transitions**

Transmission
completion (IFS ← 1)

Interrupts inhibited

IFS ← 0

SMR write

IFS = 1?

Yes

Transmit clock
error processing

No

Normal termination
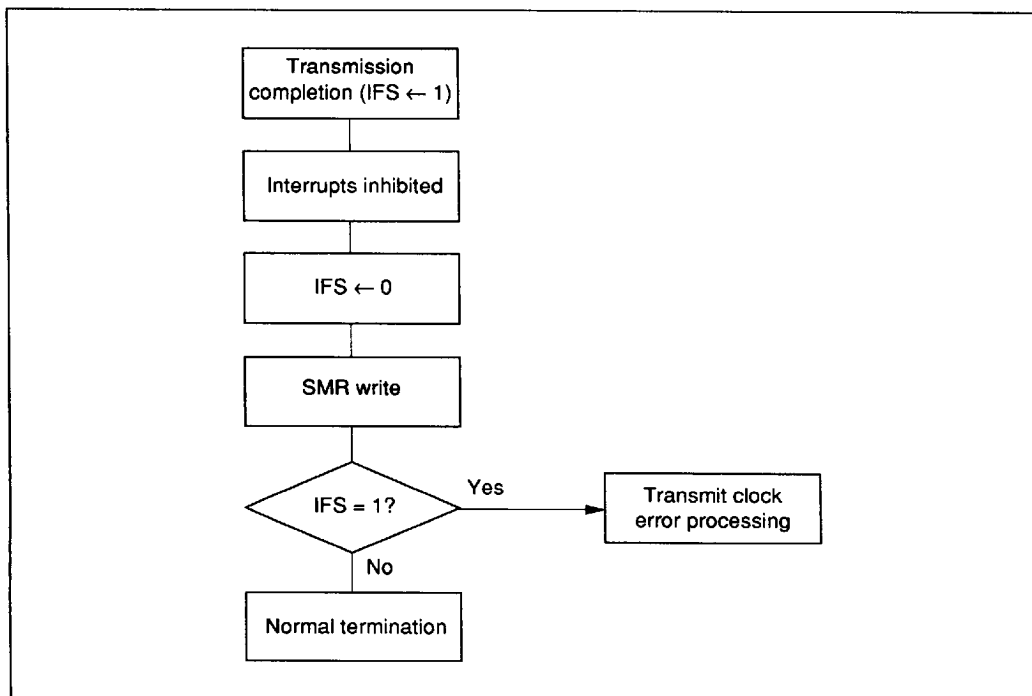
**Figure 33   Transmit Clock Error Detection**

## A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure four analog inputs with an eight-bit resolution. As shown in the block diagram of figure 34, the A/D converter has a four-bit A/D mode register, a one-bit A/D start flag, and a four-bit plus four-bit A/D data register.

**A/D Mode Register (AMR: $016):** Four-bit write-only register which selects the A/D conversion period and indicates analog input pin information. Bit 0 of the AMR selects the A/D conversion period, and bits 2 and 3 select a channel, as shown in figure 35.

**A/D Start Flag (ADSF: $020, Bit 2):** One-bit flag that initiates A/D conversion when 1 is written to it. At the completion of A/D conversion, the converted data is stored in the A/D data register and the ADSF is cleared. Refer to figure 35.

Note: Use the SEM and SEMD instructions to write data to the ADSF, but make sure that the ADSF is not written to during A/D conversion.

**A/D Data Register (ADRL: $017, ADRU: $018):** Eight-bit read-only register that is not cleared by a reset. Note that data read from this register during A/D conversion cannot be guaranteed. After the completion of A/D conversion, the resultant eight-bit data is held in this register, as shown in figure 36, until the start of the next conversion.

**Note on Use:** The contents of the A/D data register are not guaranteed during A/D conversion. To ensure that the A/D converter operates stably, do not execute port output instructions during A/D conversion.
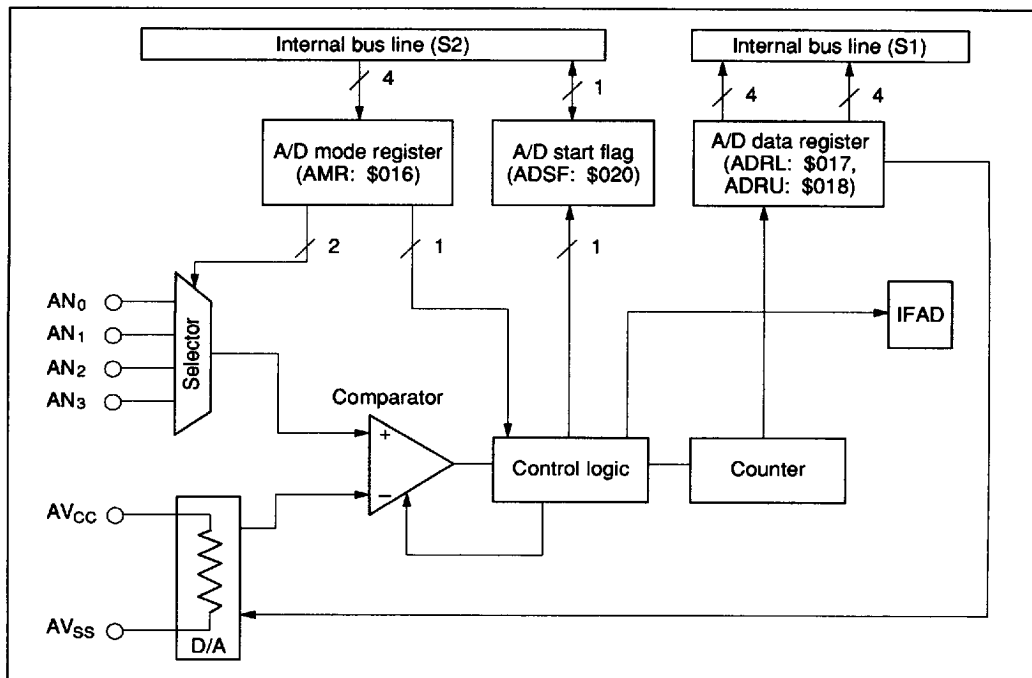


**Figure 34   A/D Converter Block Diagram**

**A/D mode register (AMR): $016**



Initial value: 0000, R/W: W

Switching time
Not used
Analog input selection
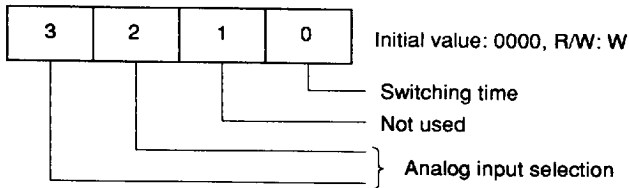
| AMR | Switching Time |
|-----|----------------|
| Bit 0 | |
| 0 | 34 $t_{cyc}$ |
| 1 | 67 $t_{cyc}$ |

| AMR | | Analog Input Selection |
|-----|-----|------------------------|
| Bit 3 | Bit 2 | |
| 0 | 0 | $AN_0$ |
| | 1 | $AN_1$ |
| 1 | 0 | $AN_2$ |
| | 1 | $AN_3$ |

**Special flag bits: $020**



LSON (refer to description of low-power dissipation modes)
WDON (refer to description of timers)
A/D start flag (ADSF)
DTON (refer to description of low-power dissipation modes)
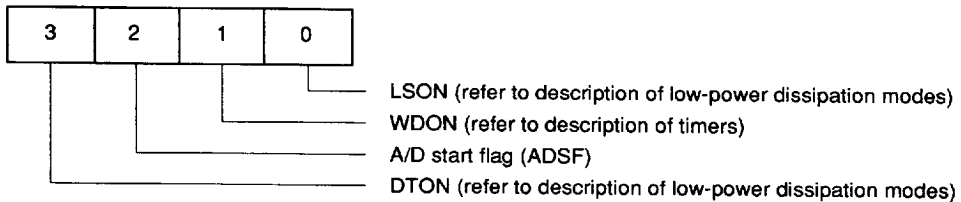
| Bit 2 | A/D Start Flag (ADSF) |
|-------|------------------------|
| 1 | A/D conversion started |
| 0 | A/D conversion completed |

**Figure 35   A/D Registers**

**ADRU: $018**    **ADRL: $017**



Result
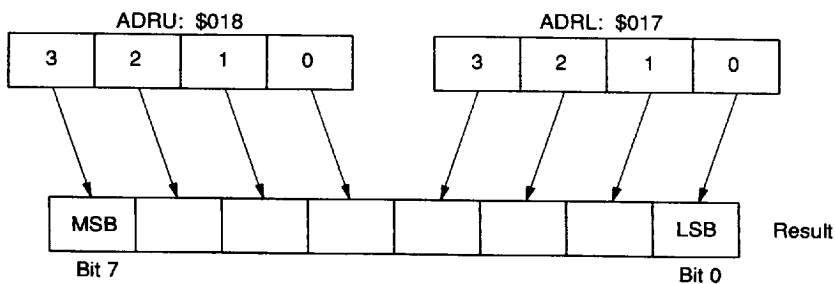
**Figure 36   A/D Data Registers**

## LCD Controller/Driver

The MCU has an LCD controller and driver which drive four common signal pins and 24 segment pins. The controller consists of a RAM area in which display data is stored, a display control register (LCR), and a duty cycle/clock control register (LMR), as shown in figures 37 and 38.

Four duty cycles and the LCD clock are program-controllable, and a built-in dual-port RAM ensures that display data can be automatically transmitted to the segment signal pins without program intervention. If a 32-kHz oscillation clock is selected as the LCD clock source, the LCD can be used even in watch mode, in which the system clock stops.
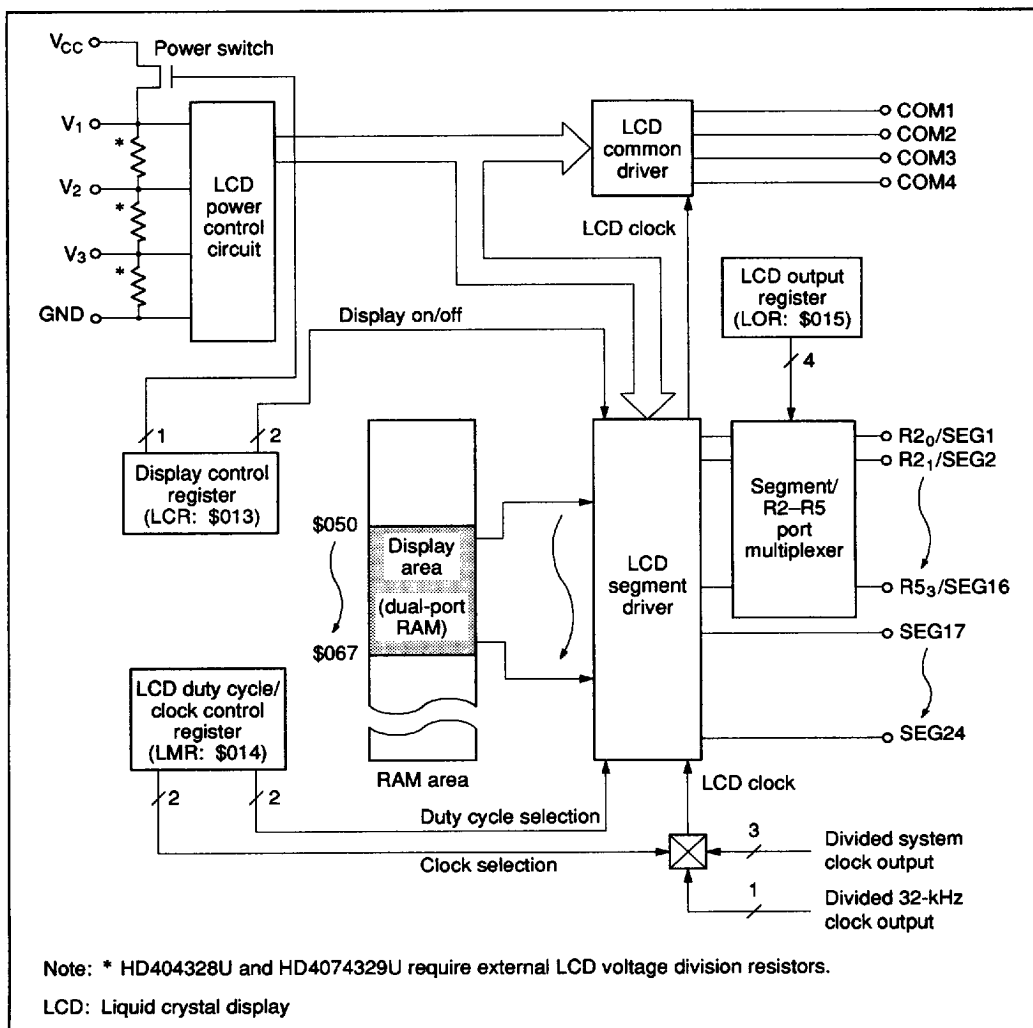


**Figure 37   Block Diagram of LCD Controller/Driver**

4496204 0047669 5TT

**LCD Data Area and Segment Data ($050–$067):** As shown in figure 39, each bit of the storage area corresponds to one of four duty cycles. If data is written to an area corresponding to a certain duty cycle, it is automatically output to the corresponding segments as display data.

**LCD Control Register (LCR: $013):** Three-bit write-only register which controls LCD blanking, the turning on and off of the liquid-crystal display's power supply division resistor, and display in watch and subactive modes, as shown in table 29.

**LCD control register (LCR): $013**

| ✕ | 2 | 1 | 0 | Initial value: 000, R/W: W |

- Blank/display
- Power switch on/off
- Display on/off in watch mode or subactive mode
- (not used)

**LCD mode register (LMR): $014**

| 3 | 2 | 1 | 0 | Initial value: 0000, R/W: W |

- } Duty cycle selection
- } Input clock selection

**LCD output register (LOR): $015**

| 3 | 2 | 1 | 0 | Initial value: 0000, R/W: W |

- R2/SEG1–SEG4 pin mode selection
- R3/SEG5–SEG8 pin mode selection
- R4/SEG9–SEG12 pin mode selection
- R5/SEG13–SEG16 pin mode selection
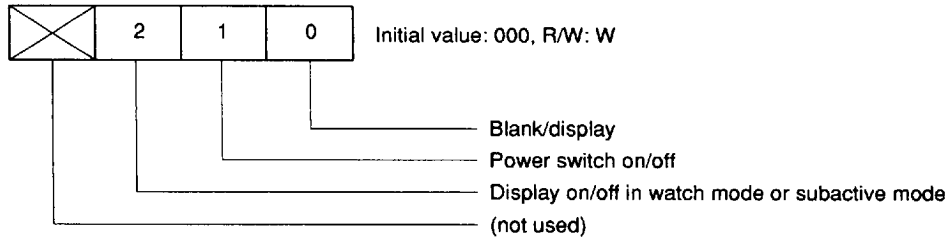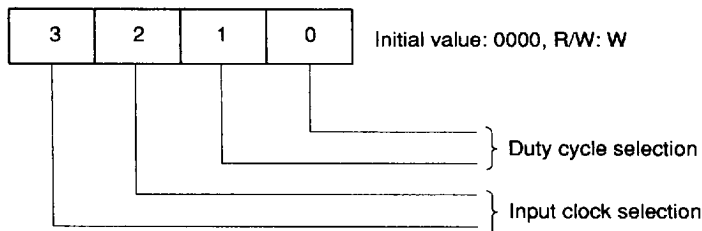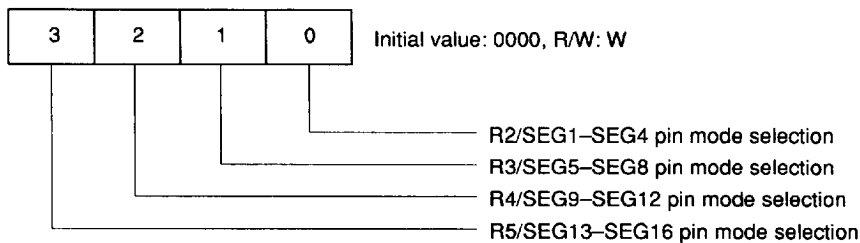
**Figure 38   LCD Registers**

- Blank/display
  Blank:     Segment signals are turned off, regardless of LCD RAM data setting.
  Display:  LCD RAM data is output as segment signals.

- Power switch on/off
  Off: The power switch is off.
  On: The power switch is on and $V_1$ is $V_{CC}$.

- Watch/subactive mode display
  Off: In watch and subactive modes, all common and segment pins are grounded and the liquid-crystal power switch is turned off.
  On: In watch and subactive modes, LCD RAM data is output as segment signals.

**LCD Duty Cycle/Clock Control Register (LMR: $014):** Four-bit write-only register which selects the display duty cycle and LCD clock source, as shown in table 30. The dependence of frame frequency on duty cycle is shown in table 31.

**LCD Output Register (LOR: $015):** Write-only register used to specify that ports R2–R5 act as pins SEG1–SEG16, as shown in table 32.

**Large Liquid-Crystal Panel Drive and $V_{LCD}$:** To drive a large-capacity LCD, decrease the resistance of the built-in division resistors by attaching external resistors in parallel, as shown in figure 40.

Since HD404328U and HD4074329U do not have built-in division resistors, they require external LCD voltage division resistors for voltage adjustment.

The size of these resistors cannot be simply calculated from the LCD load capacitance because the matrix configuration of the LCD complicates the paths of charge/discharge currents flowing through the capacitors—and the resistance will also vary with lighting conditions. This size must be determined by trial-and-error, taking into account the power dissipation of the device using the LCD, but a resistance of 1 kΩ to 10 kΩ would usually be suitable. (Another effective method is to attach capacitors of 0.1 µF to 0.3 µF.)

Always turn off the power switch (set bit 1 of the LCR to 0) before changing the liquid-crystal drive voltage ($V_{LCD}$).

|    | Bit 3 | Bit 2 | Bit 1 | Bit 0 |       |     | Bit 3 | Bit 2 | Bit 1 | Bit 0 |       |
|----|-------|-------|-------|-------|-------|-----|-------|-------|-------|-------|-------|
| 80 | SEG1  | SEG1  | SEG1  | SEG1  | $050  | 92  | SEG13 | SEG13 | SEG13 | SEG13 | $05C  |
| 81 | SEG2  | SEG2  | SEG2  | SEG2  | $051  | 93  | SEG14 | SEG14 | SEG14 | SEG14 | $05D  |
| 82 | SEG3  | SEG3  | SEG3  | SEG3  | $052  | 94  | SEG15 | SEG15 | SEG15 | SEG15 | $05E  |
| 83 | SEG4  | SEG4  | SEG4  | SEG4  | $053  | 95  | SEG16 | SEG16 | SEG16 | SEG16 | $05F  |
| 84 | SEG5  | SEG5  | SEG5  | SEG5  | $054  | 96  | SEG17 | SEG17 | SEG17 | SEG17 | $060  |
| 85 | SEG6  | SEG6  | SEG6  | SEG6  | $055  | 97  | SEG18 | SEG18 | SEG18 | SEG18 | $061  |
| 86 | SEG7  | SEG7  | SEG7  | SEG7  | $056  | 98  | SEG19 | SEG19 | SEG19 | SEG19 | $062  |
| 87 | SEG8  | SEG8  | SEG8  | SEG8  | $057  | 99  | SEG20 | SEG20 | SEG20 | SEG20 | $063  |
| 88 | SEG9  | SEG9  | SEG9  | SEG9  | $058  | 100 | SEG21 | SEG21 | SEG21 | SEG21 | $064  |
| 89 | SEG10 | SEG10 | SEG10 | SEG10 | $059  | 101 | SEG22 | SEG22 | SEG22 | SEG22 | $065  |
| 90 | SEG11 | SEG11 | SEG11 | SEG11 | $05A  | 102 | SEG23 | SEG23 | SEG23 | SEG23 | $066  |
| 91 | SEG12 | SEG12 | SEG12 | SEG12 | $05B  | 103 | SEG24 | SEG24 | SEG24 | SEG24 | $067  |
|    | COM4  | COM3  | COM2  | COM1  |       |     | COM4  | COM3  | COM2  | COM1  |       |

**Figure 39   Configuration of LCD RAM Area (for Dual-Port RAM)**

**Table 29   LCD Control Register**

| LCR Bit 2 | Display in Watch Mode or Subactive Mode | LCR Bit 1 | Power Switch On/Off | LCR Bit 0 | Blank/Display |
|---|---|---|---|---|---|
| 0 | Off | 0 | Off | 0 | Blank |
| 1 | On | 1 | On | 1 | Display |

Note:   When using an LCD in watch mode or subactive mode, use the divided output of a 32-kHz oscillator as the LCD clock and set bit 2 of the LCR to 1.  If using the divided output of the system clock as the LCD clock, always set bit 2 of the LCR to 0.

**Table 30   LCD Duty Cycle/Clock Control Register**

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Duty Selection/Input Clock Selection |
|---|---|---|---|---|
| — | — | 0 | 0 | 1/4 duty cycle |
|  |  |  | 1 | 1/3 duty cycle |
|  |  | 1 | 0 | 1/2 duty cycle |
|  |  |  | 1 | Static |
| 0 | 0 | — | — | CL0 (32.768/64 kHz when using a 32.768-kHz oscillator) |
|  | 1 |  |  | CL1 ($f_{cyc}$/256) |
| 1 | 0 |  |  | CL2 ($f_{cyc}$/2048) |
|  | 1 |  |  | CL3 (refer to table 31) |

Note:   $f_{cyc}$ is the divided system clock output.

### Table 31  LCD Frame Periods for Different Duty Cycles

**Static Duty Cycle**

| | LMR | | | |
|---|---|---|---|---|
| | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 |
| | 0     0 | 0     1 | 1     0 | 1     1 |
| Instruction Cycle Time | CL0 | CL1 | CL2 | CL3* |
| 2 µs | 512 Hz | 1953 Hz | 244 Hz | 122 Hz/64 Hz |

**1/2 Duty Cycle**

| | LMR | | | |
|---|---|---|---|---|
| | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 |
| | 0     0 | 0     1 | 1     0 | 1     1 |
| Instruction Cycle Time | CL0 | CL1 | CL2 | CL3* |
| 2 µs | 256 Hz | 976.5 Hz | 122 Hz | 61 Hz/32 Hz |

**1/3 Duty Cycle**

| | LMR | | | |
|---|---|---|---|---|
| | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 |
| | 0     0 | 0     1 | 1     0 | 1     1 |
| Instruction Cycle Time | CL0 | CL1 | CL2 | CL3* |
| 2 µs | 170.6 Hz | 651 Hz | 81.3 Hz | 40.6 Hz/21.3 Hz |

**1/4 Duty Cycle**

| | LMR | | | |
|---|---|---|---|---|
| | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 | Bit 3  Bit 2 |
| | 0     0 | 0     1 | 1     0 | 1     1 |
| Instruction Cycle Time | CL0 | CL1 | CL2 | CL3* |
| 2 µs | 128 Hz | 488.2 Hz | 61 Hz | 30.5 Hz/16 Hz |

Note:  * The division ratio depends on the value of bit 3 of timer mode register A (TMA);  the first value is for TMA3 = 0 and the second is for TMA3 = 1.

When TMA3 = 0, CL3 = $f_{cyc}/4096$.
When TMA3 = 1, CL3 = 32.768 kHz/512.

### Table 32  LCD Output Register

| LOR | | LOR | | LOR | | LOR | |
|---|---|---|---|---|---|---|---|
| Bit 3 | Port Selection | Bit2 | Port Selection | Bit 1 | Port Selection | Bit 0 | Port Selection |
| 0 | R5 | 0 | R4 | 0 | R3 | 0 | R2 |
| 1 | SEG16–SEG13 | 1 | SEG12–SEG9 | 1 | SEG8–SEG5 | 1 | SEG4–SEG1 |
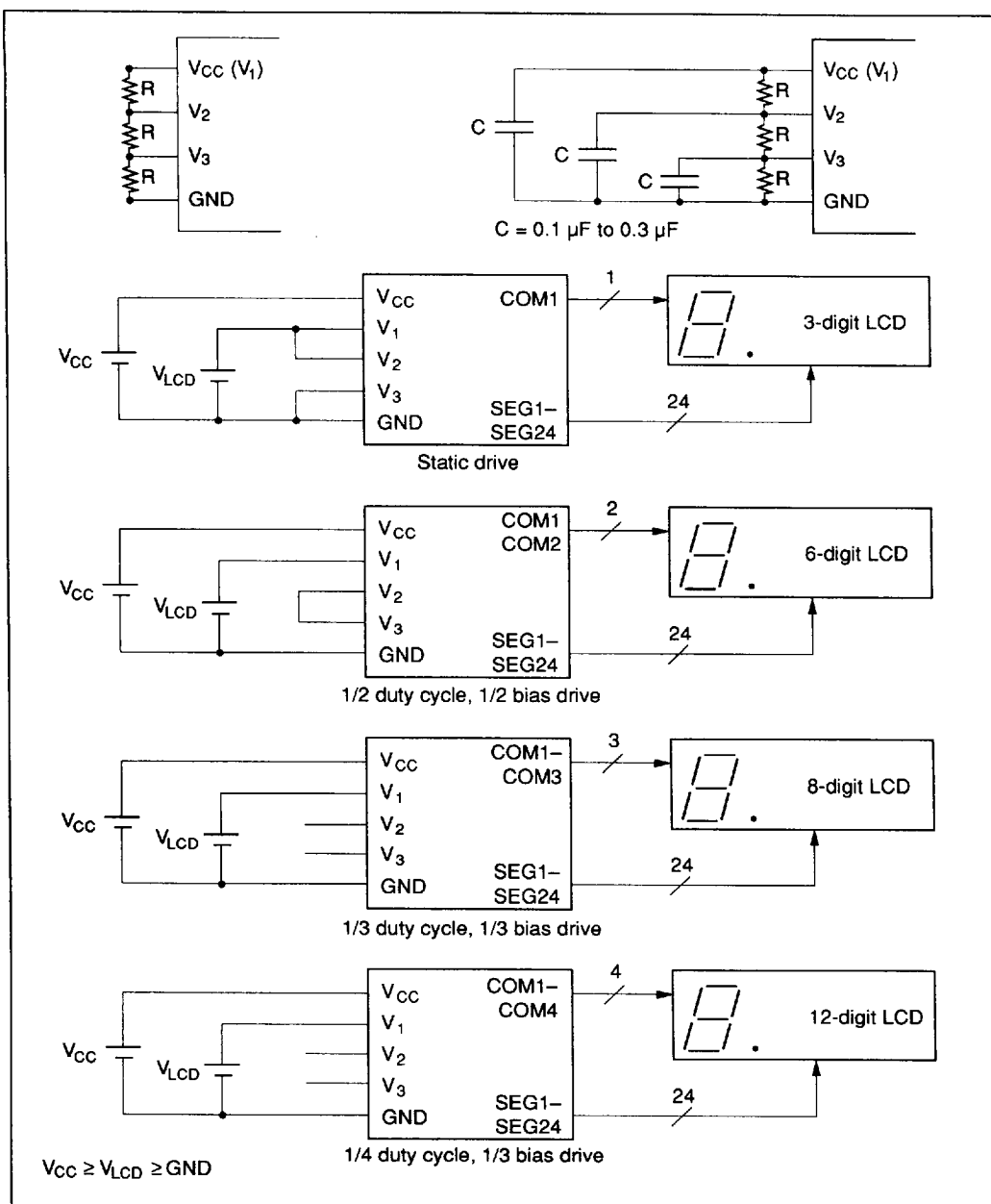
**Figure 40   LCD Connection Examples**

## Zero-Crossing Detection Circuit

The MCU has a zero-crossing detection circuit that generates a digital signal in synchronism with an AC signal input to the ZCD pin through an external capacitor. A block diagram of the zero-crossing detection circuit is shown in figure 41.

The zero-crossing detection circuit has two modes (low sensitivity mode and high sensitivity mode) which are set by port mode register B (PMRB: $011) as shown in table 33.

A digital signal generated by the zero-crossing detection circuit sets the zero-crossing interrupt request flag (IFZC). The interrupt edge is selected by the interrupt mode register (IMR: $010). This signal can be made as the input clock of timer B by setting the input clock source of timer mode register B (TMB: $009) for external event input.

Note: After MCU reset, the $D_8$/ZCD/$\overline{EVENT}$ pin is set to ZCD. With this setting, a supply current (bias current) always flows because a bias circuit within the zero-crossing circuit is still operating. This current flows in all MCU operation modes, but it is particularly critical in stop mode because the MCU is more affected by bias current since the other circuits of the LSI are not dissipating much current. If the zero-crossing detection function is not being used, use port mode register B to set this pin to $D_8$ or $\overline{EVENT}$. This prevents the bias current from flowing.
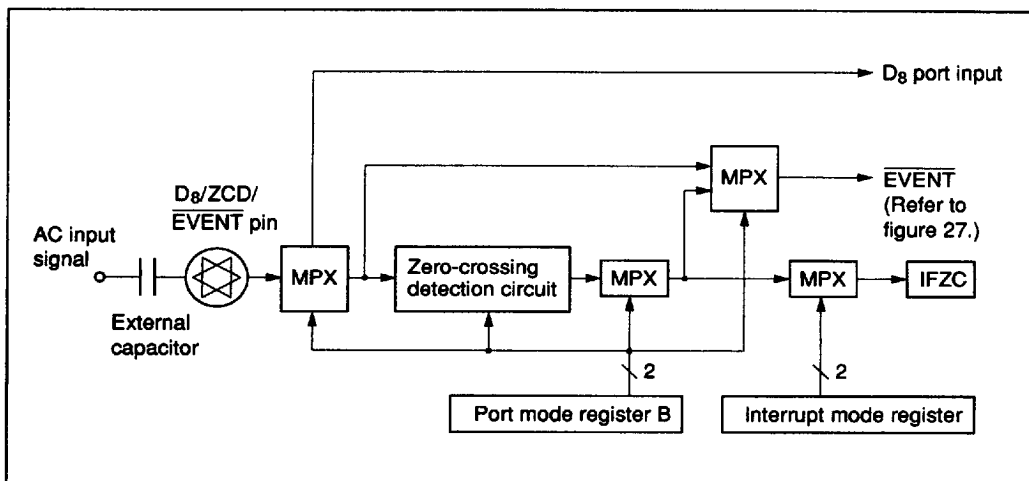


**Figure 41   Block Diagram of Zero-Crossing Detection Circuit**

**Table 33   Port Mode Register B**

| PMRB | | Port Selection |
|---|---|---|
| 1 | 0 | |
| 0 | 0 | ZCD (low sensitivity mode) |
| | 1 | ZCD (high sensitivity mode)* |
| 1 | 0 | $D_8$ |
| | 1 | $\overline{EVENT}$ |

Note:  * Becomes low sensitivity in subactive mode.

**Table 34 Registers in Special Register Area**

| Name | Address | R/W | Bit | Description |
|------|---------|-----|-----|-------------|
| PMRA | $004 | W | 0 | $R1_2/S0$ pin mode selection |
| | | | 1 | $R1_1/SI$ pin mode selection |
| | | | 2 | $D_9/\overline{INT_0}$ pin mode selection |
| | | | 3 | $D_{10}/INT_1$ pin mode selection |
| SMR | $005 | W | 2–0 | Serial transmit clock speed selection |
| | | | 3 | $R1_0/\overline{SCK}$ pin mode selection |
| SRL | $006 | R/W | 3–0 | Serial interface data register, lower 4 bits |
| SRU | $007 | R/W | 3–0 | Serial interface data register, upper 4 bits |
| TMA | $008 | W | 2–0 | Input clock selection (timer A) |
| | | | 3 | Timer-A/time-base mode selection |
| TMB | $009 | W | 2–0 | Input clock selection (timer B) |
| | | | 3 | Auto-reload function selection |
| TCBL/TLRL | $00A | R/W | 3–0 | Timer counter/timer load register (timer B), lower 4 bits |
| TCBU/TLRU | $00B | R/W | 3–0 | Timer counter/timer load register (timer B), upper 4 bits |
| MIS | $00C | W | 1, 0 | Interrupt frame period selection |
| | | | 2 | $R1_2/SO$ PMOS off |
| | | | 3 | Changeover to setting by system oscillator frequency |
| TMC | $00D | W | 2–0 | Input clock selection (timer C) |
| | | | 3 | Auto-reload function selection |
| TCCL/TCRL | $00E | R/W | 3–0 | Timer counter/timer load register (timer C), lower 4 bits |
| TCCU/TCRU | $00F | R/W | 3–0 | Timer counter/timer load register (timer C), upper 4 bits |
| IMR | $010 | W | 1, 0 | $INT_1$ detection edge selection |
| | | | 3, 2 | Zero-crossing detection edge selection |
| PMRB | $011 | W | 1, 0 | $D_8/ZCD/\overline{EVENT}$ pin mode selection |
| | | | 3, 2 | Do not use |
| PMRC | $012 | W | 1, 0 | Buzzer frequency selection |
| | | | 2 | $R1_3/$ BUZZ pin mode selection |
| | | | 3 | Pull-up MOS transistor on/off selection |
| LCR | $013 | W | 0 | LCD display selection |
| | | | 1 | LCD power switch on/off selection |
| | | | 2 | LCD display selection during watch mode |
| | | | 3 | Do not use |
| LMR | $014 | W | 1, 0 | LCD duty cycle selection |
| | | | 3, 2 | LCD input clock selection |

**Table 34   Registers in Special Register Area (cont)**

| Name | Address | R/W | Bit | Description |
|------|---------|-----|-----|-------------|
| LOR | $015 | W | 0 | R2/SEG1–SEG4 pin mode selection |
| | | | 1 | R3/SEG5–SEG8 pin mode selection |
| | | | 2 | R4/SEG9–SEG12 pin mode selection |
| | | | 3 | R5/SEG13–SEG16 pin mode selection |
| AMR | $016 | W | 0 | Conversion timing selection (A/D) |
| | | | 1 | Do not use |
| | | | 3, 2 | Analog input selection (A/D) |
| ADRL | $017 | R | 3–0 | A/D data register, lower 4 bits |
| ADRU | $018 | R | 3–0 | A/D data register, upper 4 bits |
| DCR0 | $030 | W | 3–0 | Data control register for port R0 |
| DCR1 | $031 | W | 3–0 | Data control register for port R1 |
| DCR2 | $032 | W | 3–0 | Data control register for port R2 |
| DCR3 | $033 | W | 3–0 | Data control register for port R3 |
| DCR4 | $034 | W | 3–0 | Data control register for port R4 |
| DCR5 | $035 | W | 3–0 | Data control register for port R5 |
| DCRB | $03B | W | 3–0 | Data control register for port $D_0$–$D_3$ |
| DCRC | $03C | W | 3–0 | Data control register for port $D_4$–$D_7$ |
| DCRD | $03D | W | 0 | Data control register for port $D_8$ |
| | | | 3–1 | Do not use |

## PROM Mode Description

### Programming the Built-In ROM

The MCU's built-in ROM is programmed in PROM mode in which the pins are arranged as shown in figure 42. PROM mode is set by pulling $\overline{\text{TEST}}$, $\overline{\text{M}_0}$, and $\overline{\text{M}_1}$ low, and RESET high as shown in figure 43. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 64-to-28–pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 35.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower five bits and an upper five bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.
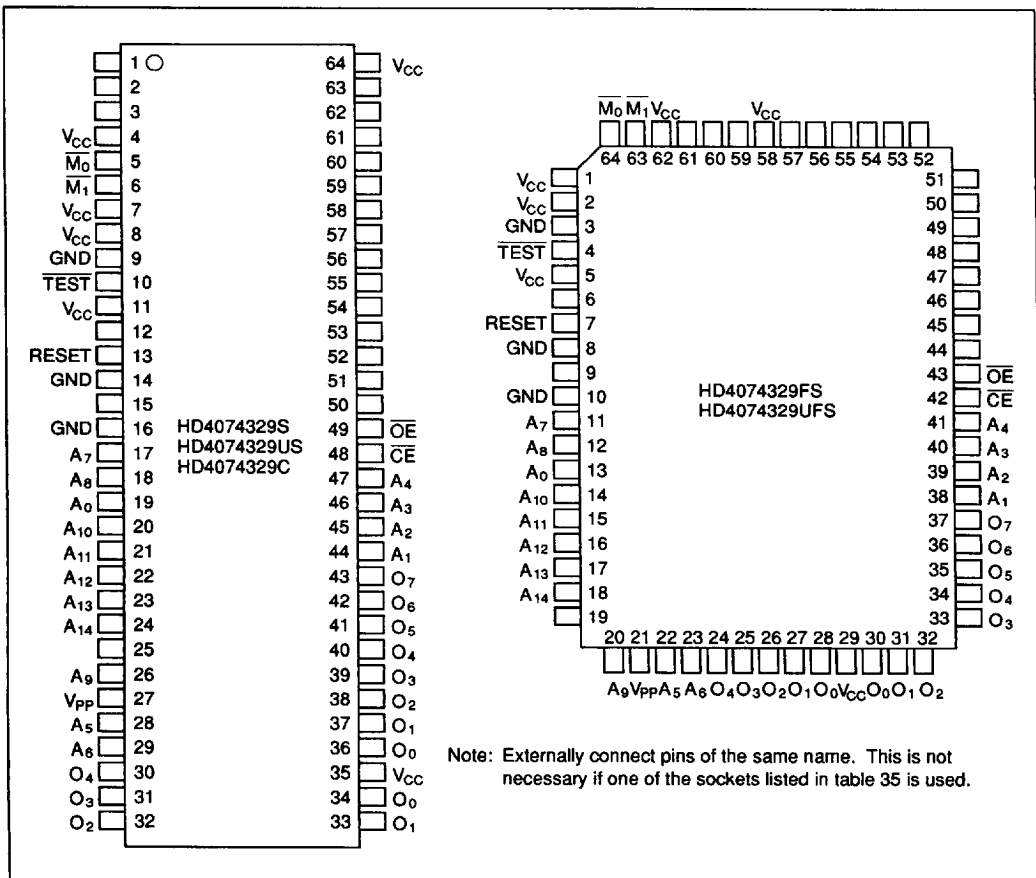


**Figure 42   Pin Arrangement in PROM Mode**
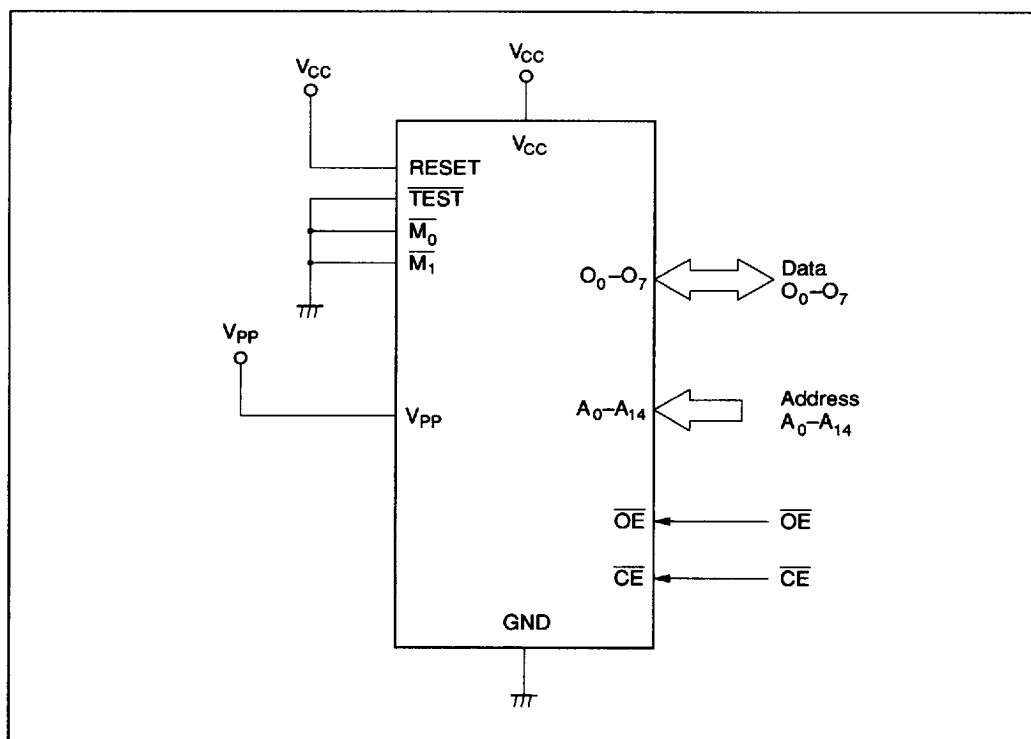
**Figure 43  PROM Mode Connections**

**Table 35  Recommended PROM Programmers and Socket Adapters**

| PROM Programmer | | Socket Adapter | | |
|---|---|---|---|---|
| Manufacturer | Model Name | Package | Model Name | Manufacturer |
| DATA I/O Corp. | 29B | DP-64S DC-64S | HS432ESS01H | Hitachi |
| | | FP-64B | HS432ESF01H | Hitachi |
| AVAL Data Corp. | PKW-1000 | DP-64S DC-64S | HS432ESS01H | Hitachi |
| | | FP-64B | HS432ESF01H | Hitachi |

**Table 36  PROM Mode Selection**

| Mode | Pin | | | |
|---|---|---|---|---|
| | $\overline{CE}$ | $\overline{OE}$ | $V_{PP}$ | $O_0$–$O_7$ |
| Programming | Low | High | $V_{PP}$ | Data input |
| Verification | High | Low | $V_{PP}$ | Data output |
| Programming inhibited | High | High | $V_{PP}$ | High impedence |

## Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed, but the ceramic window-package version can be reprogrammed after being exposed to ultraviolet light.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed in the programmer.

3. PROM programmers have two voltages ($V_{PP}$): 12.5 V and 21 V. Remember that ZTAT™ devices require a $V_{PP}$ of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

**Programming and Verification:** The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 36.

For details of PROM programming, refer to the Notes on PROM Programming section.

### Erasure (Window Package)

Data in the PROM is erased by exposing the LSI to ultraviolet light of a wavelength of 2537 Å for an integrated dose of at least 15 W.s/cm². These conditions can be satisfied by placing the LSI about 2 cm to 3 cm away from an ultraviolet lamp with a rating of 12,000 µW/cm² for about 20 minutes. After erasure, all PROM bits are set to 1.

For details of packages with windows, refer to the Notes on Window Packages section.

## Addressing Modes

### RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 44 and described below.

**Register Indirect Addressing Mode:** The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

**Direct Addressing Mode:** A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

**Memory Register Addressing Mode:** The memory registers (MR), which consist of 16 digits from $040–$04F, are accessed with the LAMR and XMRA instructions.
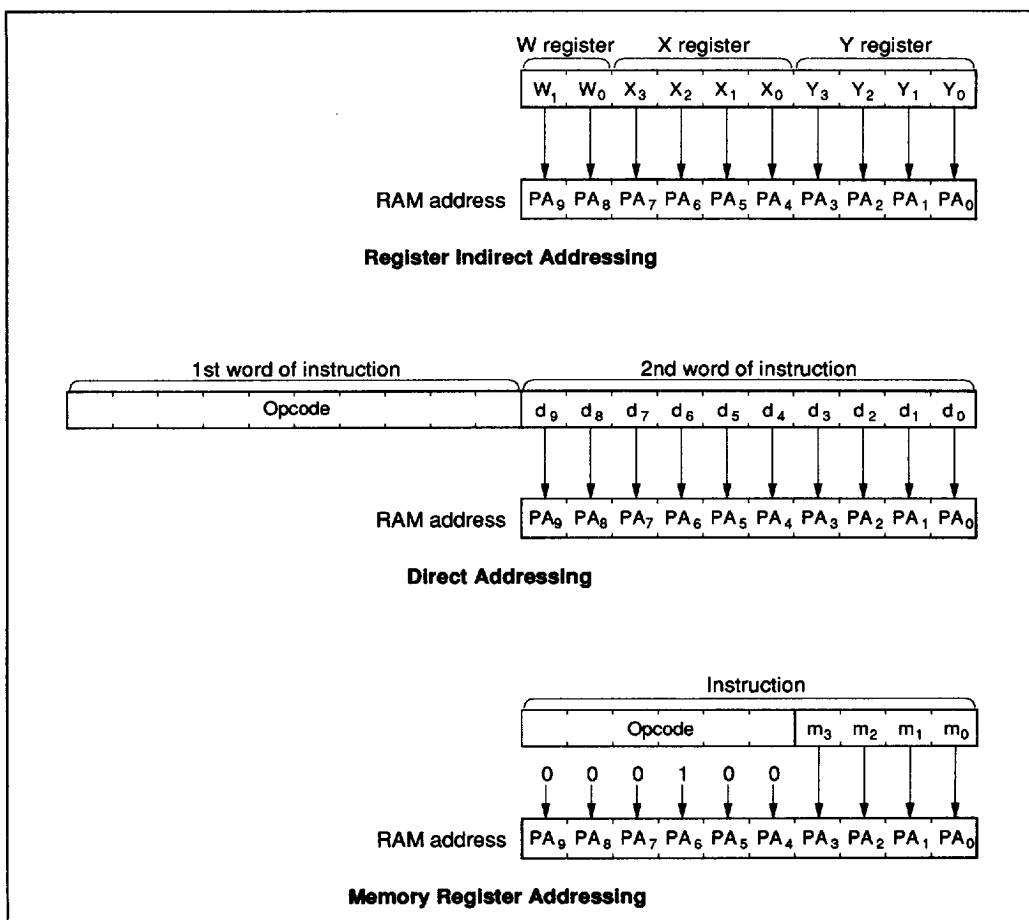
Figure 44   RAM Addressing Modes

## ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 45 and described below.

**Direct Addressing Mode:** A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits ($PC_{13}$–$PC_0$) with 14-bit immediate data.

**Current Page Addressing Mode:** The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter ($PC_7$–$PC_0$) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 47. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-Series cross macroassembler has an automatic paging feature for ROM pages.

**Zero-Page Addressing Mode:** A program can branch to the zero-page subroutine area located at $000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter ($PC_5$–$PC_0$), and 0s are placed in the eight high-order bits ($PC_{13}$–$PC_6$).

**Table Data Addressing Mode:** A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

**P Instruction:** ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 46. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R0 and R1 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R0 and R1 port output registers at the same time.
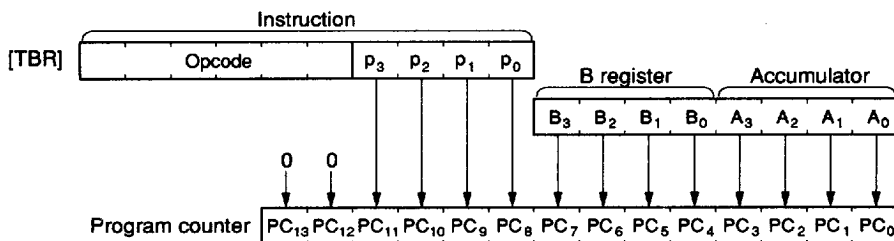
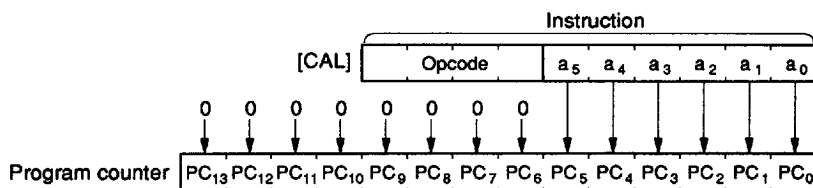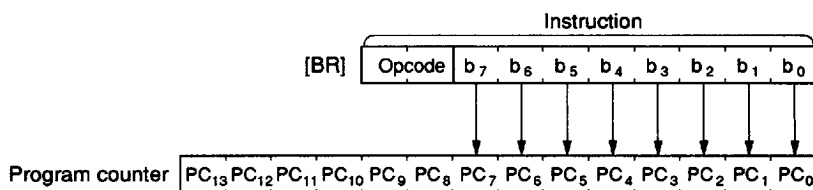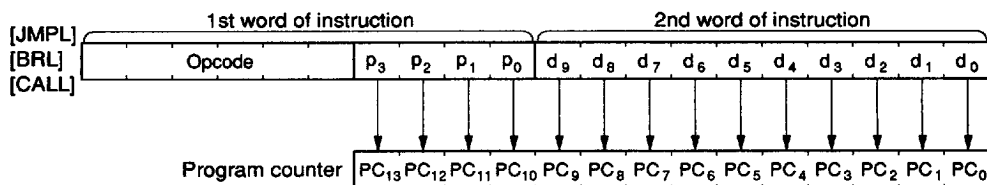The P instruction has no effect on the program counter.

**Figure 45  ROM Addressing Modes**

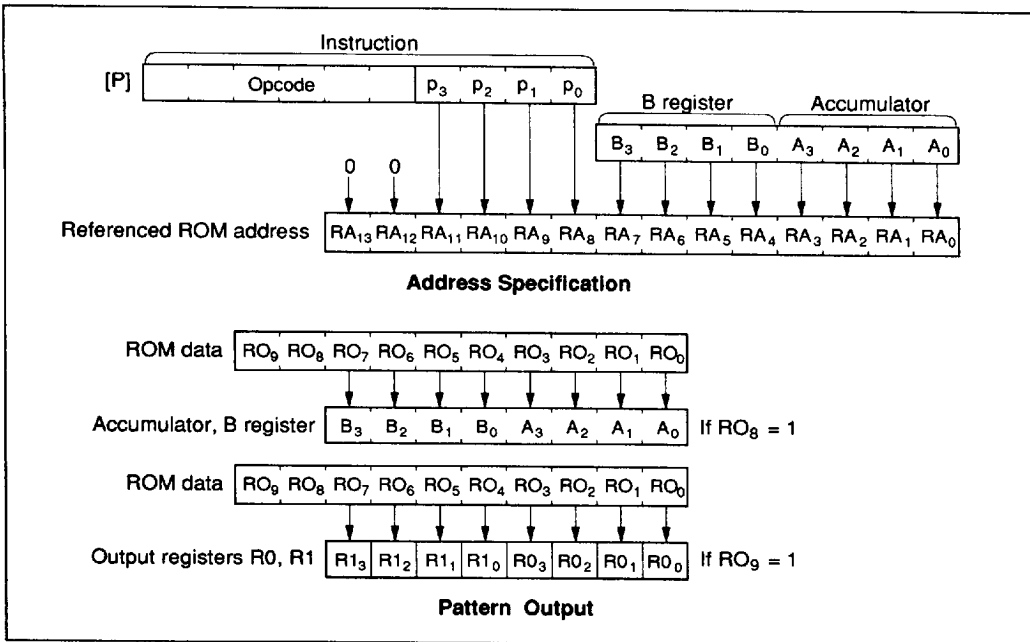**Figure 46   P Instruction**



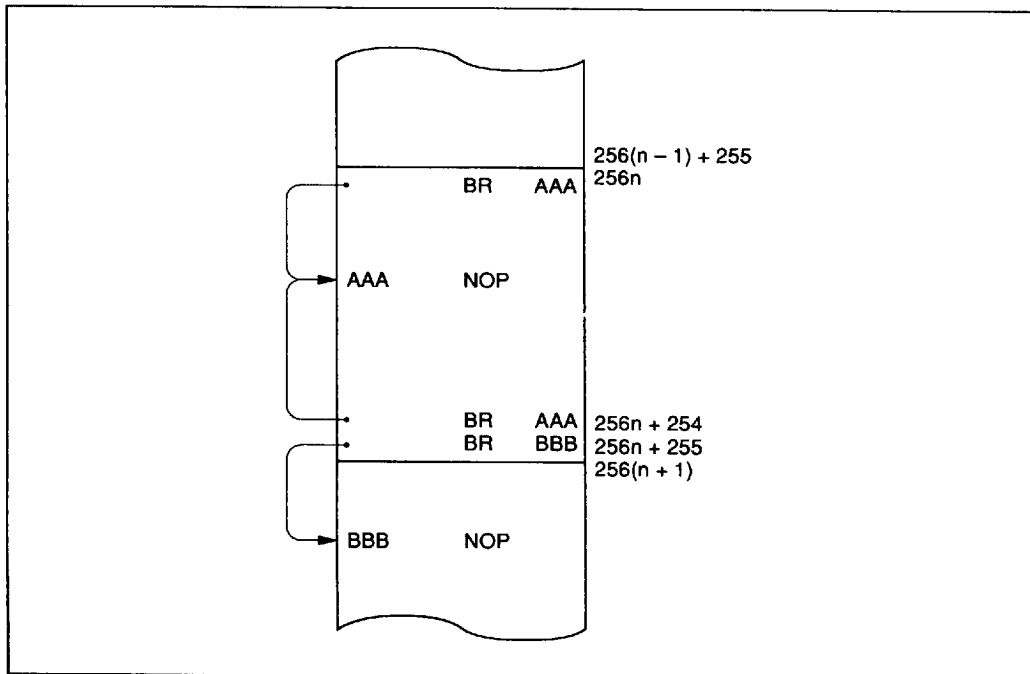**Figure 47   Branching when Branch Destination is on a Page Boundary**

## Absolute Maximum Ratings

| Item | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Power voltage | $V_{CC}$ | −0.3 to +7.0 | V | |
| Programming voltage | $V_{PP}$ | −0.3 to +14.0 | V | 1 |
| Pin voltage | $V_T$ | −0.3 to ($V_{CC}$ + 0.3) | V | |
| Total permissible input current | $\Sigma I_o$ | 100 | mA | 2 |
| Total permissible output current | $-\Sigma I_o$ | 50 | mA | 3 |
| Maximum input current | $I_o$ | 4 | mA | 4, 5 |
| | | 30 | mA | 4, 6 |
| Maximum output current | $-I_o$ | 4 | mA | 7, 8 |
| Operating temperature | $T_{opr}$ | HD404328, HD4074329, HD4074329U: −20 to +75 | °C | |
| | | HD404328U: −40 to +85 | °C | |
| Storage temperature | $T_{stg}$ | −55 to +125 | °C | |

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the Electrical Characteristics table. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. $D_{10}$ ($V_{PP}$) of the HD4074329 and HD4074329U.
2. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to ground.
3. The total permissible output current is the total of output currents simultaneously flowing out from $V_{CC}$ to all I/O pins.
4. The maximum input current is the maximum current flowing from any I/O pin to ground.
5. Applies to $D_8$, R0–R5.
6. Applies to $D_0$–$D_7$.
7. The maximum output current is the maximum current flowing from $V_{CC}$ to any I/O pin.
8. Applies to $D_0$–$D_8$, R0–R5.

## Electrical Characteristics

### DC Characteristics

(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;
HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | RESET, $\overline{SCK}$, $\overline{INT_0}$, $INT_1$, SI, $\overline{EVENT}$ | $0.8V_{CC}$ | — | $V_{CC}$ + 0.3 | V | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | |
| | | | $0.9V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | $OSC_1$ | $V_{CC}$ – 0.5 | — | $V_{CC}$ + 0.3 | V | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | |
| | | | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | RESET, $\overline{SCK}$, $\overline{INT_0}$, $INT_1$, $\overline{EVENT}$, SI | –0.3 | — | $0.2V_{CC}$ | V | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | |
| | | | –0.3 | — | $0.1V_{CC}$ | V | | |
| | | $OSC_1$ | –0.3 | — | 0.5 | V | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | |
| | | | –0.3 | — | 0.3 | V | | |
| Output high voltage | $V_{OH}$ | $\overline{SCK}$, SO, BUZZ | $V_{CC}$ – 1.0 | — | — | V | $-I_{OH}$ = 0.5 mA | |
| Output low voltage | $V_{OL}$ | $\overline{SCK}$, SO, BUZZ | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| I/O leakage current | $|I_{IL}|$ | RESET, $\overline{SCK}$, $\overline{INT_0}$, $INT_1$, SI SO, $OSC_1$, BUZZ | — | — | 1.0 | μA | $V_{in}$ = 0 to $V_{CC}$ | 1 |

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# HD404328 Series

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Current dissipation in active mode | $I_{CC}$ | $V_{CC}$ | — | 3 | 6 | mA | $V_{CC}$ = 5.0 V, $f_{OSC}$ = 4 MHz | 2, 4 |
| Current dissipation in standby mode | $I_{SBY}$ | $V_{CC}$ | — | 0.6 | 1.5 | mA | $V_{CC}$ = 3.0 V, LCD on | 3, 4 |
| Current dissipation in subactive mode | $I_{SUB}$ | $V_{CC}$ | — | 50 | 70 | µA | HD404328: $V_{CC}$ = 3.0 V, LCD on | |
| | | | — | 40 | 60 | µA | HD404328U: $V_{CC}$ = 3.0 V, LCD on | |
| | | | — | 70 | 150 | µA | HD4074329: $V_{CC}$ = 3.0 V, LCD on | |
| | | | — | 60 | 140 | µA | HD4074329U: $V_{CC}$ = 3.0 V, LCD on | |
| Current dissipation in watch mode (1) | $I_{WTC1}$ | $V_{CC}$ | — | 4 | 15 | µA | $V_{CC}$ = 3.0 V, LCD off | 5 |
| Current dissipation in watch mode (2) | $I_{WTC2}$ | $V_{CC}$ | — | 15 | 35 | µA | HD404328, HD4074329: $V_{CC}$ = 3.0 V, LCD on | 5 |
| | | | — | 5 | 25 | µA | HD404328U, HD4074329U: $V_{CC}$ = 3.0 V, LCD on | 5 |
| Current dissipation in stop mode | $I_{STOP}$ | $V_{CC}$ | — | 1 | 10 | µA | $V_{CC}$ = 3.0 V, X1 = $V_{CC}$ | 5 |
| Stop mode retain voltage | $V_{STOP}$ | $V_{CC}$ | 2 | — | — | V | No 32-kHz oscillator | 6 |

Notes on next page.

Notes: 1. Output buffer current is excluded.
2. $I_{CC1}$ is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions:    MCU: Reset
   Pins: RESET, $\overline{TEST}$, $D_0$–$D_7$, $D_9$, $D_{10}$, R0–R5 at $V_{CC}$
   $D_8$ open
3. $I_{SBY}$ is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions:    MCU: I/O reset
   Serial interface stopped
   Standby mode
   Pins: RESET at GND
   $\overline{TEST}$, $D_0$–$D_7$, $D_9$, $D_{10}$, R0–R5 at $V_{CC}$
   $D_8$ open
4. The power dissipation is in proportion to $f_{OSC}$ only when the MCU is operating or is in standby mode. The value of the dissipation current when $f_{OSC}$ = x MHz is given by the following equation:
   Maximum value ($f_{OSC}$ = x MHz) = x/4 × maximum value ($f_{OSC}$ = 4 MHz)
5. $D_{10}$ is connected to $V_{CC}$ in the HD4074329 and HD4074329U.
6. RAM data retention.

## I/O Characteristics for Standard Pins
**(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;**
**HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;**
**HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;**
**unless otherwise specified)**

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_8$–$D_{10}$, R0–R5 | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_8$–$D_{10}$, R0–R5 | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | $D_8$, R0–R5 | $V_{CC}$ – 1.0 | — | — | V | $-I_{OH}$ = 0.5 mA | |
| Output low voltage | $V_{OL}$ | $D_8$, R0–R5 | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| I/O leakage current | $|I_{IL}|$ | $D_8$, $D_9$, R0–R5 | — | — | 1.0 | μA | $V_{in}$ = 0 to $V_{CC}$ | * |
| | | $D_{10}$ | — | — | 1.0 | μA | HD404328, HD404328U: $V_{in}$ = 0 to $V_{CC}$ | * |
| | | | — | — | 20.0 | μA | HD4074329, HD4074329U: $V_{in}$ = 0 to $V_{CC}$ | |
| Pull-up MOS current | $-I_{pu}$ | $D_8$, R0–R5 | 5 | 25 | 90 | μA | $V_{CC}$ = 3.0 V, $V_{in}$ = 0.0 V | |

Note: * Output buffer current is excluded.

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## HD404328 Series

**I/O Characteristics for High-Current Pins**
(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;
HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_0$–$D_7$ | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_0$–$D_7$ | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | $D_0$–$D_7$ | $V_{CC}$ – 1.0 | — | — | V | $-I_{OH}$ = 0.5 mA | |
| Output low voltage | $V_{OL}$ | $D_0$–$D_7$ | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| | | | — | — | 2.0 | V | HD404328, HD404328U: $I_{OL}$ = 15 mA, $V_{CC}$ = 4.5 V to 6.0 V | |
| | | | — | — | — | | HD4074329, HD4074329U: $I_{OL}$ = 15 mA, $V_{CC}$ = 4.5 V to 5.5 V | |
| I/O leakage current | $|I_{IL}|$ | $D_0$–$D_7$ | — | — | 1.0 | μA | $V_{in}$ = 0 to $V_{CC}$ | * |
| Pull-up MOS current | $-I_{pu}$ | $D_0$–$D_7$ | 5 | 25 | 90 | μA | $V_{CC}$ = 3.0, $V_{in}$ = 0 | |

Note: * Output buffer current is excluded.

**LCD Circuit Characteristics**
(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;
HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| Segment driver voltage drop | $V_{DS}$ | SEG1–SEG24 | — | — | 0.6 | V | $I_d$ = 3.0 μA | 1 |
| Common driver voltage drop | $V_{DC}$ | COM1–COM4 | — | — | 0.3 | V | $I_d$ = 3.0 μA | 1 |
| LCD power supply division resistor | $R_W$ | | 100 | 300 | 900 | kΩ | HD404328, HD4074329: Between $V_1$ and GND, $V_1$ = $V_{CC}$ | |
| LCD voltage | $V_{LCD}$ | $V_1$ | 2.7 | — | $V_{CC}$ | V | HD404328, HD404328U | 2 |
| | | | 2.9 | — | $V_{CC}$ | V | HD4074329, HD4074329U | 2 |

Notes: 1. $V_{DS}$ and $V_{DC}$ are the voltage drops from power supply pins $V_1$, $V_2$, and $V_3$, and GND to each segment pin and each common pin.
2. When $V_{LCD}$ is supplied from an external source, the following relations must be retained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq$ GND

## A/D Converter Characteristics

(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, $AV_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C;
HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, $AV_{SS}$ = 0.0 V, $T_a$ = –40°C to +85°C;
HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, $AV_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Note |
|------|--------|--------|-----|-----|-----|------|-----------------|------|
| Analog power voltage | $AV_{CC}$ | $AV_{CC}$ | $V_{CC} - 0.3$ | $V_{CC}$ | $V_{CC} + 0.3$ | V | | |
| Analog input voltage | $AV_{in}$ | $AN_0$–$AN_3$ | $AV_{SS}$ | — | $AV_{CC}$ | V | | |
| Current between $AV_{CC}$ and $AV_{SS}$ | $I_{AD}$ | — | — | 50 | — | μA | $V_{CC} = AV_{CC} = 5.0$ V | |
| Analog input capacitance | $CA_{in}$ | $AN_0$–$AN_3$ | — | 30 | — | pF | | |
| Resolution | | | 8 | 8 | 8 | Bit | | |
| Number of inputs | | | 0 | — | 4 | Channel | | |
| Absolute accuracy | | | — | — | ±2.0 | LSB | | * |
| Conversion period | | | 34 | — | 67 | $t_{cyc}$ | | |
| Analog input impedance | | $AN_0$–$AN_3$ | 1 | — | — | MΩ | f = 1 MHz, $V_{in}$ = 0.0 V | |

Note: * Operating frequency of A/D conversion $f_{OSC}$ is from 1 (MHz) to 4.5 (MHz).

## Zero-Crossing Detection Circuit Characteristics

### Low Sensitivity Mode

(HD404328, HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = 0°C to +70°C;
HD4074329, HD4074329U: $V_{CC}$ = 3.0 V to 5.5 V, GND = 0.0 V, $T_a$ = 0°C to +70°C;
unless otherwise specified)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Conditions | Note |
|------|--------|-----|-----|-----|-----|------|-----------------|------|
| Zero-crossing detection input voltage | $V_{ZC}$ | ZCD | 2.0 | — | 3.0 | $V_{P-P}$ | AC connection, C = 0.1 μF | |
| Zero-crossing detection accuracy | $V_{AZC}$ | | — | — | ±750 | mV | $f_{ZC}$ = 50/60 Hz (sine wave), $f_{OSC}$ = 4 MHz | Refer to figure 48 |
| Zero-crossing detection input frequency | $f_{ZC}$ | | 45 | — | 250 | Hz | | |

# HD404328 Series

High Sensitivity Mode ($V_{CC}$ = 5.0 V, GND = 0.0 V, $T_a$ = 0°C to 70°C, unless otherwise specified)

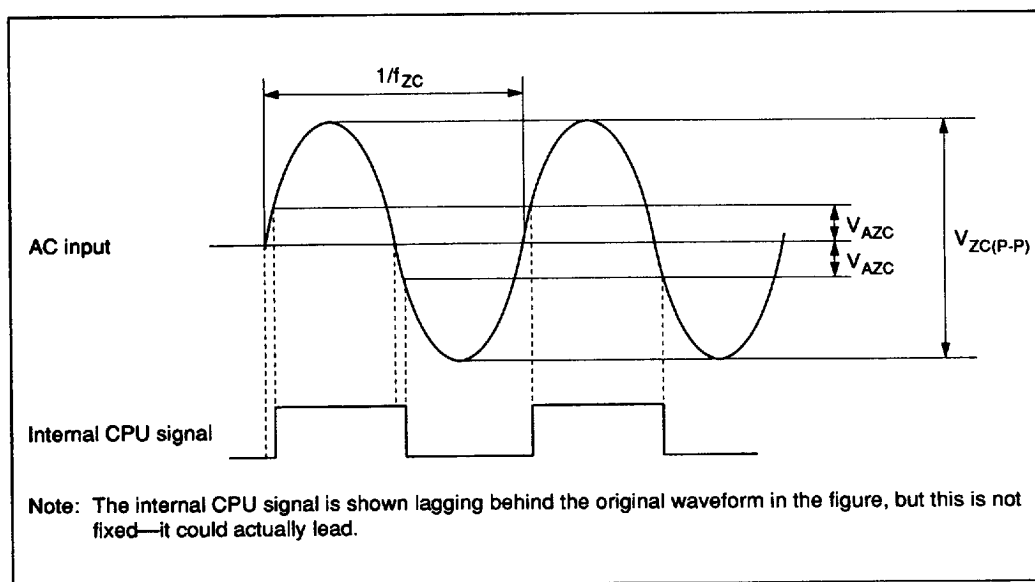| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Conditions | Note |
|------|--------|-----|-----|-----|-----|------|-----------------|------|
| Zero-crossing detection input voltage | $V_{ZC}$ | ZCD | 2.0 | — | 3.0 | $V_{P-P}$ | AC connection, C = 0.1 μF | |
| Zero-crossing detection accuracy | $V_{AZC}$ | | — | — | ±100 | mV | $f_{ZC}$ = 50/60 Hz (sine wave), $f_{OSC}$ = 4 MHz, $V_{CC}$ = 5.0 V | Refer to figure 48 |
| Zero-crossing detection input frequency | $f_{ZC}$ | | 45 | — | 1000 | Hz | | |



Figure 48  Zero-Crossing Detection

## AC Characteristics
(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;
HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Note |
|------|--------|--------|-----|-----|-----|------|-----------------|------|
| Clock oscillation frequency | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 0.4 | 4.0 | 4.5 | MHz | 1/8 division, 32 kHz used | 1 |
| | | | 0.4 | 4.0 | 4.5 | MHz | 1/8 division used, 32 kHz not used | |
| | | X1, X2 | — | 32.768 | — | kHz | | |
| Instruction cycle time | $t_{cyc}$ | | — | 2 | — | µs | $f_{OSC}$ = 4 MHz | |
| Oscillation stabilization time (crystal) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 40 | ms | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | 2 |
| | | | — | — | 60 | ms | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | 2 |
| Oscillation stabilization time (ceramic) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 20 | ms | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | 2 |
| | | | — | — | 60 | ms | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | 2 |
| Oscillation stabilization time | $t_{RC}$ | X1, X2 | — | — | 3 | s | | 3 |
| External clock high width | $t_{CPH}$ | $OSC_1$ | 90 | — | — | ns | | 4 |
| External clock low width | $t_{CPL}$ | $OSC_1$ | 90 | — | — | ns | | 4 |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 20 | ns | | 4 |
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 20 | ns | | 4 |
| $\overline{INT_0}$, $INT_1$, $\overline{EVENT}$ high width | $t_{IH}$ | $\overline{INT_0}$, $INT_1$, $\overline{EVENT}$ | 2 | — | — | $t_{cyc}$/ $t_{subcyc}$ | | 5 |
| $\overline{INT_0}$, $INT_1$, $\overline{EVENT}$ width | $t_{IL}$ | $\overline{INT_0}$, $INT_1$, $\overline{EVENT}$ | 2 | — | — | $t_{cyc}$/ $t_{subcyc}$ | | 5 |

Notes on next page.

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## AC Characteristics
(**HD404328:** $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
**HD404328U:** $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;
**HD4074329, HD4074329U:** $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified) (cont)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Conditions | Note |
|------|--------|--------|-----|-----|-----|------|-----------------|------|
| RESET high width | $t_{RSTH}$ | RESET | 2 | — | — | $f_{cyc}$ | | 6 |
| RESET fall time | $t_{RSTf}$ | RESET | — | — | 20 | ms | | 6 |
| Input capacitance | $C_{in}$ | All pins except $D_{10}$, $AN_0$–$AN_3$ | — | — | 30 | pF | f = 1 MHz, $V_{in}$ = 0.0 V | |
| | | $D_{10}$ | — | — | 30 | pF | HD404328, HD404328U: f = 1 MHz, $V_{in}$ = 0.0 V | |
| | | | — | — | 180 | pF | HD4074329, HD4074329U: f = 1 MHz, $V_{in}$ = 0.0 V | |

Notes: 1. If $f_{OSC}$ = 0.4 MHz to 1.0 MHz, bit 3 of the miscellaneous register (MIS: $00C) must be set to 1; if $f_{OSC}$ = 1.6 MHz to 4.5 MHz, bit 3 must be set to 0. Do not use $f_{OSC}$ = 1.0 MHz to1.6 MHz with 32-kHz oscillation.
2. The oscillation stabilization time is the time required for the oscillator to stabilize after $V_{CC}$ reaches 2.7 V (2.9 V for the HD4074329 and HD4074329U, or 3.5 V if $V_{CC}$ = 3.5 V to 5.5 V) at power-on or after RESET input goes high after stop mode is canceled. At power-on and when stop mode is cancelled, RESET must be input for at least $t_{RC}$ to ensure the oscillation stabilization time. If using a crystal oscillator or a ceramic oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
3. The oscillation stabilization time is the time required for the oscillator to stabilize after $V_{CC}$ reaches 2.7 V (2.9 V for the HD4074329 and HD4074329U) at power-on—at least $t_{RC}$ must be ensured. If using a 32.768-kHz crystal oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitances.
4. Refer to figure 49.
5. Refer to figure 50. The $t_{cyc}$ unit applies when the MCU is in standby or active mode. The $t_{subcyc}$ unit applies when the MCU is in watch or subactive mode. $t_{subcyc}$ = 244.14 μs (32.768-kHz crystal)
6. Refer to figure 51.

**Serial Interface Timing Characteristics**
(HD404328: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
HD404328U: $V_{CC}$ = 2.7 V to 6.0 V, GND = 0.0 V, $T_a$ = –40°C to +85°C;
HD4074329, HD4074329U: $V_{CC}$ = 2.9 V to 5.5 V, GND = 0.0 V, $T_a$ = –20°C to +75°C;
unless otherwise specified)

**During Transmit Clock Output**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1.0 | — | — | $t_{cyc}$, $t_{subcyc}$ | Load shown in figure 53 | 1, 2 |
| Transmit clock high width | $t_{SCKH}$ | $\overline{SCK}$ | 0.3 | — | — | $t_{Scyc}$ | Load shown in figure 53 | 1 |
| Transmit clock low width | $t_{SCKL}$ | $\overline{SCK}$ | 0.3 | — | — | $t_{Scyc}$ | Load shown in figure 53 | 1 |
| Transmit clock rise time | $t_{SCKr}$ | $\overline{SCK}$ | — | — | 100 | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V, load shown in figure 53 | 1 |
| | | | — | — | 100 | ns | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 53 | 1 |
| | | | — | — | 200 | ns | Load shown in figure 53 | 1 |
| Transmit clock fall time | $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V, load shown in figure 53 | 1 |
| | | | — | — | 100 | ns | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 53 | 1 |
| | | | — | — | 200 | ns | Load shown in figure 53 | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 300 | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V, load shown in figure 53 | 1 |
| | | | — | — | 300 | ns | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 53 | 1 |
| | | | — | — | 500 | ns | Load shown in figure 53 | 1 |

Notes: 1. Refer to figure 52.
2. The $t_{subcyc}$ unit applies when subactive mode is operating.

**During Transmit Clock Output (cont)**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Conditions | Note |
|------|--------|-----|-----|-----|-----|------|-----------------|------|
| Serial input data setup time | $t_{SSI}$ | SI | 200 | — | — | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | * |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | * |
| | | | 300 | — | — | ns | | * |
| Serial input data hold time | $t_{HSI}$ | SI | 150 | — | — | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | * |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | * |
| | | | 300 | — | — | ns | | * |

Note: * Refer to figure 52.

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**During Transmit Clock Input**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1.0 | — | — | $t_{cyc}$, $t_{subcyc}$ | | 1, 2 |
| Transmit clock high width | $t_{SCKH}$ | $\overline{SCK}$ | 0.3 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock low width | $t_{SCKL}$ | $\overline{SCK}$ | 0.3 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock rise time | $t_{SCKr}$ | $\overline{SCK}$ | — | — | 100 | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | 1 |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | — | — | 200 | ns | | 1 |
| Transmit clock fall time | $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | 1 |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | — | — | 200 | ns | | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 300 | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V, load shown in figure 53 | 1 |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 53 | 1 |
| | | | — | — | 500 | ns | Load shown in figure 53 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 200 | — | — | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | 1 |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | 300 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 150 | — | — | ns | HD404328, HD404328U: $V_{CC}$ = 3.5 V to 6.0 V | 1 |
| | | | | | | | HD4074329, HD4074329U: $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | 300 | — | — | ns | | 1 |

Notes: 1. Refer to figure 52.
2. The $t_{subcyc}$ unit applies when subactive mode is operating.

$V_{CC}$ = 3.5 V to 6.0 V (HD404328, HD404328U)
$V_{CC}$ = 3.5 V to 5.5 V (HD4074329, HD4074329U)

$V_{CC}$ = 2.7 V to 3.5 V (HD404328, HD404328U)
$V_{CC}$ = 2.9 V to 3.5 V (HD4074329, HD4074329U)
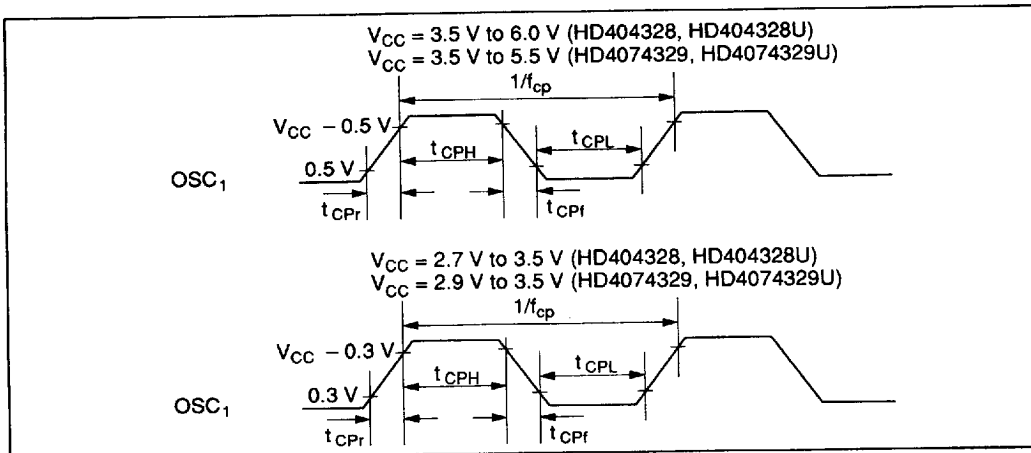
**Figure 49  Oscillator Timing**



$V_{CC}$ = 3.5 V to 6.0 V (HD404328, HD404328U)
$V_{CC}$ = 3.5 V to 5.5 V (HD4074329, HD4074329U)

$V_{CC}$ = 2.7 V to 3.5 V (HD404328, HD404328U)
$V_{CC}$ = 2.9 V to 3.5 V (HD4074329, HD4074329U)
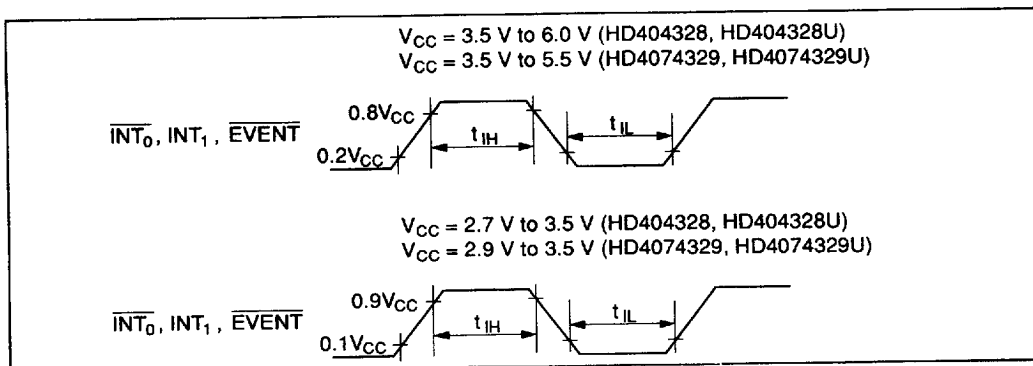
**Figure 50  Interrupt Timing**



$V_{CC}$ = 3.5 V to 6.0 V (HD404328, HD404328U)
$V_{CC}$ = 3.5 V to 5.5 V (HD4074329, HD4074329U)

$V_{CC}$ = 2.7 V to 3.5 V (HD404328, HD404328U)
$V_{CC}$ = 2.9 V to 3.5 V (HD4074329, HD4074329U)

**Figure 51  Reset Timing**

$V_{CC} = 3.5$ V to 6.0 V (HD404328, HD404328U)
$V_{CC} = 3.5$ V to 5.5 V (HD4074329, HD4074329U)

Note: * $V_{CC} - 2.0$ V and 0.8 V are the threshold voltages for transmit clock output,
$0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input, and
$t_{DSO}$, $t_{SSI}$, and $t_{HSI}$ are the timings used with transmit clock input voltages.

$V_{CC} = 2.7$ V to 3.5 V (HD404328, HD404328U)
$V_{CC} = 2.9$ V to 3.5 V (HD4074329, HD4074329U)

Note: * $V_{CC} - 0.5$ V and 0.4 V are the threshold voltages for transmit clock output,
$0.9V_{CC}$ and $0.1V_{CC}$ are the threshold voltages for transmit clock input, and
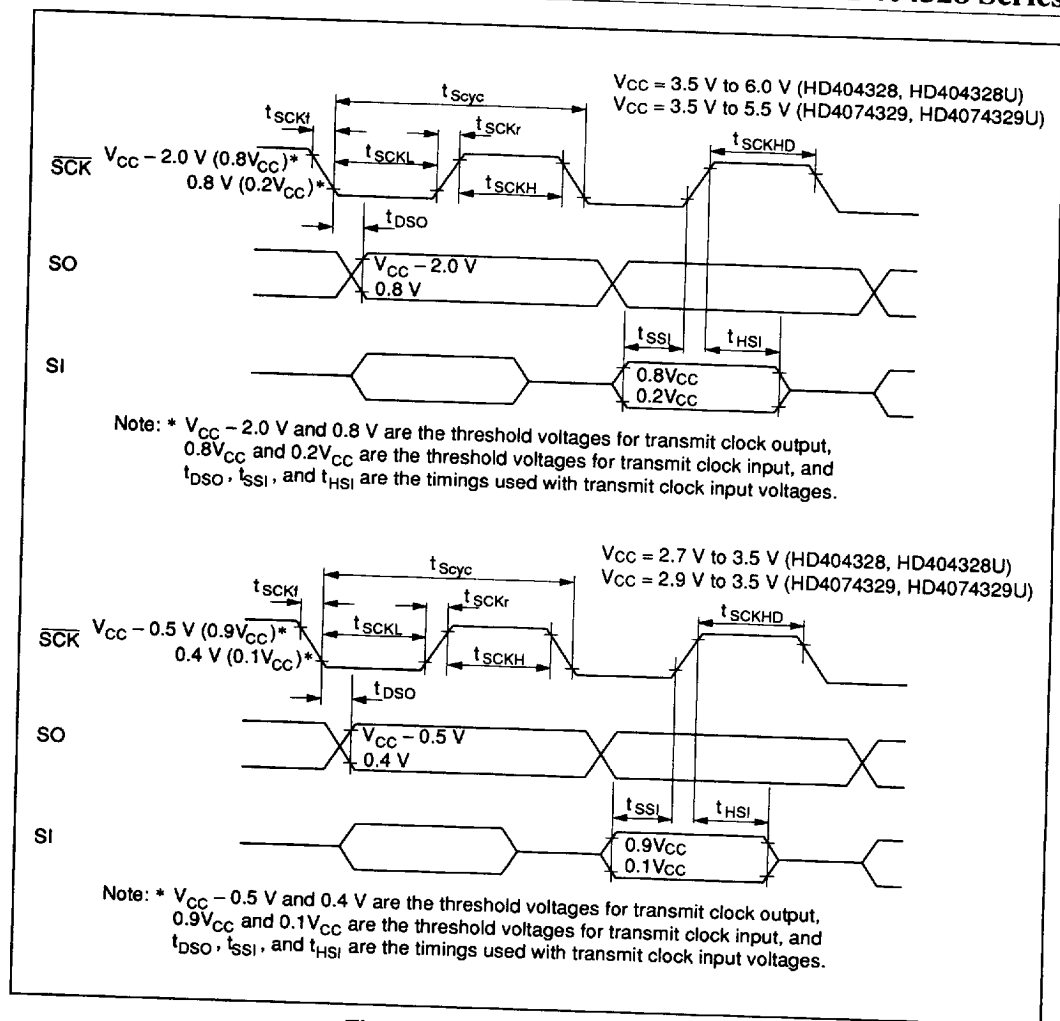$t_{DSO}$, $t_{SSI}$, and $t_{HSI}$ are the timings used with transmit clock input voltages.
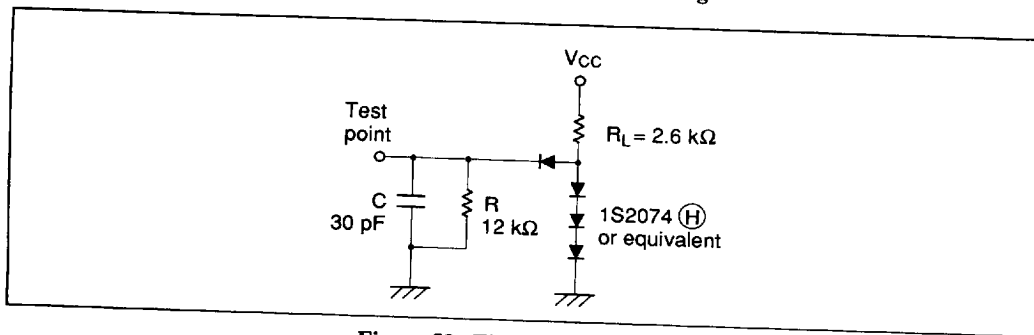
**Figure 52  Serial Interface Timing**



**Figure 53  Timing Load Circuit**

## HD404328/HD404328U Option List

Please check off the appropriate applications and enter
the necessary information.

| Date of order | / / |
|---|---|
| Customer | |
| Department | |
| ROM code name | |
| LSI number (to be filled in by Hitachi) | |

| |
|---|
| ☐ With external LCD voltage division resistors: HD404328 |
| ☐ Without external LCD voltage divison resistors: HD404328U |

### 1. Optional Function (1)

| |
|---|
| *☐ With 32-kHz CPU operation |
| *☐ Without 32-kHz CPU operation, with time-base for clock |
| ☐ Without 32-kHz CPU operation, without time-base |

Note: * Options marked with an asterisk require a subsystem
crystal oscillator (X1, X2).

### 2. Optional Function (2)

| |
|---|
| ☐ With zero-crossing detection function |
| ☐ Without zero-crossing detection function |

### 3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using
the EPROM on-package microcomputer type (including ZTAT™ version).

| |
|---|
| ☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...). |
| ☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS. |

### 4. System Oscillator for OSC1 and OSC2

| | | |
|---|---|---|
| ☐ Ceramic oscillator | f = | MHz |
| ☐ Crystal oscillator | f = | MHz |
| ☐ External clock | f = | MHz |

### 5. Stop Mode

| |
|---|
| ☐ Used |
| ☐ Not used |

### 6. Packages

| |
|---|
| ☐ DP-64S |
| ☐ FP-64A |
| ☐ FP-64B |

■ 4496204 0047699 237 ■