HD404608/HD4074608

Description

The MCU is a microcomputer unit which has powerful and efficient architecture of the HMCS400 family. The MCU incorporates a high-precision dual tone multi-frequency (DTMF) circuit, LCD driver/controller, voltage comparator, and 32kHz watch oscillator circuit.
The HD4074608, incorporating PROM, is a ZTAT microcomputer which can dramatically shorten system development period and smoothly proceed from debugging to mass production.

Features

- 8192 words of 10-bit ROM
- 1184 digits of 4-bit RAM
- 30 I/O pins:
  Including 10 high current output pins.
  I/O pin circuit configuration is CMOS
  Input/Output pull-up MOS can be selected by software
- On-chip DTMF generator
- 16-digit LCD driver
- Three timers/counters
- Clock synchronous 8-bit serial interface
- Six interrupt sources
  —External: 2
  —Internal: 4
- Subroutine stack
  —Up to 16 levels including interrupts
- Instruction cycle time
  —10 μs (fosc = 400kHz)
  —5 μs (fosc = 800kHz)
- Four low power dissipation modes
  —Stop mode
  —Standby mode
  —Watch mode
  —Subactive mode (Option)
- Internal oscillator:
  Crytal or ceramic filter
  (external clock is available)
- Voltage comparator (2 channels)
- Operation modes:
  MCU mode
  PROM mode (HD4074608)
- Package
  —80-pin plastic flat package (FP-80B)
  (FP-80A)

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Type of Products

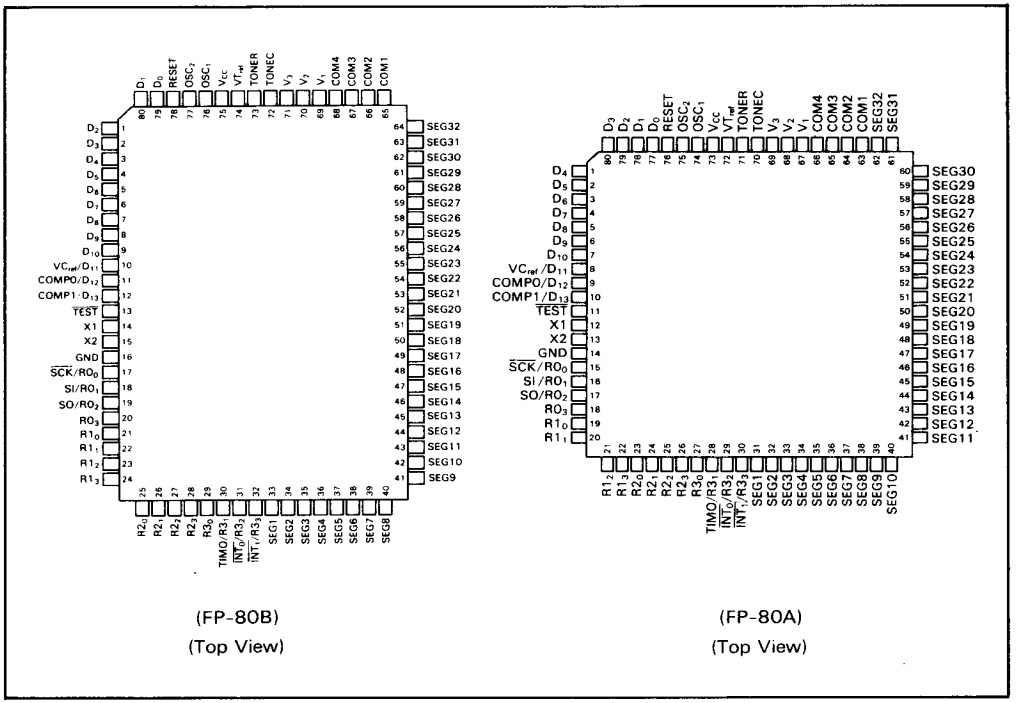
Mask ROM type

Part No.	Clock Freq. (kHz)	Package
HD404608FS	400/800	FP-80B
HD404608H		FP-80A

ZTAT type

Part No.	Clock Freq. (kHz)	Package
HD4074608FS	400/800	FP-80B
HD4074608H		FP-80A

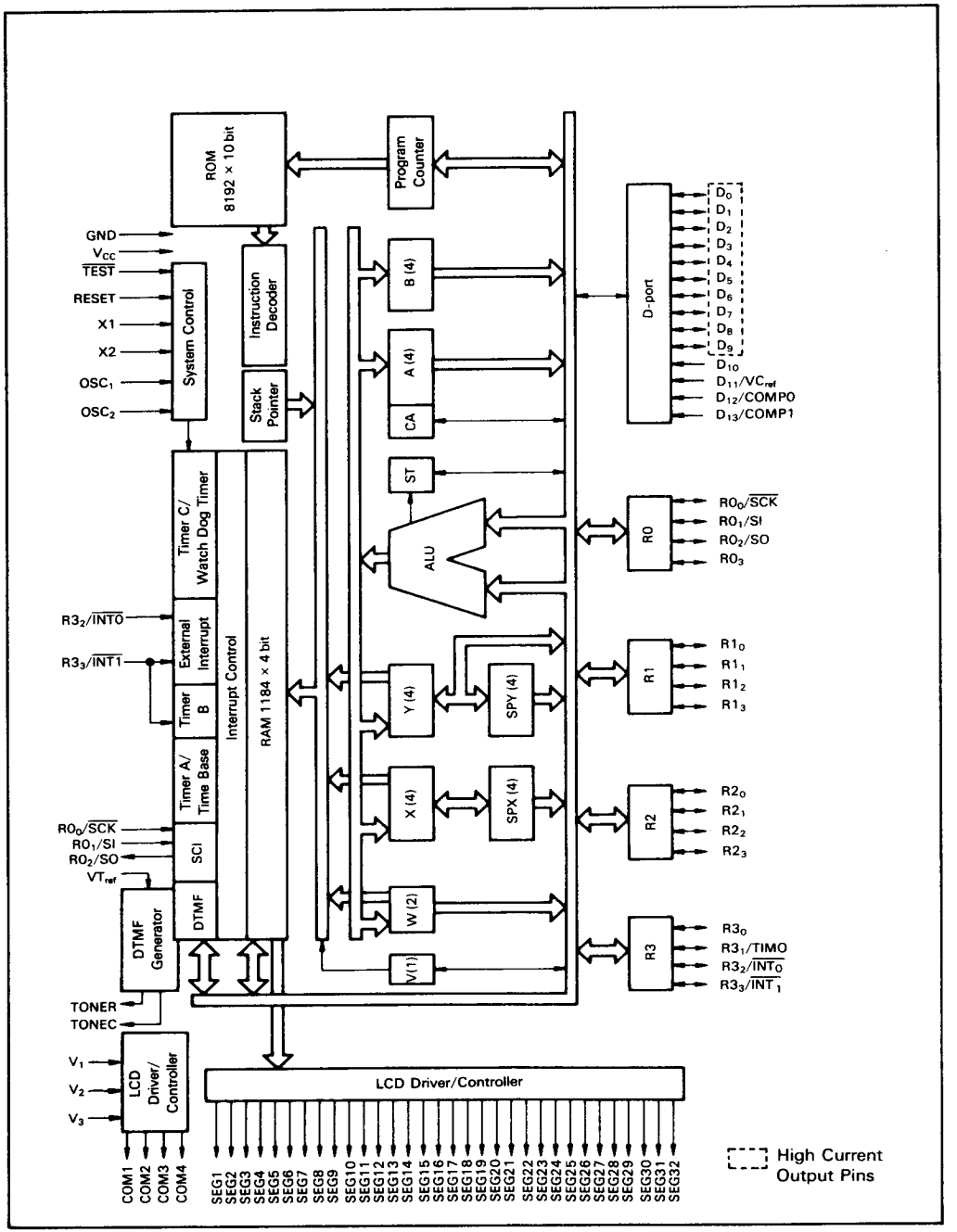
Pin Arrangement



(FP-80B)
(Top View)

(FP-80A)
(Top View)

Block Diagram



Pin Function

Pin No. FP-80B	FP-80A	Pin Name	I/O	Pin No. FP-80B	FP-80A	Pin Name	I/O
1	79	D_2	I/O	41	39	SEG9	O
2	80	D_3	I/O	42	40	SEG10	O
3	1	D_4	I/O	43	41	SEG11	O
4	2	D_5	I/O	44	42	SEG12	O
5	3	D_6	I/O	45	43	SEG13	O
6	4	D_7	I/O	46	44	SEG14	O
7	5	D_8	I/O	47	45	SEG15	O
8	6	D_9	I/O	48	46	SEG16	O
9	7	D_{10}	I	49	47	SEG17	O
10	8	D_{11}/VC_{ref}	I	50	48	SEG18	O
11	9	D_{12}/COMP0	I	51	49	SEG19	O
12	10	D_{13}/COMP1	I	52	50	SEG20	O
13	11	$\overline{TEST}$	I	53	51	SEG21	O
14	12	X1	I	54	52	SEG22	O
15	13	X2	O	55	53	SEG23	O
16	14	GND		56	54	SEG24	O
17	15	$RO_0/\overline{SCK}$	I/O	57	55	SEG25	O
18	16	RO_1/SI	I/O	58	56	SEG26	O
19	17	RO_2/SO	I/O	59	57	SEG27	O
20	18	RO_3	I/O	60	58	SEG28	O
21	19	$R1_0$	I/O	61	59	SEG29	O
22	20	$R1_1$	I/O	62	60	SEG30	O
23	21	$R1_2$	I/O	63	61	SEG31	O
24	22	$R1_3$	I/O	64	62	SEG32	O
25	23	$R2_0$	I/O	65	63	COM1	O
26	24	$R2_1$	I/O	66	64	COM2	O
27	25	$R2_2$	I/O	67	65	COM3	O
28	26	$R2_3$	I/O	68	66	COM4	O
29	27	$R3_0$	I/O	69	67	V_1	
30	28	$R3_1$/TIMO	I/O	70	68	V_2	
31	29	$R3_2/\overline{INT_0}$	I/O	71	69	V_3	
32	30	$R3_3/\overline{INT_1}$	I/O	72	70	TONEC	O
33	31	SEG1	O	73	71	TONER	O
34	32	SEG2	O	74	72	VT_{ref}	
35	33	SEG3	O	75	73	V_{CC}	
36	34	SEG4	O	76	74	OSC_1	I
37	35	SEG5	O	77	75	OSC_2	O
38	36	SEG6	O	78	76	RESET	I
39	37	SEG7	O	79	77	D_0	I/O
40	38	SEG8	O	80	78	D_1	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin

Pin Description

GND, V_{CC} (Power)

These are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to V_{CC}.

$\overline{TEST}$

$\overline{TEST}$ is for test purposes only. Connect it to V_{CC}.

RESET

RESET resets the MCU. Refer to Reset section for details.

OSC_1, OSC_2 (Oscillator Connections)

OSC_1 and OSC_2 are the oscillator terminals of the system. They can be connected to a ceramic filter resonator or external oscillator circuits.

X1, X2

These are watch oscillator on which 32.768 kHz crystal is used.

Port D (D_0-D_{13})

Port D is a 1-bit I/O port. D_0-D_9 are I/O ports and D_{10}-D_{13} are input ports. D_0-D_9 are high current output ports (15 mA max). D_{11}-D_{13} are also available as voltage comparators. Refer to Input/Output for details.

Port R (R0-R3)

Port R is a 4-bit I/O port. R0-R3 are I/O ports. And $R0_0$, $R0_1$, $R0_2$, $R3_1$, $R3_2$, and $R3_3$ are multiplexed with $\overline{SCK}$, SI, SO, TIMO, $\overline{INT_0}$, $\overline{INT_1}$, respectively.

$\overline{INT_0}$, $\overline{INT_1}$ (Interrupts)

$\overline{INT_0}$ and $\overline{INT_1}$ are external interrupts for the MCU. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$ respectively. For details, see Interrupt section.

$\overline{SCK}$, SI, SO

The transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. $\overline{SCK}$, SI, and SO are multiplexed with $R0_0$, $R0_1$, and $R0_2$, respectively. For details, see Serial Interface section.

TIMO

TIMO is a duty variable square waveform output pin. See Timer C section for details.

V_1, V_2, V_3

These are power supply pins for LCD driver. Internal resistors provide voltage level for each pin. The voltage condition is; $V_{CC} \geqq V_1 \geqq V_2 \geqq V_3 \geqq GND$. See section Liquid Crystal Display for details.

COM1 to COM4

These are common signal output pins for LCD display. See Liquid Crystal Display section for details.

SEG1 to SEG32

These are segment signals output pins for LCD display. See Liquid Crystal Display section for details.

TONER, TONEC, VT_{ref}

These are DTMF signal output pins. TONER and TONEC transmits signals for ROW and COLUMN, respectively. VT_{ref} is a reference voltage of DTMF signals and apply $V_{CC} \geqq VT_{ref} \geqq GND$ to this. For details, see DTMF Output section.

COMP0, COMP1, VC_{ref}

COMP0, COMP1 are analog inputs for the voltage comparator. VC_{ref} is used as a reference voltage pin to input the threshold voltage of the analog input pin.

Functional Description

ROM Memory Map

The MCU includes 8,192 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area ($0000 to $000F): Locations $0000 through $000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F are reserved for subroutines. Program sequence branches to subroutine by CAL instruction.

Pattern Area ($0000 to $0FFF): Locations $0000 through $0FFF are reserved for ROM data. P instructions allow the MCU to refer to the ROM data as a pattern.

Program Area ($0000 to $1FFF): Locations from $0000 to $1FFF can be used for program code.

RAM Memory Map

The MCU includes 1184 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area ($000 to $003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $01F, $024 to $03F): The special function registers are the mode or data registers for the serial interface, timer/counter, LCD, and DTMF, and the data control registers for the I/O ports. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2.

SEM/REM, SEMD/REMD instructions are available to the LCD control register (LCR).

Other registers cannot be accessed by RAM bit manipulation instructions.

Register Flag Area ($020-$023): Locations $020 through $023 are consisted of LSON, WDON, TGSP flags which are bit registers accessible by RAM bit manipulation instruction. Note that WDON flag can only be set and SEM/SEMD instruction is available to this.

TGSP flag can be set/reset, and SEM/REM and SEMD/REMD instructions are available to this.

LCD Data Area ($050-$06F): Locations $050 to $06F store the LCD data which is automatically transmitted to segment as a display data. LCD is illuminated with 1 and faden with 0. This area can be used as a data area.

Data Area ($040 to $2CF, $100 to $2CF; Bank1): 16 digits of $040 through $04F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4). 464 digits of $100 through $2CF is select the bank of location depending on the value of V register.

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

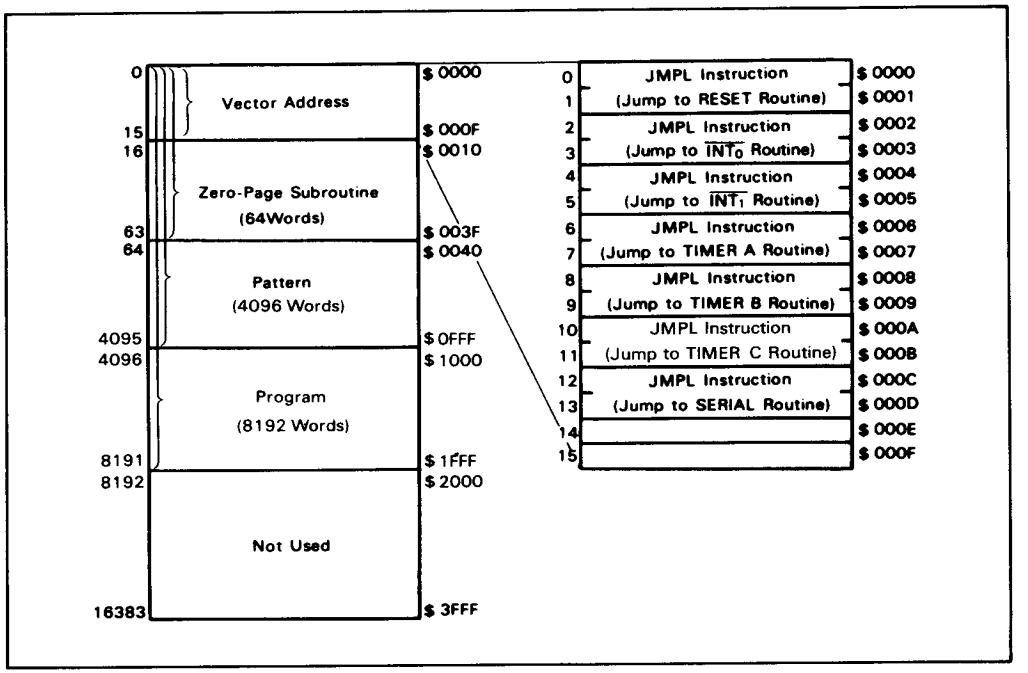


Figure 1. ROM Memory Map

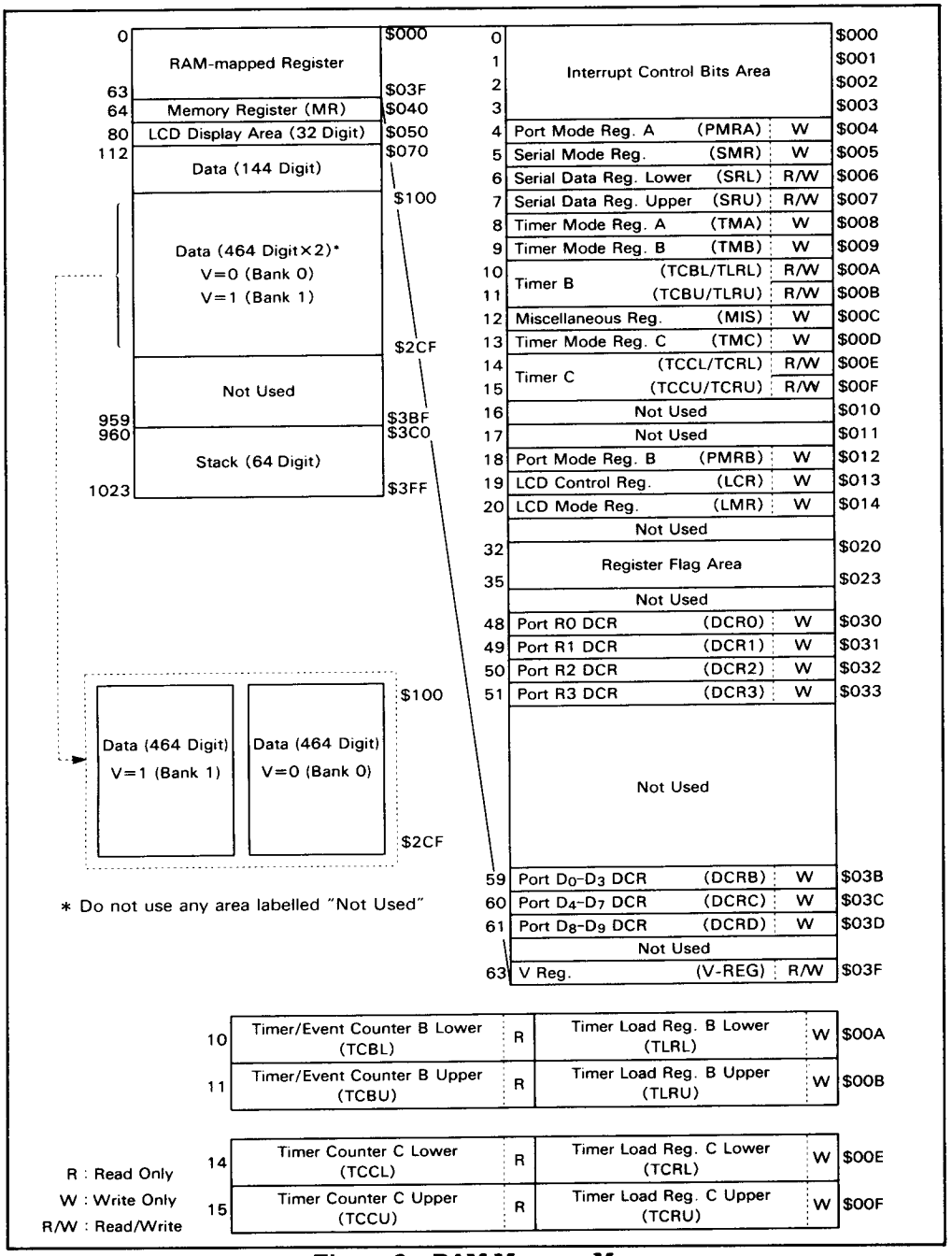


Figure 2. RAM Memory Map

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of TIMER-C)	IFTC (IF of TIMER-C)	IMTB (IM of Timer B)	IFTB (IF of Timer B)	$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

IF: Interrupt Request Flag
IM: Interrupt Mask
I/E: Interrupt Enable Flag
SP: Stack Pointer
Note: Each bit in the interrupt control bits area or register flag area is set by the SEM/SEMD instruction, is reset by the REM/REMD instruction, and is tested by the TM/TMD instruction. They are not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction.
The content of status becomes invalid when "Not Used" bit and RSP bit are tested by a TM/TMD instruction.

	bit 3	bit 2	bit 1	bit 0	
32	Not Used	TGSP (Tone Generator Speed Flag)	WDON (Watch Dog on Flag)	LSON (Low Speed on Flag)	$020
	Reserved				

SEM/SEMD instruction is available for WDON flag (can be reset only by MCU reset).
SEM/SEMD, REM/REMD instruction is available for TGSP flag.

Figure 3. Configuration of Interrupt Control Bit Area and Register Flag Area

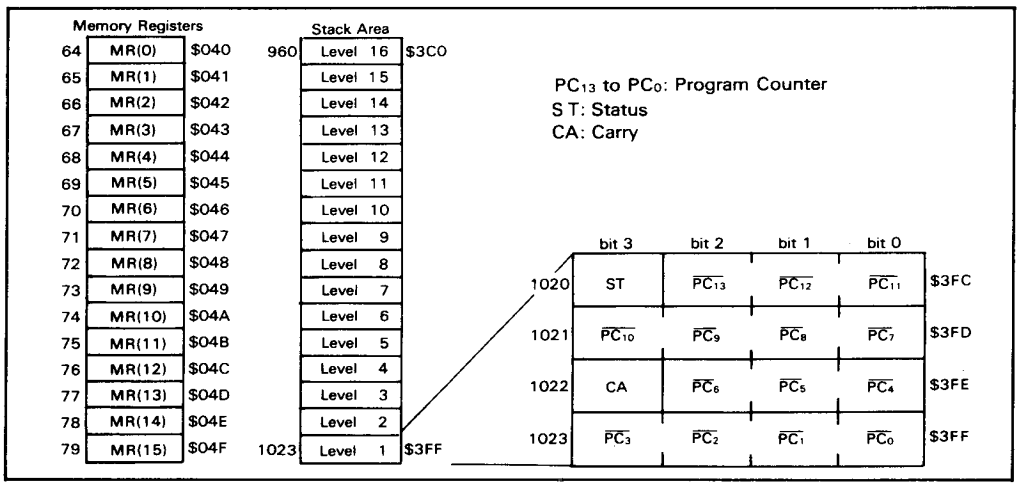


Figure 4. Configuration of Memory Register, Stack Area and Stack Position

Registers and Flags

The MCU provides ten registers and two flags for the CPU operations. They are illustrated in figure 5 and described in the following paragraphs.

Accumulator (A), Register B (B): The accumulator and register B are 4-bit registers which hold the results of the arithmetic logic unit (ALU), and exchange data between memories, I/O pins, and other registers.

Register V (V): Register V, available for RAM address expansion, selects the bank of location $100-$2CF on the RAM address (464 digits) depending on its value. Therefore, when you access location $100-$2CF on the RAM address, specify the value of register V (V = $0; Bank 0, V = $1; Bank 1). You can access location $000-$0FF and $300-$3FF independently of register V's value. Register V locates on $03F of the RAM address area.

Register W (W), Register X (X), Register Y (Y): Register W is a 2-bit, and registers X and Y are 4-bit registers which address RAM indirectly. Register Y is also available for addressing port D.

Register SPX (SPX), Register SPY (SPY): Registers SPX and SPY are 4-bit registers available for assisting registers X and Y, respectively.

Carry (CA): The carry holds the ALU overflow which arithmetic operation generates. It is also affected by SEC, REC, ROTL, and ROTR instructions. During interrupt servicing, the carry is pushed onto the stack and restored back from the stack by RTNI instruction (It is unaffected by RTN instructions).

Status (ST): The status holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. The status is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until an instruction which affects the next status is executed. The status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, the status is pushed onto the stack and restored back from the stack by RTNI instruction, not by RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter for holding ROM address.

Stack Pointer (SP): The stack pointer is a 10-bit register to indicate the next stacking area up to 16 levels. The stack pointer is initialized to $3FF on the RAM address at the MCU reset. It is decremented by 4 as data pushed onto the stack, and incremented by 4 as data restored back from the stack. The stack pointer is initialized to $3FF either by MCU reset or the RSP bit reset by REM/REMD instruction.

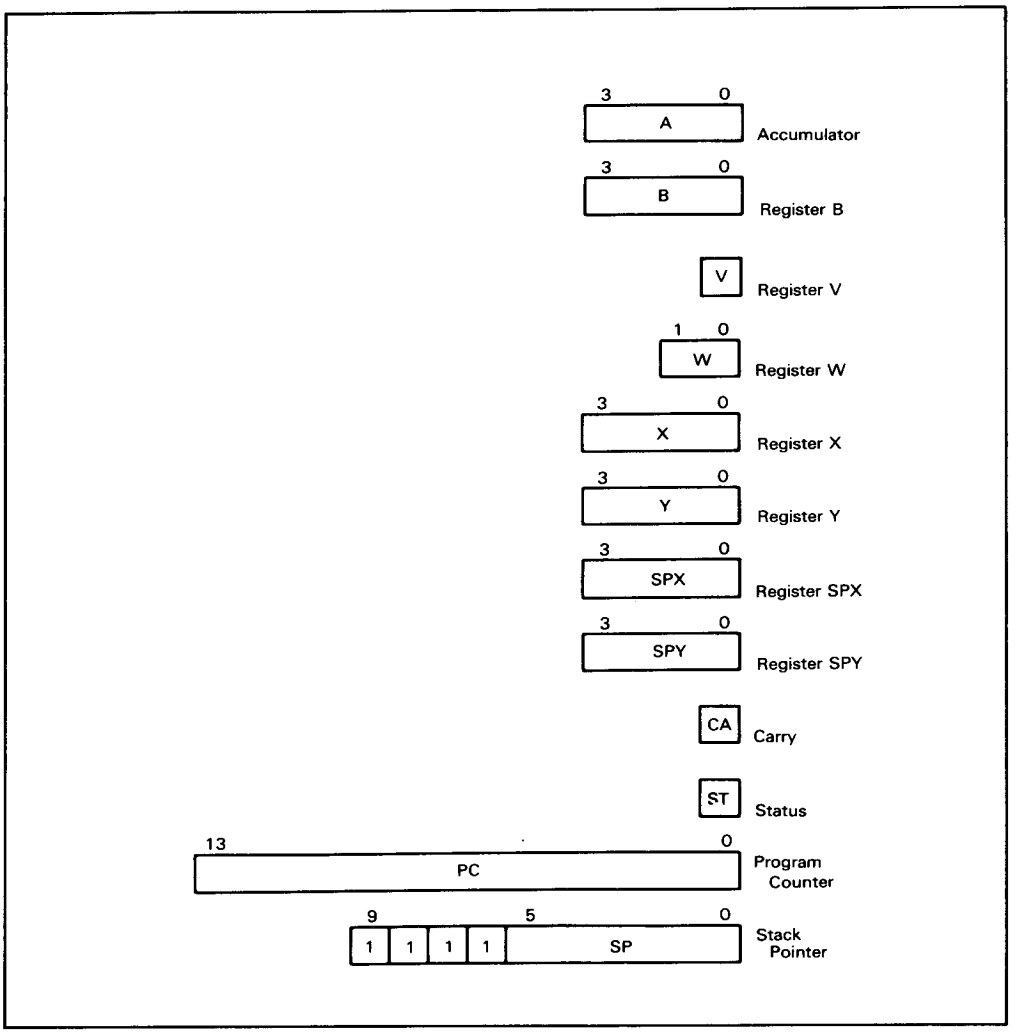


Figure 5. Registers and Flags

Interrupt

Six interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (timers A, B, C), and serial interface (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions (The interrupt request flag (IF) cannot be set by software). The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

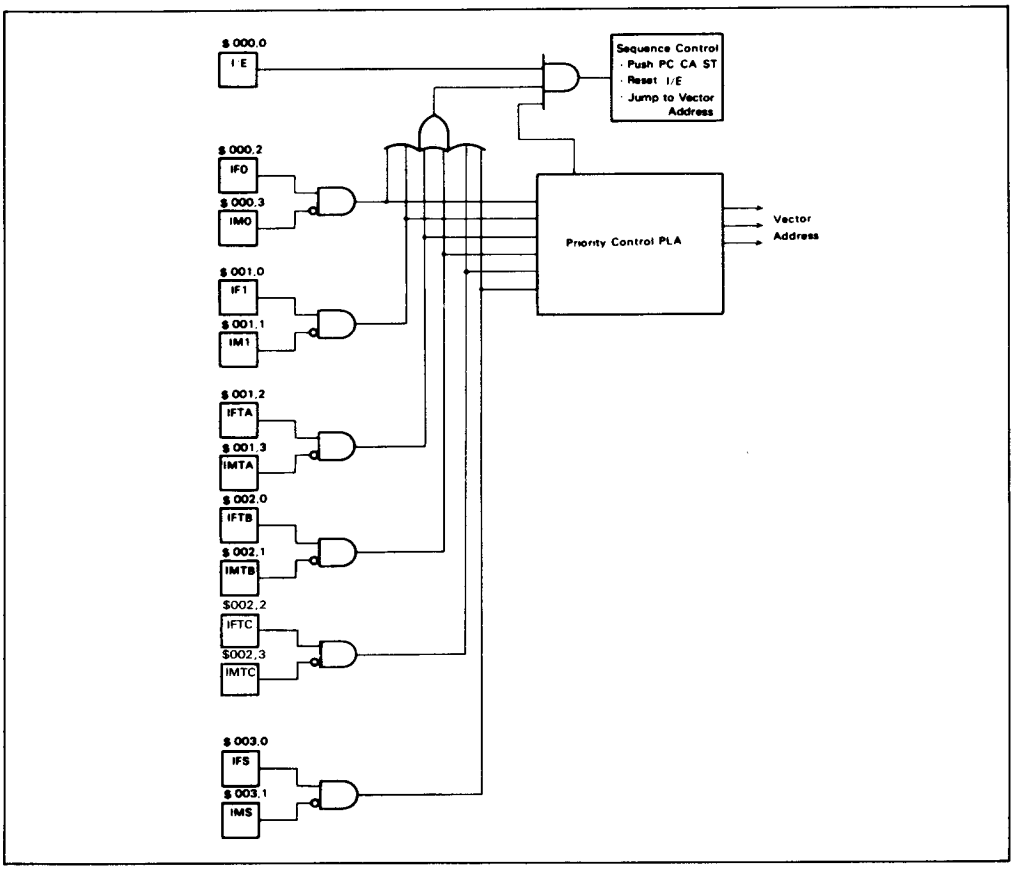


Figure 6. Interrupt Control Circuit Block Diagram

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status, and program counter are pushed onto the stack. In the third cycle, the instruction is executed after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF, which caused the interrupt service, must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: $000 bit 0): The interrupt enable flag enables/disables interrupt requests (table 3). It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMRA: $004).

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs (table 4).

The $\overline{INT_1}$ input can be used as a clock signal input to timer B. Then, timer B counts up at

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
SERIAL	6	$000C

Table 2. Conditions of Interrupt Service

	Interrupt Source					
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**Timer A**	**Timer B**	**Timer C**	**SERIAL**
I/E	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0	0
IFTC · $\overline{IMTC}$	*	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	*	1

* Don't care

each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted (table 5).

To detect the edge of $\overline{INT_0}$ or $\overline{INT_1}$, it must need more than two instruction cycle times level ($2t_{cyc}/2t_{SUBcyc}$).

External Interrupt Request Flags (IF0: $000 bit 2, IF1: $001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$, and $\overline{INT_1}$ inputs, respectively (table 4).

External Interrupt Masks (IM0: $000 bit 3, IM1: $001 bit 1): The external interrupt masks mask the external interrupt requests (table 5).

Timer A Interrupt Request Flag (IFTA: $001 bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 6).

Timer A Interrupt Mask (IMTA: $001 bit 3): Timer A interrupt mask prevents an interrupt request from being generated by timer A interrupt request flag (table 7).

Timer B Interrupt Request Flag (IFTB: $002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: $002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B interrupt request flag (table 9).

Timer C Interrupt Request Flag (IFTC: $002 bit 2): The timer C interrupt request flag is set by the overflow output of timer C (table 10).

Timer C Interrupt Mask (IMTC: $002 bit 3): The timer C interrupt mask prevents the interrupt from being generated by timer C interrupt request flag (table 11).

Serial Interrupt Request Flag (IFS: $003 bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter (table 12).

Serial Interrupt Mask (IMS: $003 bit 1): The serial interrupt mask masks the interrupt request (table 13).

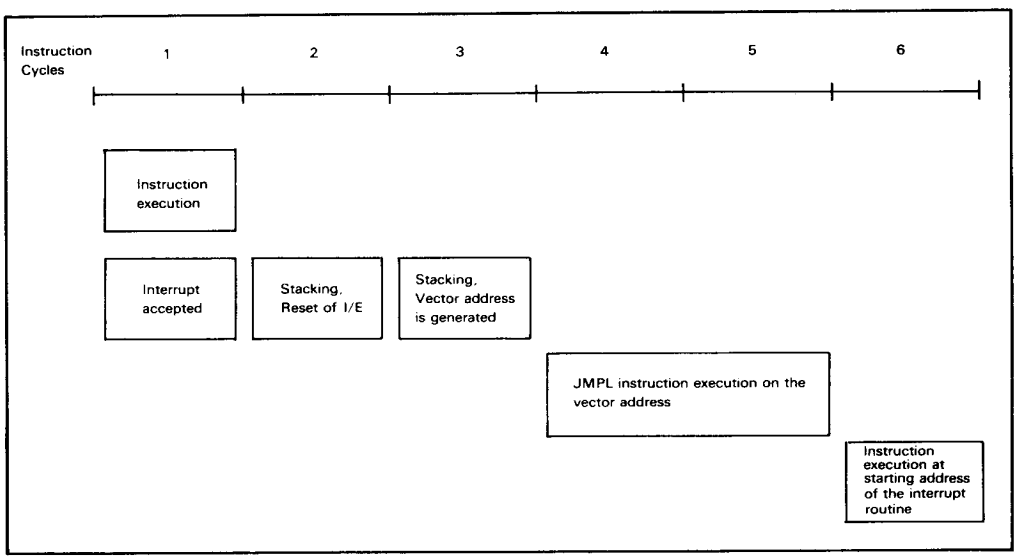


Figure 7. Interrupt Servicing Sequence

Table 3. Interrupt Enable Flag

Interrupt Enable Flag (I/E)	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags (IF0, IF1)	Interrupt Request
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks (IM0, IM1)	Interrupt Request
0	Enable
1	Disable (masks)

Table 6. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag (IFTA)	Interrupt Request
0	No
1	Yes

Table 7. Timer A Interrupt Mask

Timer A Interrupt Mask (IMTA)	Interrupt Request
0	Enable
1	Disable (Mask)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag (IFTB)	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask (IMTB)	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Timer C Interrupt Request Flag

Timer C Interrupt Request Flag (IFTC)	Interrupt Request
0	No
1	Yes

Table 11. Timer C Interrupt Mask

Timer C Interrupt Mask (IMTC)	Interrupt Request
0	Enable
1	Disable (mask)

Table 12. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 13. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

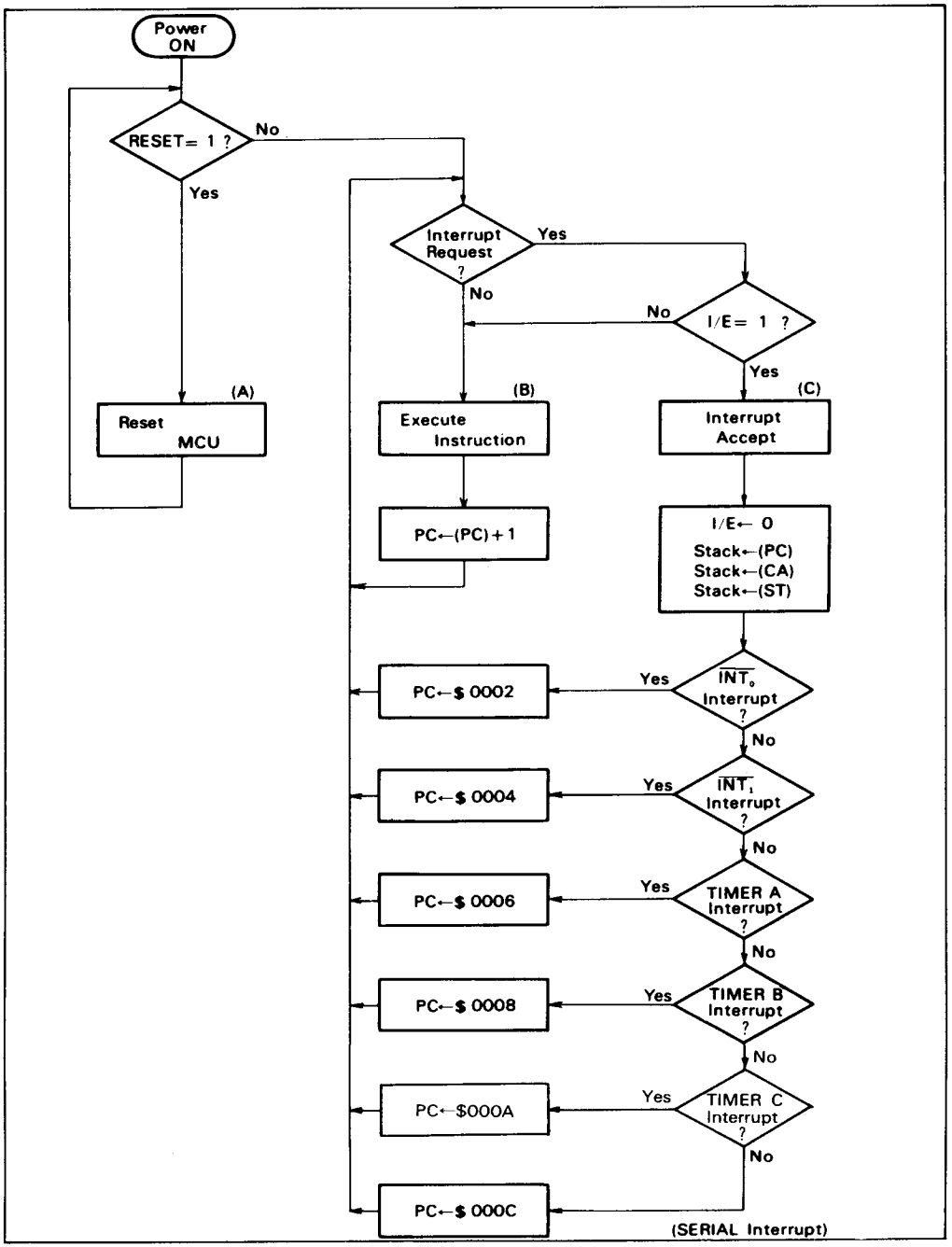


Figure 8. Interrupt Servicing Flowchart

Serial Interface

The serial interface transmits/receive 8-bit data in serial. This consists of the serial data register, the serial mode register, the port mode register A, the octal counter, and the multiplexer (figure 9). Pin $R0_0/\overline{SCK}$ and the transfer clock signal are controlled by the serial mode register. The data of the serial data register can be written in or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

The STS instruction starts serial interface operations and resets the octal counter to $0. The octal counter starts to count at the falling edge of the transfer clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the octal counter is reset to $0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: $005): The 4-bit write-only serial mode register controls the $R0_0/\overline{SCK}$, prescaler divide ratio, and transfer clock source (table 14).

The write signal to the serial mode register controls the internal state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying transfer clock, and it also resets the octal counter to $0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Data of the serial mode register will be changed from the second instruction of writing into the serial mode register. Therefore, it is required to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data regis-

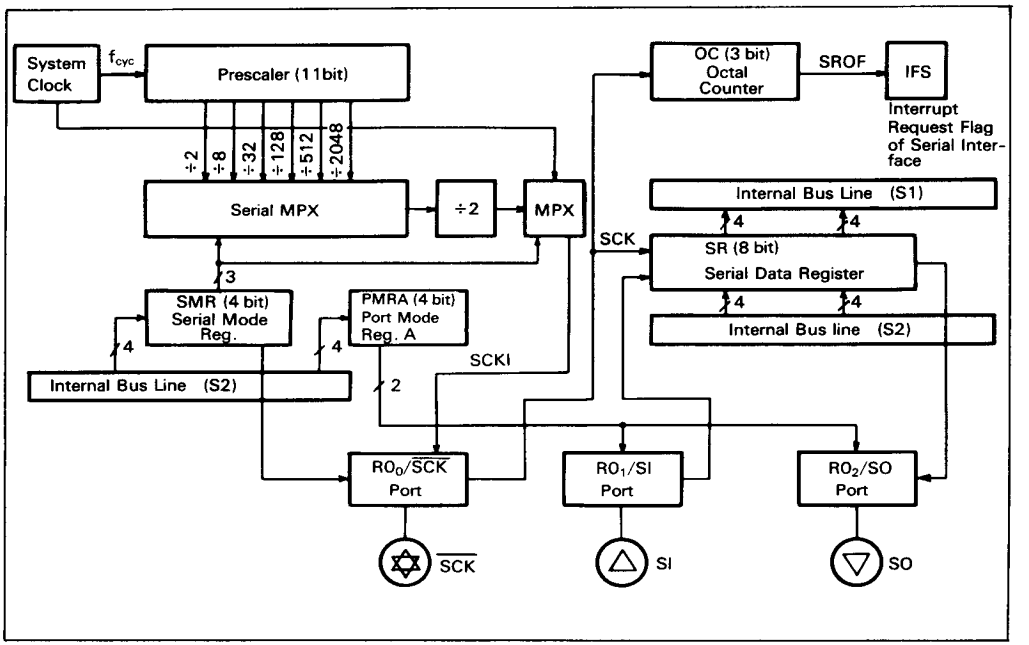


Figure 9. Serial Interface Block Diagram

ter consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register will be output from the SO pin of LSB synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the SI pin to the serial data register synchronously with the rising edge of the transfer clock. Figure 11 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Selection and Change of the Operation Mode: Table 15 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register.

Initialize the serial interface by the write signal to the serial mode register in order to change the operation mode of the serial interface.

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, SCK waiting state, and transfer state (figure 12).

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer

Table 14. Serial Mode Register

SMR3	$R0_0/\overline{SCK}$
0	Used as $R0_0$ port input/output pin
1	Used as $\overline{SCK}$ input/output pin

				Transfer Clock		
SMR2	SMR1	SMR0	$R0_0/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ Output	System Clock		÷ 1
1	1	1	$\overline{SCK}$ Input	External Clock		

clock is applied. If an STS instruction is executed then, the serial interface shifts to SCK waiting state.

In this state, the falling edge of the first transfer clock causes the serial interface shift to transfer state, while the octal counter counts-up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously.
The octal counter becomes 000 again by 8 external transfer clocks or by execution of STS instruction, so that the serial interface returns to SCK waiting state, and the serial

Table 15. Serial Interface Operation Mode

SMR3	PMRA1	PMRA0	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

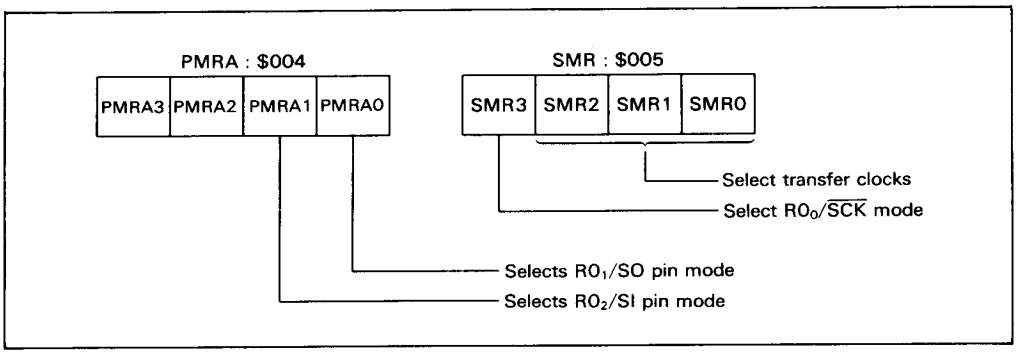


Figure 10. Configurations and the Functions of the Mode Registers

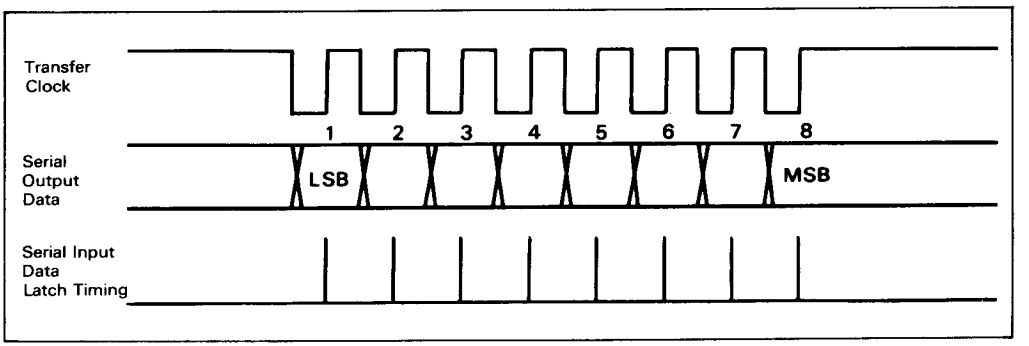


Figure 11. Serial Interface I/O Timing Chart

interrupt request flag is set simultaneously. In transfer state the octal counter becomes 000 by 8 internal transfer clocks, so that the serial interface enters to STS instruction waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output is triggered by the execution of an STS instruction, and stops after 8 clocks.

Program the SMR again to initialize the

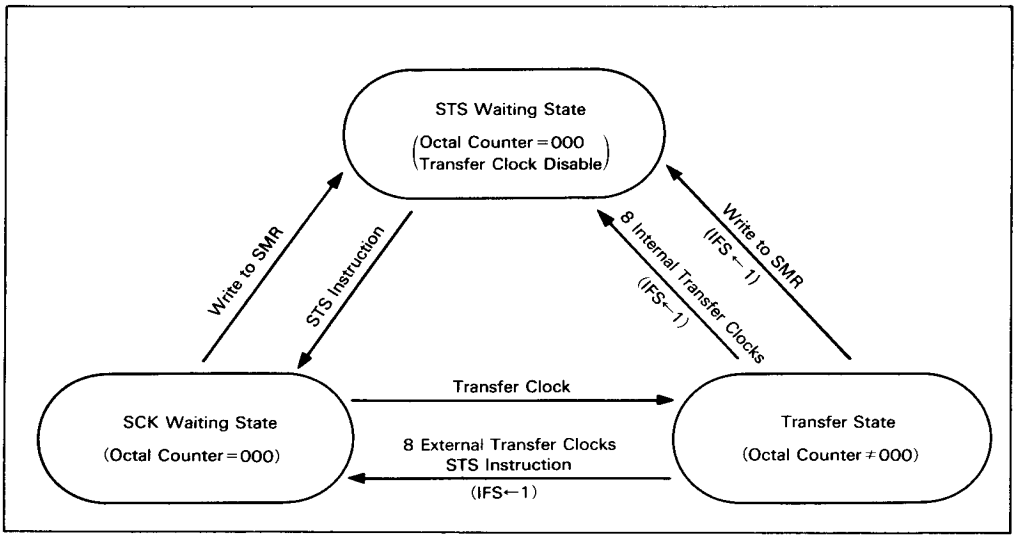


Figure 12. Serial Interface Operation State

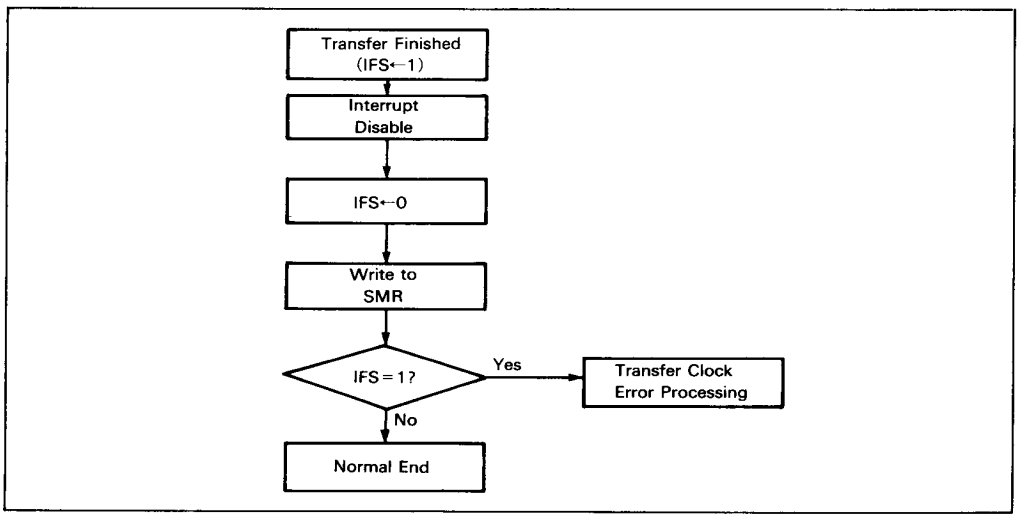


Figure 13. Example of Transfer Clock Error Detection

internal state of the serial interface when the PMRA is programmed in the transfer state or in the SCK waiting state. Then the serial interface goes into the STS waiting state.

Example of Transfer Clock Error Detection: The serial interface malfunctions when the transfer clock is disturbed by external noises. In this case, transfer clock error can be detected by the procedure shown in figure 13.

If more than 8 transfer clocks are applied in the SCK waiting state, the state of the serial interface shifts in the following sequence: first, transfer state, second, SCK waiting state, and third, transfer state again. The serial interrupt request flag should be reset before entering into the STS waiting state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

Timer

The MCU provides prescalers S and B (Each prescaler has the different input clock source individually), and 3 timers/counters (timers A, B, and C). Figures 14, 15 shows their diagrams.

Prescaler S: The input to the prescaler S is a system clock signal. The prescaler is initialized to $000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except by MCU reset and in the stop and watch modes. The prescaler provides input clock signals of timer A-C and the transfer clock of the serial interface. They can be selected by the timer mode registers A (TMA), B (TMB), C (TMC), and the serial mode register (SMR), respectively.

Prescaler W: The input to the prescaler W is a clock which devides X1 input clock into 8. The output of the prescaler W is available as an input clock for timer A by controlling the timer mode register (TMA).

Timer A Operation: After timer A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A is counted up to $FF, timer A is set to $00 again, and generating overflow output. This leads to setting timer A interruput request flag (IFTA: $001, bit 2) to 1. Therefore, timer A can function as an interval timer periodically generating overflow output at every 256th clock signal input.

To use timer A as a watch time base, set TMA3 to 1. The timer counter receives pres-

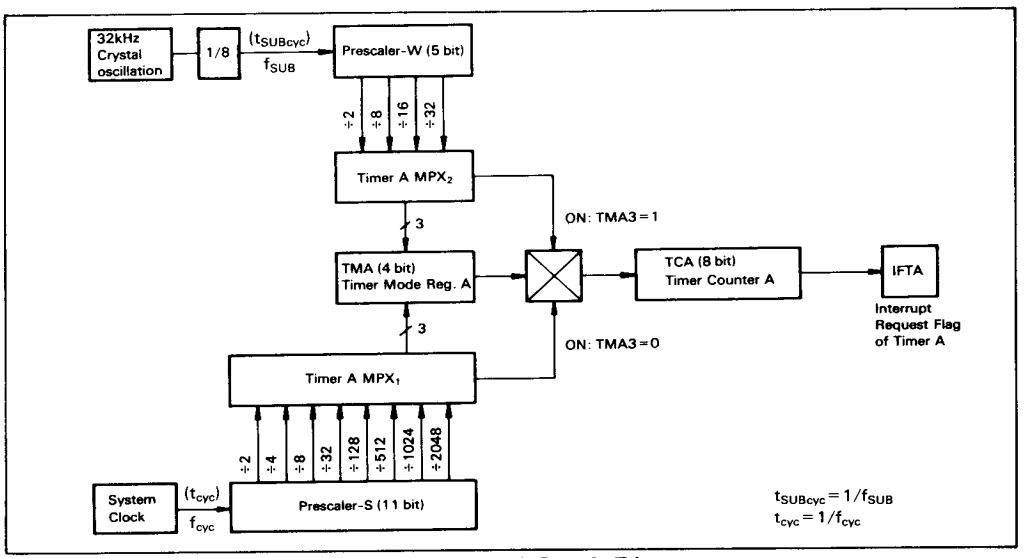


Figure 14. Timer A Block Diagram

caler W output, and timer A generates interrupts with an accurate timing (reference clock = 32kHz crystal oscillation). When you use timer A as a watch time base, prescaler W and timer counter can be initialized to $0 by setting timer mode register A.

The clock input signals to timer A are selected by the timer mode register A (TMA: $008).

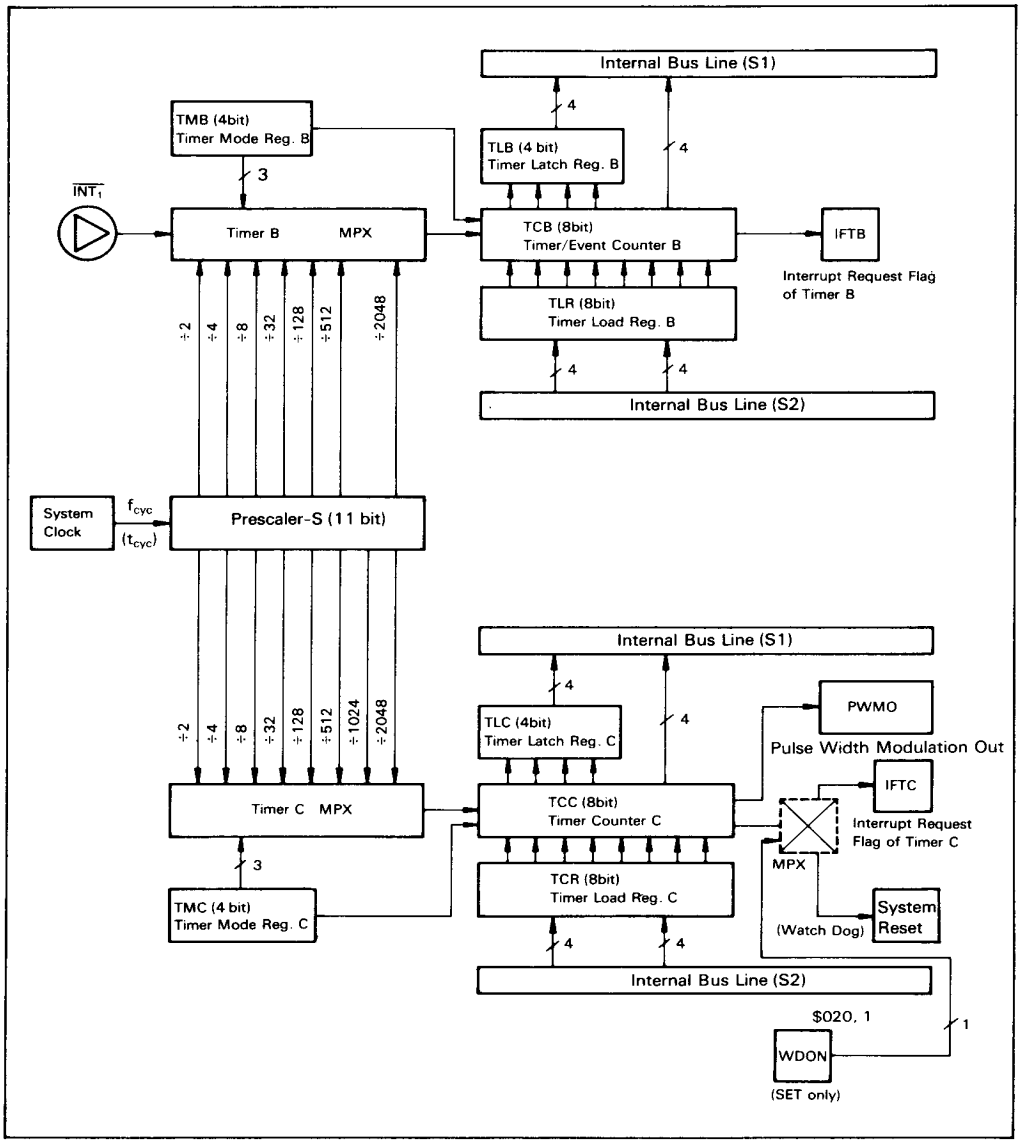


Figure 15. Timer B/Timer C Block Diagram

Timer B Operation: The timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT}_1$ as $\overline{INT}_1$ by the port mode register (PMR: $004) control to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002 bit 0) will be set at this overflow output.

Timer C Operation: The timer mode register C (TMC: $00D) selects the auto-reload function, and the prescaler divide ratio for timer C.

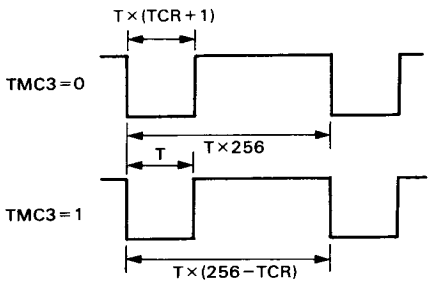
Timer C is initialized according to the data written into the timer load register by software. Timer C counts up at every clock input signal. When the next clock signal is applied to timer C after it is set to $FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer C is initialized according to the value of the timer load register. If it is not selected, timer C goes to $00. The timer C interrupt request flag (IFTC: $002 bit 2) will be set at this overflow output.

Timer C is also available as a watch dog timer for detecting a program out of sequence. An MCU reset occurs when the watch dog on flag (WDON) is 1 and the counter overflow output is generated by the program out of sequence. During timer C is stopped, the watchdog timer function is also stopped. In the standby mode, the function is enabled.

Timer C provides the duty variable pulse output function (PWMO). The output waveform differs depending on the contents of the timer mode register and the timer load register C (figure 16). When you select pulse output function, set $R3_1$/TIMO to TIMO by controlling the port mode register B.
During timer C is stopped, this function is also stopped.

Timer Mode Register A (TMA: $008): The timer mode register A is a 4-bit write only register which controls the timer A operation as table 16 shows. The timer mode register A is initialized to $0 at MCU reset.

Timer Mode Register B (TMB: $009): The timer mode register B (TMB) is a 4-bit write-



T: Input clock Period to couunter (Table 18)
TCR: The value of the timer load register

Note: Always fixed to low when TCR=$FF.

Figure 16. Variable Duty-Cycle Pulse Output Waveform

only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 17. The timer mode register B is initialized to $0 by MCU reset.

The data of timer B changes from the second instruction cycle of the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed.

Timer Mode Register C (TMC: $00D): The timer mode register C is a 4-bit write only register which selects the auto-reload function and prescaler divide ratio as table 18 shows. The timer mode register C is initialized to $0 at MCU reset.

The contents of the timer mode register C can be changed from the second instruction cycle of writing into this. Therefore, it is required to initialize the timer C after the contents of the timer mode register C has been changed completely.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has low-order digits (TCBL: $00A, TLRL: $00A) and high-order digits (TCBU: $00B, TLRU: $00B). (Refer to figure 15.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digits first, and then the high-order digits. The timer/event

Table 16. Timer Mode Register A

TMA3	TMA2	TMA1	TMA0	Source prescaler, input clock period, operation mode	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	Time base mode
			1	PSW, 16 t_{SUBcyc}	
		1	0	PSW, 8 t_{SUBcyc}	
			1	PSW, 2 t_{SUBcyc}	
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

Notes: 1. t_{SUBcyc} = 244.14 μs (when 32.768 kHz crystal oscillation is used.)
2. Timer counter overflow output cycle (s) = Input clock cycle(s) × 256
3. LCD enters into halt mode when PSW/TCA reset is selected during LCD display (Power switch OFF). To display LCD continuously, PSW/TCA reset time must be minimized by programming.

counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digits first, and then the low-order digits. The count value of the low-order digit is obtained when the high-order digit is read.

Timer C (TCCL: $00E, TCCU: $00F, TCRL: $00E, TCRU: $00F): Timer C is consisted of the 8-bit write-only timer load register and the 8-bit read-only timer/counter. These are individually consisted of low-order digits (TCCL: $00E, TCRL: $00E) and high-order digits (TCCU: $00F, TCRU: $00F). The operation mode of timer C is the same as that of timer B.

Table 17. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

Table 18. Timer Mode Register C

TMC3	Auto-reload Function
0	No
1	Yes

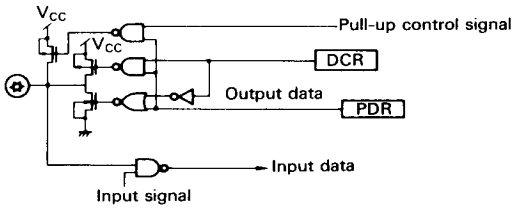
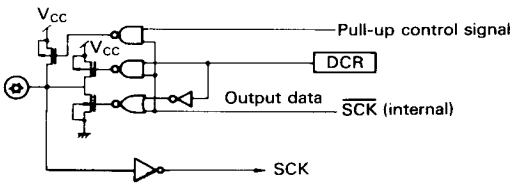
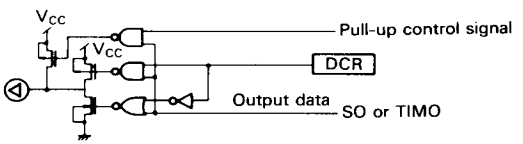
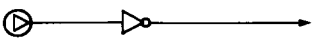
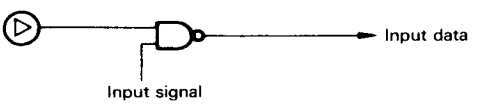
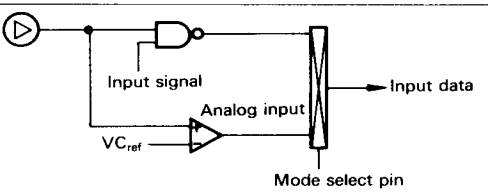
TMC2	TMC1	TMC0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Input/Output

The MCU provides 26 I/O pins and 4 input only pins including 10 high current pins (15 mA max). 26 I/O pins contain pull-up MOS controllable by program.

When every I/O is used as an input, the data control register (DCR) controls ON/OFF of the output buffer. Table 19 shows the I/O pin circuit type.
The configuration of I/O buffers are shown in figure 19.

Table 19. I/O Pin Circuit Type

I/O pins	Circuit	Applicable pins
I/O common pins (with pull-up MOS)		D_0-D_9 RO_0-RO_3 $R1_0$-$R1_3$ $R2_0$-$R2_3$ $R3_0$-$R3_3$
		$\overline{SCK}$
Output pins (with pull-up MOS)		SO TIMO
Input pins		$\overline{INT_0}$ $\overline{INT_1}$ SI
		D_{10} D_{11}/VCref
		D_{12}/COMP0 D_{13}/COMP1 (Multiplexed with analog inputs)

Note: Refer to table 20, Note 3 about RO_2/SO.

Port D: Port D is consisted of 10 1-bit I/O ports and 4 input ports. Ports D_0-D_9 are high current I/O ports (15 mA max). The sum of the current for all ports is up to 100mA. Port D can be set/reset by SED/RED and SEDD/REDD instructions, and can be tested by TD/TDD instructions. An output data is stored in the port data register.

ON/OFF of the output buffer for port D can be controlled by the data control registers for port D (DCRB, DCRC, DCRD). The DCR is located on the memory address area. Pins D_{10}-D_{13} are input only pins.

Two operation modes are available to pins D_{12} and D_{13}: digital input mode and analog input mode. The operation modes can be selected by the port mode register (PMRB; bits 1, 0). In the digital input mode, these pins can be used as input with the same characteristics as other I/O pins. In the analog input mode, users can read the result of the comparison between the reference voltage as an input data. The reference voltage is input by D_{11}/VCref.

Port R: Port R, consisted of 16 4-bit I/O ports, can receive/transmit data by LAR/LRA and LBR/LRB instructions. An output data is stored in data register (PDR) of each pin.

ON/OFF of the output buffer for port R can be controlled by the data control registers for port R (DCR0-DCR3).

The DCR is located on the memory address area.

Pins $R0_0$,$R0_1$, $R0_2$ are multiplexed with $\overline{SCK}$, SI, SO, respectively.

Pins $R3_1$, $R3_2$, $R3_3$ are multiplexed with TIMO, $\overline{INT_0}$, $\overline{INT_1}$, respectively. Refer to figure 18.

Controlling the pull-up MOS: All I/O ports, except for pins D_{10}-D_{13}, contain pull-up MOS controllable by program.

Bit 3 of the port mode register B (PMRB3) controls ON/OFF of all pull-up MOS simultaneously. Pull-up MOS is controlled by the port data register (PDR) of each pin. Therefore, each bit of pull-up MOS can be individually ON and OFF. Refer to table 20.

Unused I/O Pins: If unused pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent this; pull-up with V_{CC} through internal pull-up MOS, or pull-up with V_{CC} through a resistor 100kΩ approx.

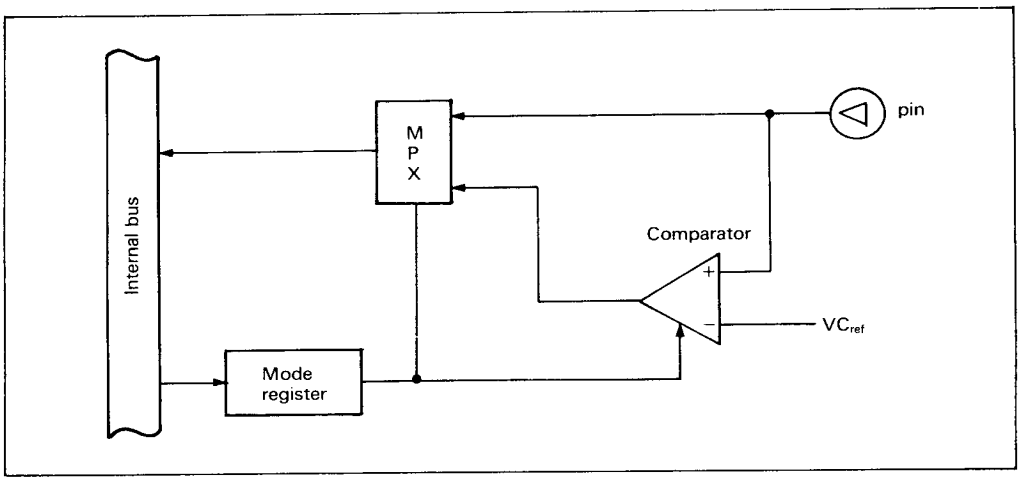
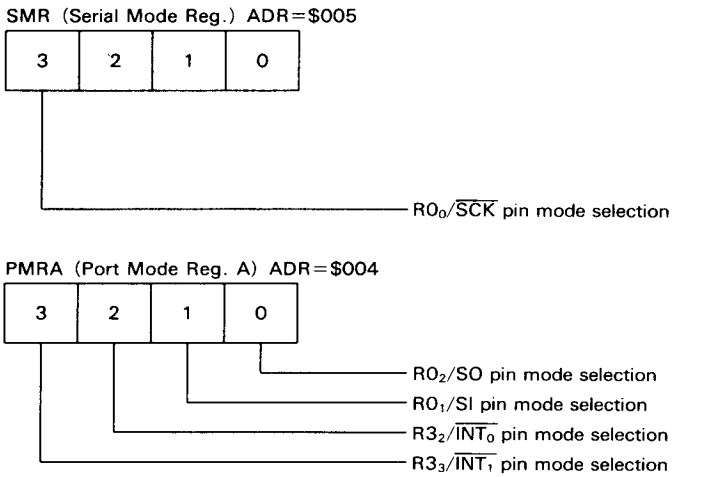


Figure 17. Configuration of D_{12}, D_{13}



SMR bit 3	Port Select
0	$R0_0$
1	$\overline{SCK}$

PMRA bit 3	Port Select	PMRA bit 2	Port Select	PMRA bit 1	Port Select	PMRA bit 0	Port Select
0	$R3_3$	0	$R3_2$	0	$R0_1$	0	$R0_2$
1	$\overline{INT_1}$	1	$\overline{INT_0}$	1	SI	1	SO

PMRB bit 3	Pull up MOS ON/OFF	PMRB bit 2	Port Select	PMRB bit 1	Port Select	PMRB bit 0	Port Select
0	OFF	0	$R3_1$	0	D_{13}	0	D_{12}
1	ON	1	TIMO	1	COMP1	1	COMP0

Figure 18. I/O Select Mode Register

Table 20. Input/Output by Program Control

PRMB; bit 3	0				1			
DCR	0		1		0		1	
PDR	0	1	0	1	0	1	0	1
PMOS (A)	–	–	–	ON	–	–	–	ON
NMOS (B)	–	–	ON	–	–	–	ON	–
Pull-up MOS	–	–	–	–	–	ON	–	ON

Notes: 1. –: OFF

2. Combine the values of the mode registers above (PMRB3, DCR, PDR) to select input/output for PMOS (A), NMOS (B), and the pull-up MOS individually.
   The DCR and the PDR control each pin. And the PMRB3 controls ON/OFF of all pull-ups.
3. The second bit of the miscellaneone register (MIS2) controls RO_2/SO. When MIS2 is 1, PMOS (A) is OFF.

MIS2	RO_2/SO PMOS (A)
0	ON
1	OFF

4. Correspondence between DCR's and pins are shown below:

DCR	bit 3	bit 2	bit 1	bit 0
DCR0	RO_3	RO_2	RO_1	RO_0
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCRB	D3	D2	D1	D0
DCRC	D7	D6	D5	D4
DCRD	–	–	D9	D8

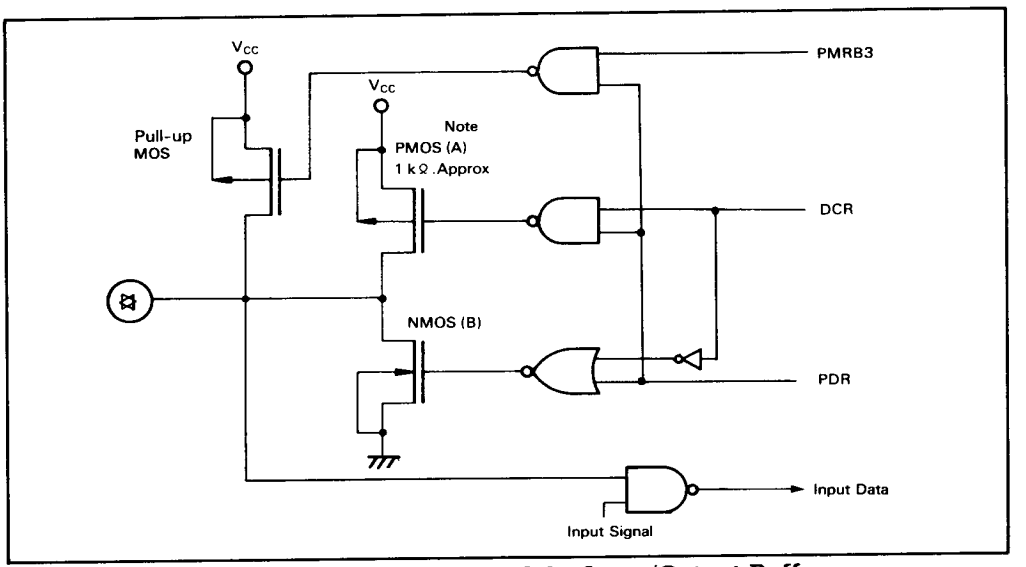


Figure 19. Configuration of the Input/Output Buffer

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when obtaining the stablization time for oscillator, apply the RESET input for at least t_{RC}. In all other cases, at least two instruction cycles of RESET input are required for the MCU reset.

Table 21 shows the parts initialized by MCU reset, and the status of each.

Table 21. Initial Value After MCU Reset

Items		Initial value by MCU reset	Contents
Program Counter	(PC)	$0000	Execute program from the top of the ROM address.
Status	(ST)	1	Enable to branch with conditional branch instructions
Stack Pointer	(SP)	$3FF	Stack level is 0
Register V (Bank Register)	(V)	0	Bank 0 (Memory)
Interrupt	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
Flag/Mask	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Masks interrupt request
I/O	Port Data Register (PDR)	All bits are 1	Enable to transmit high
	Data Control Register (DCR)	All bits are 0	Output buffer is OFF (high impedance)
	Port Mode Register A (PMRA)	0000	See port mode register A
	Port Mode Register B (PMRB)	0000	See port mode register B
Timer/Counter	Timer Mode Register A (TMA)	0000	See timer mode register A
Serial Interface	Timer Mode Register B (TMB)	0000	See timer mode register B
	Timer Mode Register C (TMC)	0000	See timer mode register C
	Serial Mode Register (SMR)	0000	See serial mode register
	Prescaler S	$000	—
	Prescaler W	$00	—
	Timer Counter A (TCA)	$00	—
	Timer Counter B (TCB)	$00	—
	Timer Counter C (TCC)	$00	—
	Timer Load Register B (TLR)	$00	—
	Timer Load Register C (TCR)	$00	—
	Octal Counter	000	—

Table 21. Initial Value After MCU Reset (Cont)

Items		Initial value by MCU reset	Contents
LCD	LCD Control Register (LCR)	000	See LCD control register
	LCD Mode Register (LMR)	0000	See LCD duty/clock control
DTMF Generator	Tone Generator Control Register (TGC)	000	See tone generator control register
	Tone Generator Mode Register (TGM)	0000	See generator mode register
Bit Register	Low Speed On Flag (LSON)	0	See low power dissipation mode
	Watch Dog Timer ON Flag (WDON)	0	See timer C
	Tone Generator Speed Flag (TGSP)	0	See DTMF generation circuit
Miscelaneous Register	(MIS)	000	—

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
Register B	(B)		
Register W	(W)		
Registers X/SPX	(X/SPX)		
Registers Y/SPY	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

Internal Oscillator Circuit

Figure 20 gives an internal oscillator circuit. Ceramic filter can be connected to OSC_1-OSC_2. 32.768 kHz crystal oscillator can be connected to X1, X2. External clock operation is available to the system oscillator.

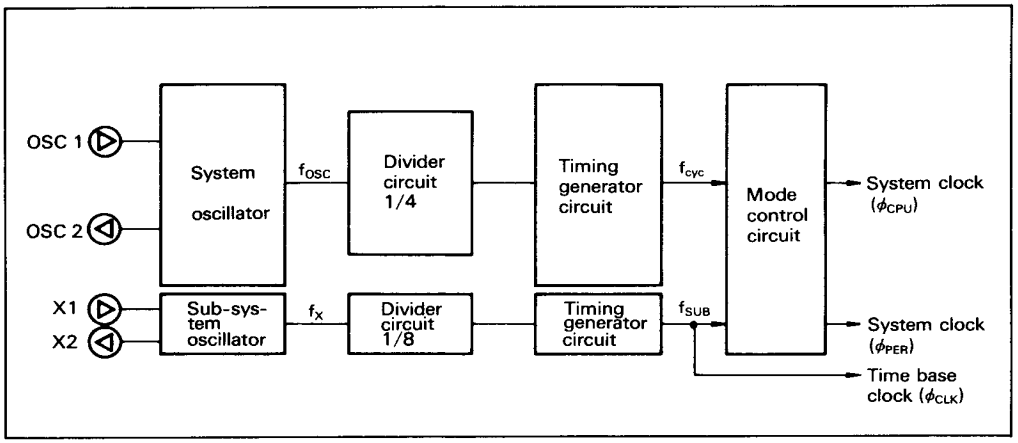


Figure 20. Internal Oscillator Circuit

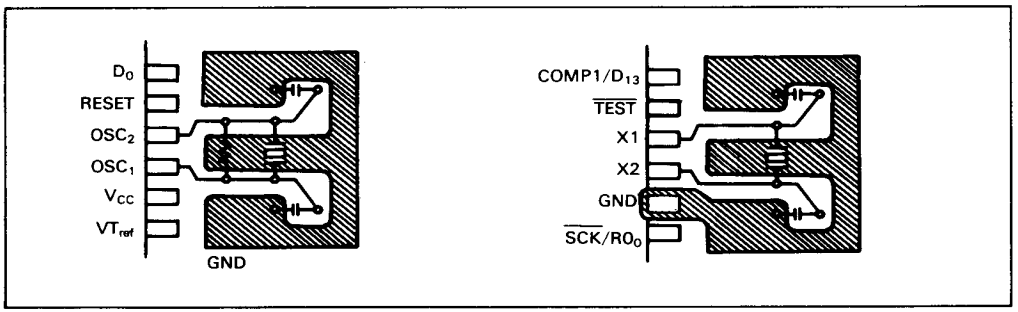
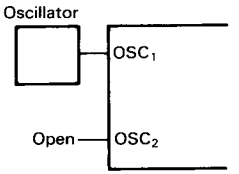
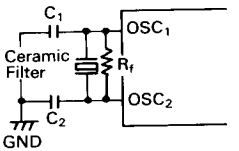
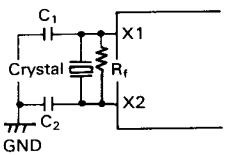
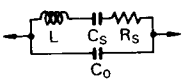


Figure 21. Layout of Crystal and Ceramic Filter

Table 22. Examples of Oscillator Circuit

	Circuit Configuration	Circuit Constants
External clock Operation		
Ceramic filter oscillator		Ceramic filter: CSB400P (Murata) $R_f = 1\ M\Omega \pm 20\%$ $C_1 = C_2 = 220\ pF \pm 5\%$ Ceramic filter: CSB800J (Murata) $R_f = 1\ M\Omega \pm 20\%$ $C_1 = C_2 = 220\ pF \pm 5\%$
Crystal oscillator	 	Crystal: 32.768kHz: MX38T (Nippon Denpa Kogyo) $R_s = 14\ k$ $C_0 = 1.5\ pF$ $C_1 = 6\ pF \pm 20\%$ $C_2 = 20\ pF \pm 20\ \%$

Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.

2. Wiring among OSC_1, OSC_2 (X1, X2) and elements should be as short as possible, and never cross the other wirings. Refer to figure 21.
3. When the crystal (32.768 kHz) is not used, the X1 pin must be fixed to V_{CC} and the X2 pin must be opened.

Liquid Crystal Display (LCD)

The MCU contains 4 common signal pins, the controller, and the driver. The controller and the driver drive 32 segment signal pins. The controller is consisted of dispaly data RAM, the LCD control register (LCR), and the duty/clock control register (LMR) (figure 22).
4 kinds of duties and the LCD clocks are available by program control. And the MCU contains the dual port RAM. Thus displayed data can be transferred to segment signal pins automatically without program control. When you select 32kHz oscillation clock as a LCD clock source, the system allows the LCD display even in the watch mode in which the system clock halts.

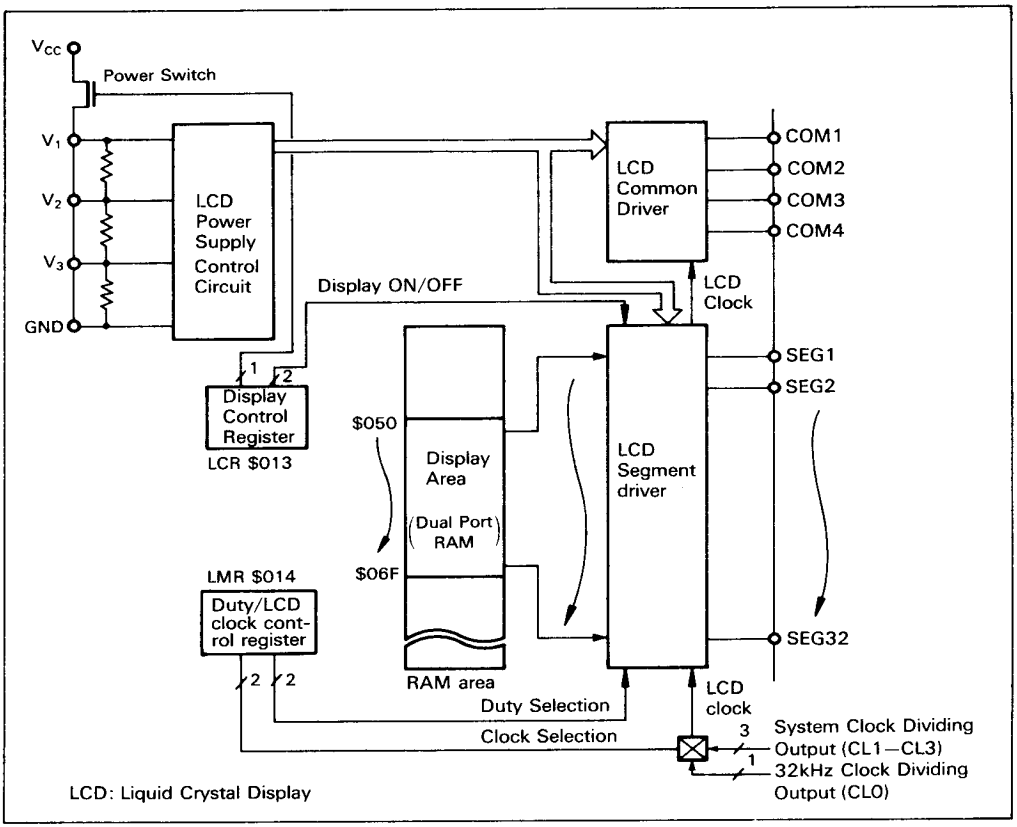


Figure 22. LCD Driver Configuration

LCD Data Area and Segment Data ($050-$06F): Figure 23 shows a configuration of LCD RAM area. Each bit of this area, corresponds to 4 types of duties, can be transmitted to segment as a display data by programming the area corresponding to the duty.

LCD Control Register (LCR: $013): The LCD control register is a 3-bit write only register which controls the blanking of the LCD, ON/OFF of the power switch and the display in the watch mode/subactive mode (table 23).

- Blank/Display
  Blank: Segment signal is faden irrespective of the LCD RAM data.
  Display: LCD RAM data is transmitted as a segment signal.

- Power Switch ON/OFF
  OFF: Power switch is off.
  ON: Power switch is on, and V_1 is V_{CC}.

- Watch Mode/Subactive mode Display
  OFF: In the watch mode/subactive mode, all common/segment pins are fixed to GND. And power switch is off.
  ON: In the watch mode/subactive mode, LCD RAM data is transmitted as a segment signal.

LCD Duty/Clock Control Register (LMR: $014): The LCD duty/clock control register is a write only register which specifies 4 kinds of display duties and reference clock for LCD (table 24).

	bit 3	bit 2	bit 1	bit 0			bit 3	bit 2	bit 1	bit 0	
80	SEG 1	SEG 1	SEG 1	SEG 1	$050	96	SEG 17	SEG 17	SEG 17	SEG 17	$060
81	SEG 2	SEG 2	SEG 2	SEG 2	$051	97	SEG 18	SEG 18	SEG 18	SEG 18	$061
82	SEG 3	SEG 3	SEG 3	SEG 3	$052	98	SEG 19	SEG 19	SEG 19	SEG 19	$062
83	SEG 4	SEG 4	SEG 4	SEG 4	$053	99	SEG 20	SEG 20	SEG 20	SEG 20	$063
84	SEG 5	SEG 5	SEG 5	SEG 5	$054	100	SEG 21	SEG 21	SEG 21	SEG 21	$064
85	SEG 6	SEG 6	SEG 6	SEG 6	$055	101	SEG 22	SEG 22	SEG 22	SEG 22	$065
86	SEG 7	SEG 7	SEG 7	SEG 7	$056	102	SEG 23	SEG 23	SEG 23	SEG 23	$066
87	SEG 8	SEG 8	SEG 8	SEG 8	$057	103	SEG 24	SEG 24	SEG 24	SEG 24	$067
88	SEG 9	SEG 9	SEG 9	SEG 9	$058	104	SEG 25	SEG 25	SEG 25	SEG 25	$068
89	SEG 10	SEG 10	SEG 10	SEG 10	$059	105	SEG 26	SEG 26	SEG 26	SEG 26	$069
90	SEG 11	SEG 11	SEG 11	SEG 11	$05A	106	SEG 27	SEG 27	SEG 27	SEG 27	$06A
91	SEG 12	SEG 12	SEG 12	SEG 12	$05B	107	SEG 28	SEG 28	SEG 28	SEG 28	$06B
92	SEG 13	SEG 13	SEG 13	SEG 13	$05C	108	SEG 29	SEG 29	SEG 29	SEG 29	$06C
93	SEG 14	SEG 14	SEG 14	SEG 14	$05D	109	SEG 30	SEG 30	SEG 30	SEG 30	$06D
94	SEG 15	SEG 15	SEG 15	SEG 15	$05E	110	SEG 31	SEG 31	SEG 31	SEG 31	$06E
95	SEG 16	SEG 16	SEG 16	SEG 16	$05F	111	SEG 32	SEG 32	SEG 32	SEG 32	$06F
	COM 4	COM 3	COM 2	COM 1			COM 4	COM 3	COM 2	COM 1	

Figure 23. Configuration of LCD RAM Area

Table 23. LCD Control Register

LCR bit 2	Watch Mode/Sub-Active Mode Display	LCR bit 1	Power Switch ON/OFF	LCR bit 0	Blank /Display
0	OFF	0	OFF	0	Blank
1	ON	1	ON	1	Display

Note: In case of LCD in the watch mode, use divider output of 32kHz oscillator as an LCD clock and set LCR bit2 to 1. When system oscillator divider output is used as an LCD clock, set LCD bit2 to 0.

Table 24. LCD Duty/Clock Control Register

LMR bit 3	LMR bit 2	LMR bit 1	LMR bit 0	Duty Select/Input Clock Select
		0	0	1/4 Duty
		0	1	1/3 Duty
		1	0	1/2 Duty
		1	1	Static
0	0			CL0 (32.768kHz/64; when 32.768kHz oscillator is used)
0	1			CL1 (f_{cyc}/256)
1	0			CL2 (f_{cyc}/2048)
1	1			CL3 (Refer to table 25.)

Note: f_{cyc} is a system oscillator divider output.

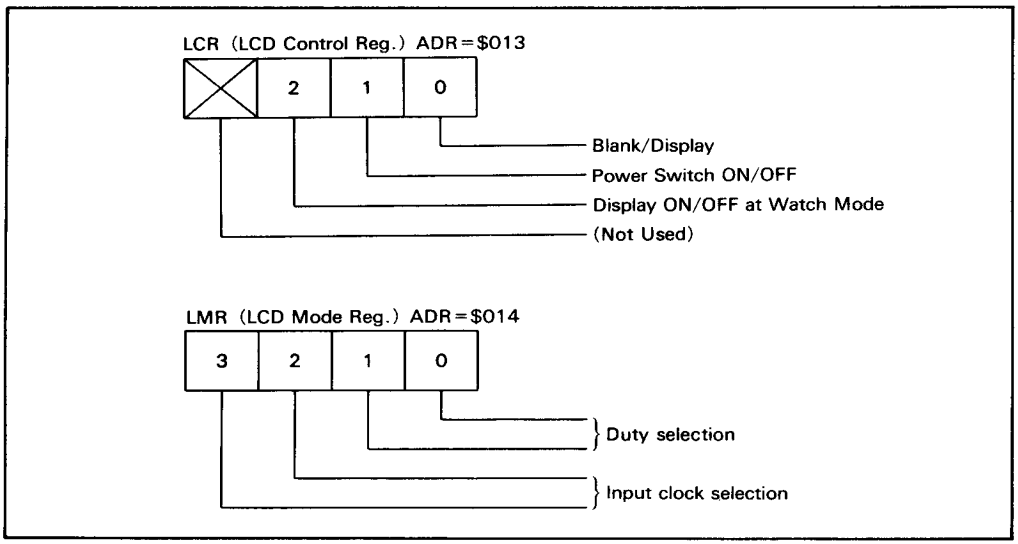


Figure 24. LCD Control Register

Table 25. LCD Frame Frequency

Duty **Static**

LMR / Instruction Cycle Time	bit 3 = 0, bit 2 = 0 (CL0)	bit 3 = 0, bit 2 = 1 (CL1)	bit 3 = 1, bit 2 = 0 (CL2)	bit 3 = 1, bit 2 = 1 (CL3)
10μs	512Hz	390.6Hz	48.8Hz	24.4Hz/64Hz
5μs	512Hz	781.2Hz	97.6Hz	48.8Hz/64Hz

Duty **1/2 Duty**

LMR / Instruction Cycle Time	bit 3 = 0, bit 2 = 0 (CL0)	bit 3 = 0, bit 2 = 1 (CL1)	bit 3 = 1, bit 2 = 0 (CL2)	bit 3 = 1, bit 2 = 1 (CL3)
10μs	256Hz	196.3Hz	24.4Hz	12.2Hz/32Hz
5μs	256Hz	390.6Hz	48.8Hz	24.4Hz/32Hz

Duty **1/3 Duty**

LMR / Instruction Cycle Time	bit 3 = 0, bit 2 = 0 (CL0)	bit 3 = 0, bit 2 = 1 (CL1)	bit 3 = 1, bit 2 = 0 (CL2)	bit 3 = 1, bit 2 = 1 (CL3)
10μs	170.6Hz	130.2Hz	16.3Hz	8.1Hz/21.3Hz
5μs	170.6Hz	260.4Hz	32.6Hz	16.2Hz/21.3Hz

Duty **1/4 Duty**

LMR / Instruction Cycle Time	bit 3 = 0, bit 2 = 0 (CL0)	bit 3 = 0, bit 2 = 1 (CL1)	bit 3 = 1, bit 2 = 0 (CL2)	bit 3 = 1, bit 2 = 1 (CL3)
10μs	128Hz	97.7Hz	12.2Hz	6.1Hz/16Hz
5μs	128Hz	195.4Hz	24.4Hz	12.2Hz/16Hz

* Division ratio differs depending on the value of bit 3 of the timer mode register (TMA3). (TMA3 = 0/TMA3 = 1)

TMA3 = 0	CL3 = f_{cyc}/4096
TMA3 = 1	CL3 = 32.768 kHz/512

Large LCD Panel Driving and Driving Voltage (V_{LCD}): When using the large LCD panel, lower the dividing resistance by implementing the external resisters parallel to the internal dividing resistors (See the following figure).

Since the liquid crystal display board is of matrix configuration, the path of the charge/discharge current through the load capacitors is very complicated. Moreover, as it varies depending on display condition, a value of resistance cannot be simply determined by referring to the load capacitance of liquid crystal display. A value of resistance must be experimentally determined according to the demand for power consumption of the equipment in which the liquid crystal display is implemented.
Capacitor C (0.1 to 0.3 μF) is recommended to be attached. In general, R is 1 kΩ to 10 kΩ.

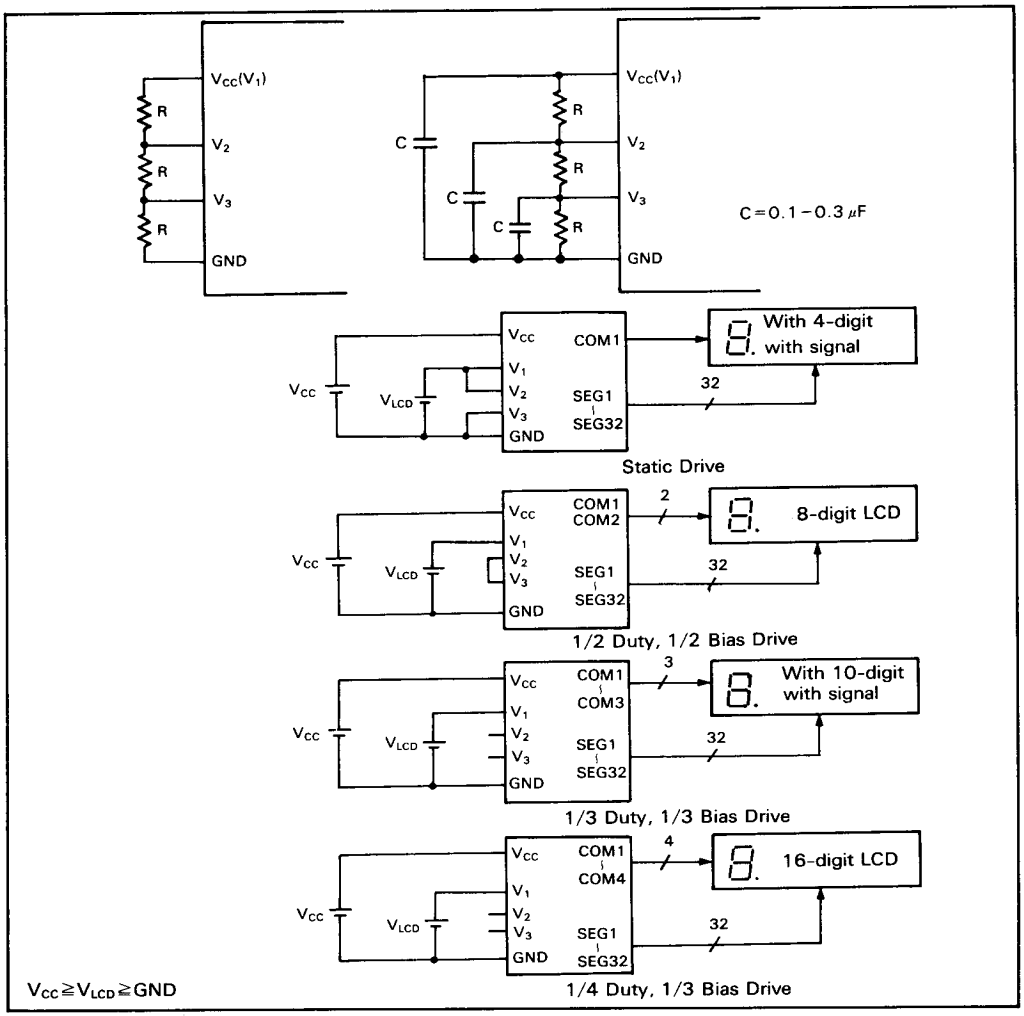


Figure 25. An Example of LCD Connection

The following figure shows a connection when changing the liquid crystal driving voltage (V_{LCD}). In this case, power supply switch for dividing resistor (power switch) should be turned OFF (Bit 1 of the LCR register is 0).

DTMF Generation Circuit

The MCU provides a dual tone multi-frequency (DTMF) generation circuit.

The DTMF signal consists of two sine waves to access the switching system.

Figure 26 shows DTMF keypad and frequencies. Press one of the keys to generate tones which corresponds to each frequencies. Figure 27 shows a block diagram of DTMF circuit.

The MCU uses oscillation frequency reduced to 400kHz, a eighth of convensional one, to realize a low power consumption. In this case, the problem is a frequency deviation. The MCU provides transformed programmable dividers in addition to sine wave counters and a control register to reduce a frequency deviation.

The DTMF generation circuit is controlled by the following three registers.

Tone Generator Mode Register (TGM: $010): The TGM register is a 4-bit write-only register which controls output frequencies (table 26), and is cleared to $0 at MCU reset.

Tone Generator Control Register (TGC: $011): The TGC register is a 3-bit write-only register which controls start/stop of DTMF signal output (table 27), and is cleared to $0 at MCU reset.

Tone Generator Speed Flag (TGSP: $020, 2): The TGSP flag is a 1-bit register which can be set/reset by SEM/REM and SEMD/REMD instruction. The DTMF generation circuit generates output frequencies as table 26 shows when 400kHz clock is selected. When 800kHz clock is selected, the DTMF generation circuit generates equivalent frequencies by pulling TGSP flag high.

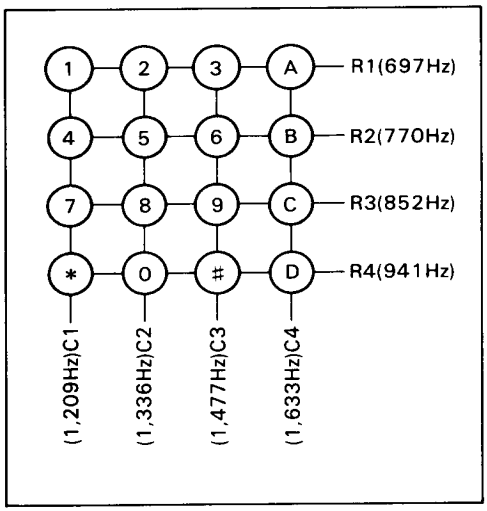


Figure 26. DTMF Keypad and Frequencies

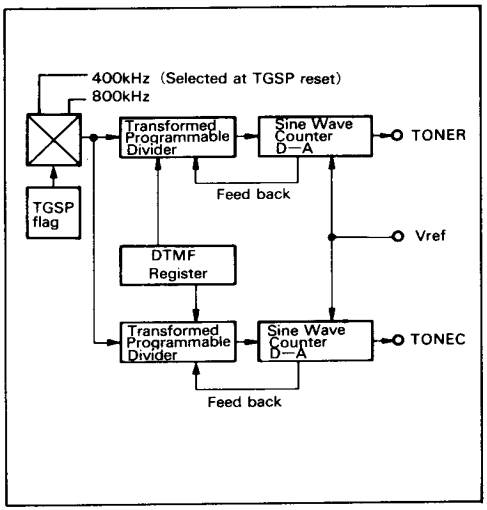


Figure 27. Block Diagram of DTMF Circuit

Table 26. Tone Generator Mode Register

TGM						
bit 3	**bit 2**	**bit 1**	**bit 0**	**Output Frequencies**		
Option		0	0	f_{R1}(:	697Hz)	Output through
(TONER output		0	1	f_{R2}(:	770Hz)	TONER pin
is not affected)		1	0	f_{R3}(:	852Hz)	
		1	1	f_{R4}(:	941Hz)	
0	0	Option		f_{C1}(:	1,209Hz)	Output through
0	1	(TONEC output		f_{C2}(:	1,336Hz)	TONEC pin
1	0	is not affected)		f_{C3}(:	1,477Hz)	
1	1			f_{C4}(:	1,633Hz)	

Table 27. Tone Generator Control Register

TGC1	DTMF Enable Bit
0	DTMF Disable
1	DTMF Enable

TGC2	TONER Output Control (Row)
0	Stop
1	TONER Output (Active)

TGC3	TONEC Output Control (Column)
0	Stop
1	TONEC Output (Active)

DTMF Output: The sine waves of row-group and high-group are individually converted from digital to analog in the D/A conversion circuit which provides high precision ladder resistance. The DTMF output pins (TONER, TONEC) transmits the sine waves of row-group and high-group, respectively. Figure 28 shows the TONE output equivalent circuit. Figure 29 shows the output waveform. One cycle of this wave consists of 32 slots. Therefore, the output waveform is stable with little distoration. And table 28 details the frequency deviation of the MCU from standard DTMF signals.

Table 28. Frequency Deviation of the MCU from Standard

Standard DTMF (Hz)		MCU (Hz)	Deviation from Standard (%)
R1	697	694.44	−0.37
R2	770	769.23	−0.10
R3	852	851.06	−0.11
R4	941	938.97	−0.22
C1	1,209	1,212.12	0.26
C2	1,336	1,333.33	−0.20
C3	1,477	1,481.48	0.30
C4	1,633	1,639.34	0.39

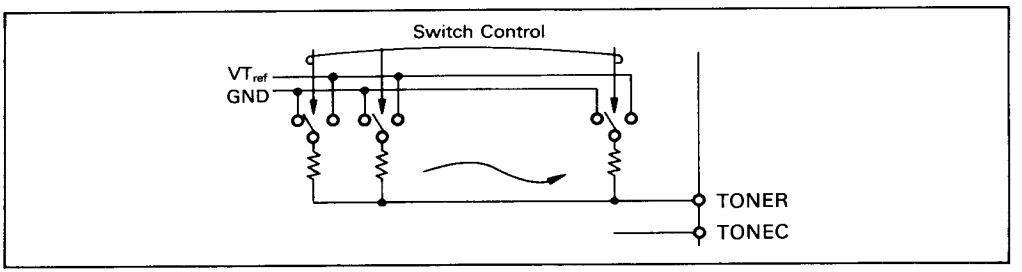


Figure 28. Tone Output Equivalent Circuit

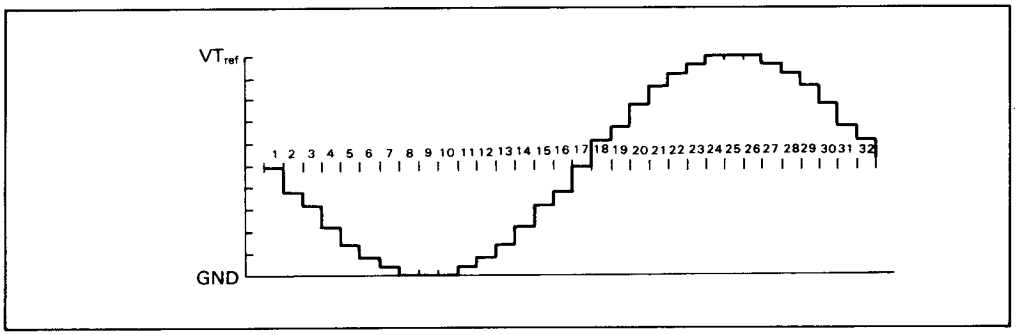


Figure 29. Waveform of Tone Output

Operating Modes

Low Power Dissipation Mode

The MCU has five low power dissipation modes.

Active Mode: In the active mode, the MCU operates through clocks generated in the oscillator circuits: OSC_1 and OSC_2.

Standby mode: Execute SBY instruction to put the MCU into the standby mode from the active mode. In standby mode, the oscillator circuit is active and interrupts, timer/counter, and the serial interface working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 after instruction execution, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. (figure 31)

Figuer 31 shows the flowchart of the standby mode.

Table 29. Low Power Dissipation Mode Function

		Condition								
Operating Mode	**Activated by**	**System oscillator**	**Sub-system oscillator**	**Instruction execution (ϕ_{CPU})**	**Peripheral interrupt (ϕ_{PER})**	**Clock interrupt (ϕ_{CLK})**	**RAM**	**Register/ Flag**	**I/O**	**Riessed by**
Active mode	RESET release Interrupt request	Active	Active	Active	Active	Active	Active	Active	Active[3]	RESET input STOP/SBY instruction
Standby mode	SBY instruction	Active	Active	Stop	Active	Active	Hold	Hold	Hold	RESET input Interrupt request
Stop mode	TMA3=0, Stop instruction	Stop	Active[1]	Stop	Stop	Stop	Hold	Reset	High impedance[3]	RESET input
Watch mode	TMA3=1, Stop instruction	Stop	Active	Stop	Stop	Active[2]	Hold	Hold	Hold[3]	Reset input $\overline{INT_0}$ or Time A interrupt request
Sub-active[4] mode	INT_0 from watch mode or Timer A interrupt request	Stop	Active	Active	Stop	Active[2]	Active	Hold/ Active	Active[3]	RESET input STOP/SBY instruction

Notes: 1. When you minimize the I_{CC}, stop the oscillation by external circuit.
2. Refer to interrupt frame section for details.
3. Refer to table 30.
4. Sub-active mode is a functional option specified via function option list.
5. On using watch mode or Sub-active mode, 32.768 kHz Crystal oscillator is essential for MCU.

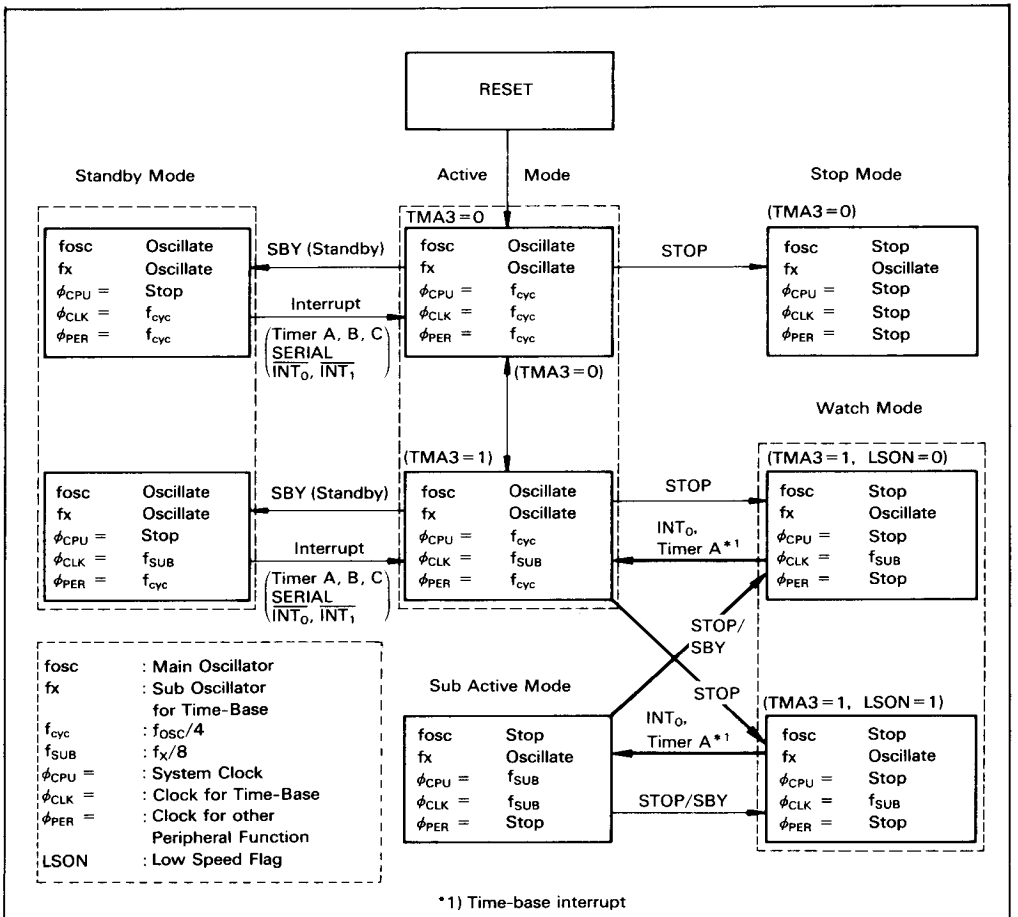
Table 30. I/O State in the Low Power Dissipation Mode

	Output		Input
	Standby mode, Watch mode	Stop mode	Active mode, Sub-active
D_0-D_9	Retained	High impedance	Input enable
D_{10}-D_{13}			Input enable
R0-R3	Retained	High impedance	Input enable

Table 31. Operations in the low power dissipation mode

Functions	Stop mode	Watch mode	Standby mode	Sub-active mode[3]
CPU	Reset	Hold	Hold	Active
RAM	Hold	Hold	Hold	Active
Timer A	Reset	Active	Active	Active
Timer B	Reset	Stop	Active	Stop
Timer C	Reset	Stop	Active[2]	Stop
Serial	Reset	Stop[4]	Active	Stop[4]
LCD	Reset	Active/ Stop	Active	Active/ Stop
DTMF	Reset	Reset	Active	Reset
I/O	Reset[1]	Hold[1]	Hold	Active

Notes: 1. Output pins are in the high impedance state.
2. ▨: in operation
3. Sub-active mode is a functional option specified via functional option list.
4. When a clock is input in the external clock mode, transmit-receive operation is performed (Interrup processing stops).



		ϕ_{CPU}[2] Active	ϕ_{CPU}[2] Stop
ϕ_{PER}[1]	Active	Active mode	Standby mode
	Stop	Sub-active mode	Watch mode (TMA3=1)
			Stop mode (TMA3=0)

Notes: 1. ϕ_{PER} is a clock for peripheral functions other than time base.
2. ϕ_{CPU} is a system clock.

Figure 30. MCU Operation Mode Transfer

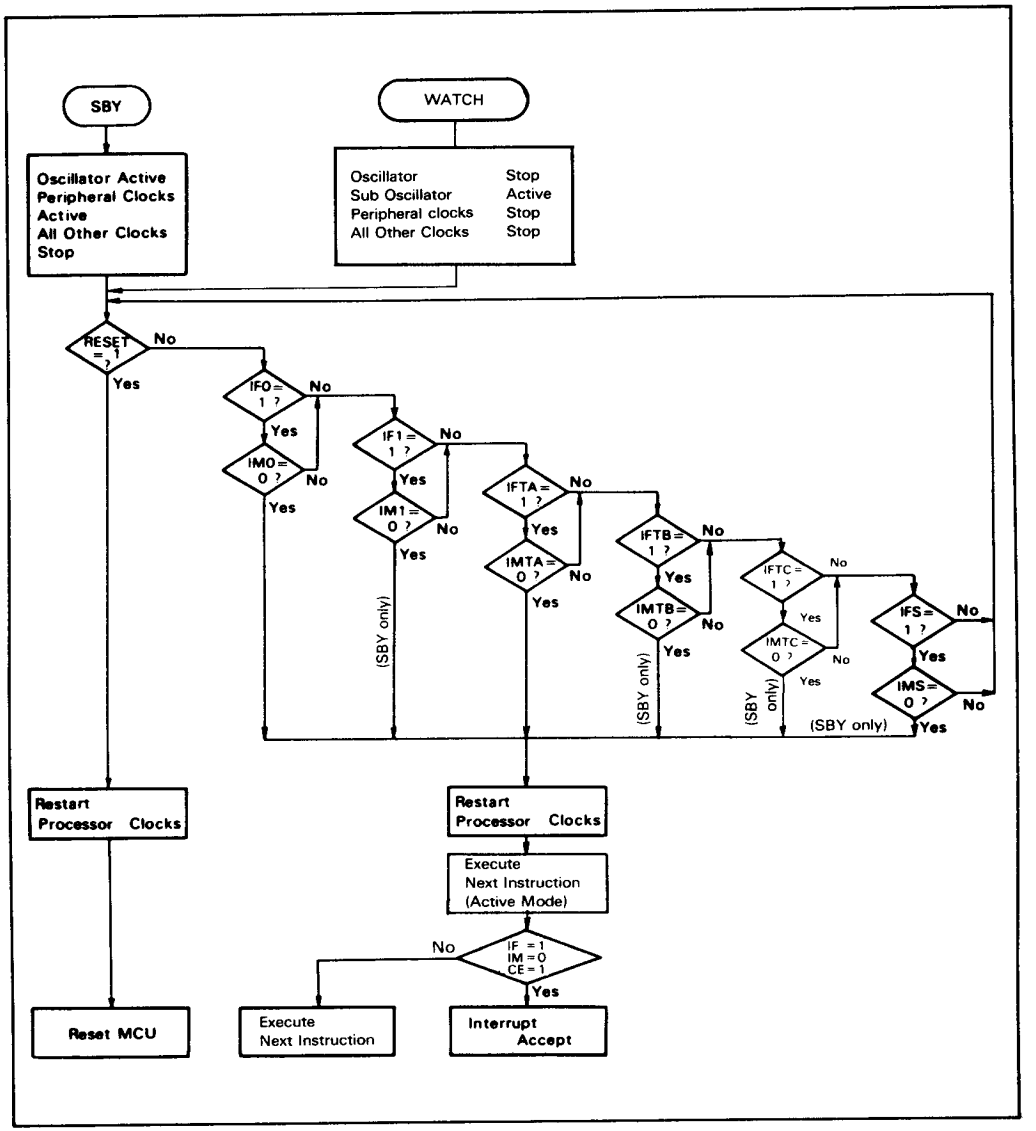


Figure 31. MCU Operating Flowchart

Stop Mode: Execute STOP instruction to put the MCU into the stop mode when the MCU is in the active mode and TMA3 is 0. In the stop mode, oscillator circuit and every function of the MCU stops.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 32, reset input must be applied at least to t_{RC} to stabilize oscillation (Refer to AC Characteristics table). After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, register B, register W, registers X/SPX and Y/SPY, and carry may not retain contents.

Watch Mode: The MCU enters Watch mode by the STOP instruction during Active mode and TMA3=1 or by the STOP or SBY instruction during Sub Active mode. Watch mode can be canceled by the RESET input or timer A/$\overline{INT_0}$ interrupt request. For a detailed description of the RESET input in canceling mode, see Stop mode section. If Watch mode is canceled by the timer A/$\overline{INT_0}$ interrupt request, the MCU enters either Active mode or Sub Active mode depending on the state of the LSON bit. When the MCU enters Active mode, the interrupt request is delayed for a half of the interrupt frame period (t_{RC}) in order to wait stabilization of the system oscillation (figure 33). In this case, MCU operation is the same as that when canceling Standby mode (figure 31).

Sub-active Mode: In the sub-active mode,

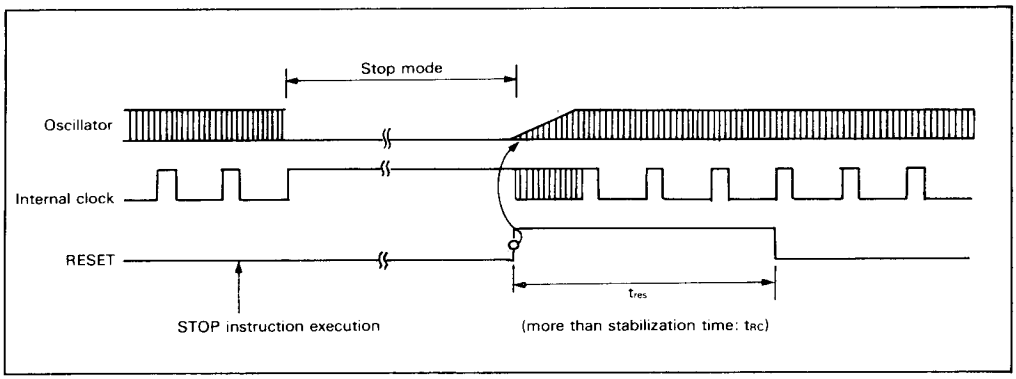


Figure 32. Timing Chart of Recovering from Stop Mode

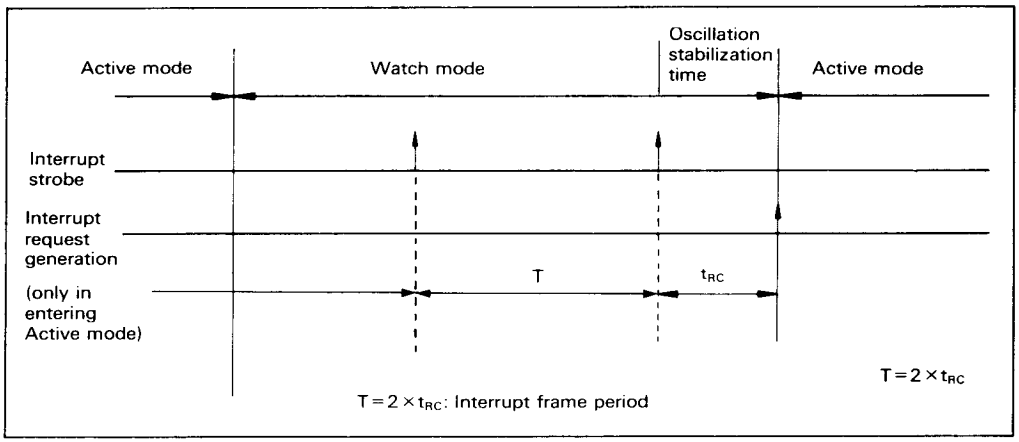


Figure 33. Interrupt Frame

the MCU operates with the clock generated in the oscillator circuit; X1-X2. Timer A/$\overline{INT_0}$ interrupt is generated in this mode with the timing synchronous with the interrupt frame timing.

Note that sub-active mode is a functional option. Therefore, sub-active is available for the devices provided with this option.

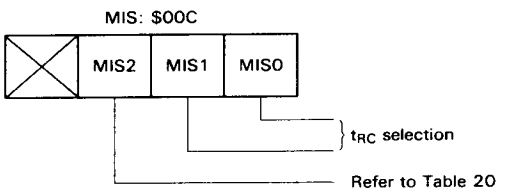
Interrupt Frame: In Watch mode and Sub-Active mode, the time-base clock (ϕ_{CLK}) is applied to timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operates as the time-base and generate the timing clock for the interrupt frame. The interrupt frame period (T) depends on the state of the miscellaneous register as shown in figure 34.

In Watch mode and Sub Active mode, the timer A/$\overline{INT_0}$ interrupt occurs synchronously with the interrupt strobe timing clock. When the MCU wakes up to Active mode from Watch mode, the interrupt request is delayed for a half of interrupt frame period (t_{RC}). The falling edge of $\overline{INT_0}$, which is input regardless of the interrupt frame clock cycle, is equivalent to that synchronous with the interrupt strobe clock just after the falling edge. During oscillation stabilization (t_{RC}) the falling edge of $\overline{INT_0}$ is not recognized. An overflow and interrupt request in timer A occurs synchronously with the interrupt strobe clock.

Limitation on Use

Please pay attention to the following items.

When MCU goes from watch mode to active



MIS		t_{RC}	Oscillation circuit condition
bit 1	bit 0		
0	0	0.12207ms	External clock input
0	1	31.25ms	400/800 kHz ceramic filter
1	0	62.5ms	
1	1	Not Used	—

The value of t_{RC} is applied only when using 32.768 kHz oscillator.

Figure 34. Miscellaneous Register

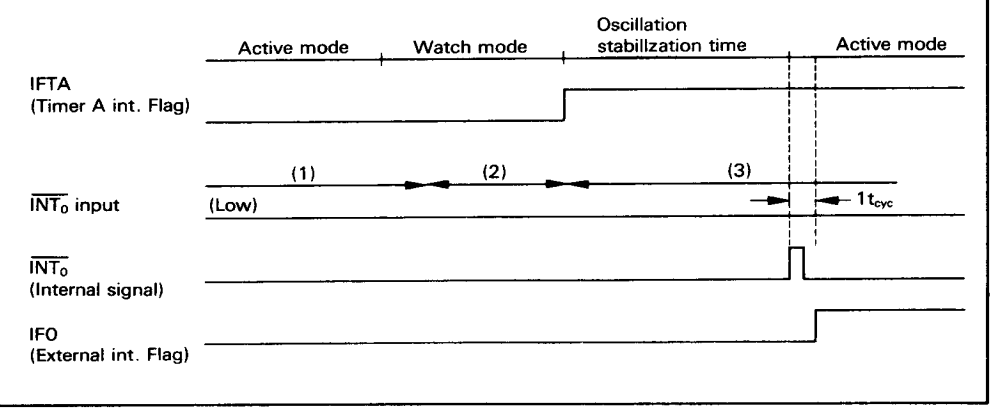


Figure 35. $\overline{INT_0}$ Detect Timing

mode by timer A interrupt request under the following conditions, the timer A interrupt request flag (IFTA) and also the external interrupt request flag (IF0) will be set.

(1) MCU goes from active mode to watch mode in $\overline{INT_0}$ low state.
(2) $\overline{INT_0}$ is low state during watch mode.
(3) MCU goes from watch mode to active mode by timer A interrupt in $\overline{INT_0}$ low state.

Interrupt flag will be set by falling edge of $\overline{INT_0}$ input signal and will not be set without this edge in regular case. However the internal $\overline{INT_0}$ signal is initialized during 1st t_{cyc} after the MCU transition from watch mode to active mode by timer A interrupt, therefore the falling edge will be generated internally with $\overline{INT_0}$ low state during this 1st t_{cyc}. This edge will cause to set IF0. (figure 35)

The $\overline{INT_0}$ input must be high if MCU goes from watch mode to active mode by the timer A interrupt.

MCU Operating Sequence

The MCU operates accoriding to the flowchart shown in figures 36 to 38.

Note that RESET input is asynchronous. Therefore, the MCU is reset immediately after the RESET input supply.

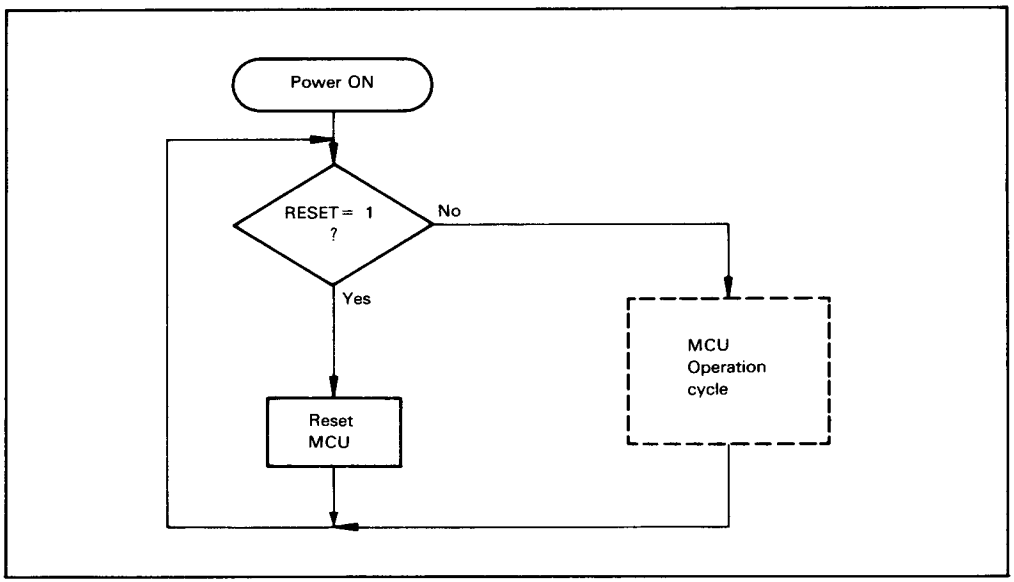


Figure 36. MCU Operating Sequence (Power ON)

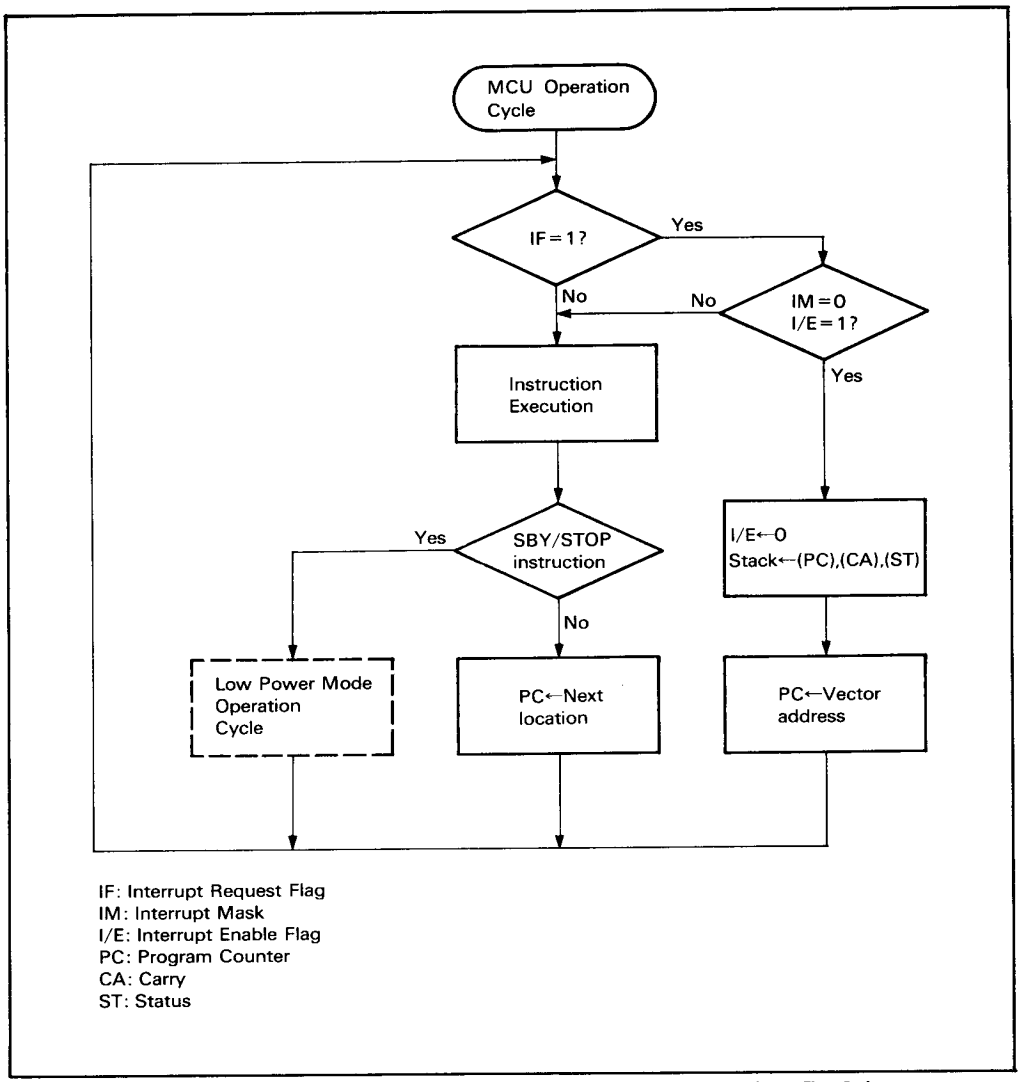


Figure 37. MCU Operating Sequence (MCU Operation Cycle)

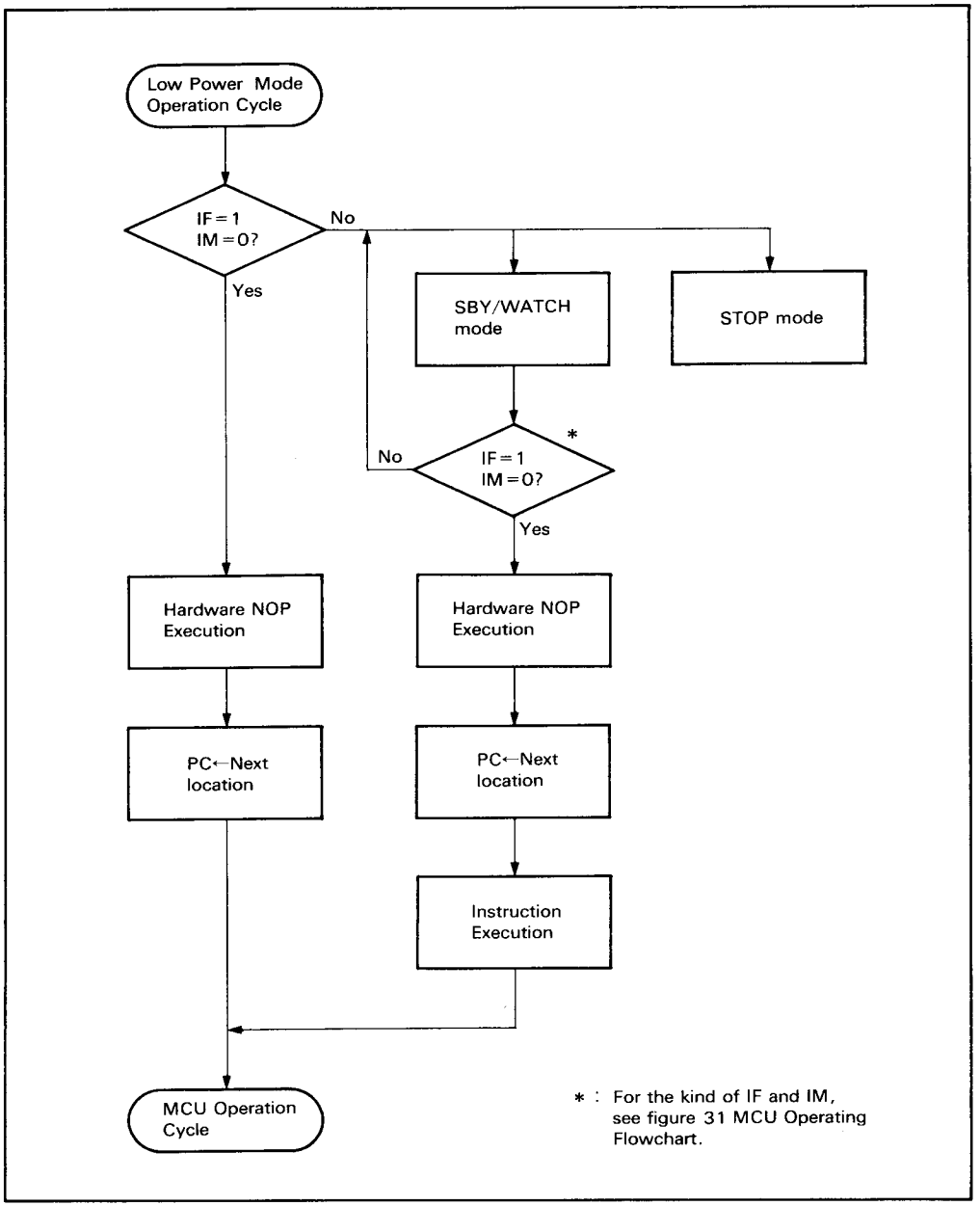


Figure 38. MCU Operating Sequence (Low Power Mode Operation)

Pin Description in PROM Mode

The HD4074608 is a ZTAT microcomputer incorporating PROM. In the PROM mode, the MCU does not operate and the HD4074608 can program the on-chip PROM.

Pin No.		MCU Mode		PROM Mode		Pin No.		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	D_2	I/O	O_2	I/O	41	39	SEG9	O		
2	80	D_3	I/O	O_3	I/O	42	40	SEG10	O		
3	1	D_4	I/O	O_4	I/O	43	41	SEG11	O		
4	2	D_5	I/O	O_5	I/O	44	42	SEG12	O		
5	3	D_6	I/O	O_6	I/O	45	43	SEG13	O		
6	4	D_7	I/O	O_7	I/O	46	44	SEG14	O		
7	5	D_8	I/O			47	45	SEG15	O		
8	6	D_9	I/O			48	46	SEG16	O		
9	7	D_{10}	I	V_{PP}		49	47	SEG17	O		
10	8	D_{11}/VC_{ref}	I	A_9	I	50	48	SEG18	O		
11	9	D_{12}/COMP0	I	$\overline{M0}$	I	51	49	SEG19	O		
12	10	D_{13}/COMP1	I	$\overline{M1}$	I	52	50	SEG20	O		
13	11	$\overline{TEST}$	I	$\overline{TEST}$	I	53	51	SEG21	O		
14	12	X1	I	GND		54	52	SEG22	O		
15	13	X2	O			55	53	SEG23	O		
16	14	GND		GND		56	54	SEG24	O		
17	15	$RO_0/\overline{SCK}$	I/O	A_1	I	57	55	SEG25	O		
18	16	RO_1/SI	I/O	A_2	I	58	56	SEG26	O		
19	17	RO_2/SO	I/O	A_3	I	59	57	SEG27	O		
20	18	RO_3	I/O	A_4	I	60	58	SEG28	O		
21	19	$R1_0$	I/O	A_5	I	61	59	SEG29	O		
22	20	$R1_1$	I/O	A_6	I	62	60	SEG30	O		
23	21	$R1_2$	I/O	A_7	I	63	61	SEG31	O		
24	22	$R1_3$	I/O	A_8	I	64	62	SEG32	O		
25	23	$R2_0$	I/O	A_0	I	65	63	COM1	O		
26	24	$R2_1$	I/O	A_{10}	I	66	64	COM2	O		
27	25	$R2_2$	I/O	A_{11}	I	67	65	COM3	O		
28	26	$R2_3$	I/O	A_{12}	I	68	66	COM4	O		
29	27	$R3_0$	I/O	A_{13}	I	69	67	V_1			
30	28	$R3_1$/TIMO	I/O	A_{14}	I	70	68	V_2			
31	29	$R3_2/\overline{INT_0}$	I/O	$\overline{CE}$	I	71	69	V_3		V_{CC}	
32	30	$R3_3/\overline{INT_1}$	I/O	$\overline{OE}$	I	72	70	TONEC	O		
33	31	SEG1	O			73	71	TONER	O		
34	32	SEG2	O			74	72	VT_{ref}		V_{CC}	
35	33	SEG3	O			75	73	V_{CC}		V_{CC}	
36	34	SEG4	O			76	74	OSC_1	I	V_{CC}	
37	35	SEG5	O			77	75	OSC_2	O		
38	36	SEG6	O			78	76	RESET	I	RESET	I
39	37	SEG7	O			79	77	D_0	I/O	O_0	I/O
40	38	SEG8	O			80	78	D_1	I/O	O_1	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin

V_{PP}
Apply the programming voltage (12.5V ± 0.3V) to V_{PP}.

$\overline{CE}$
Program the internal PROM and input the control signal to enable verify.

$\overline{OE}$
Input the data output control signal when verify.

A_0-A_{14}
A_0-A_{14} are address input pins of the internal PROM.

O_0-O_7
O_0-O_7 are data bus I/O pins of the internal PROM.

$\overline{M_0}$, $\overline{M_1}$
These are for PROM mode specification. To put the MCU into the PROM mode, pull $\overline{M_0}$, $\overline{M_1}$, and $\overline{TEST}$ low, and RESET high.

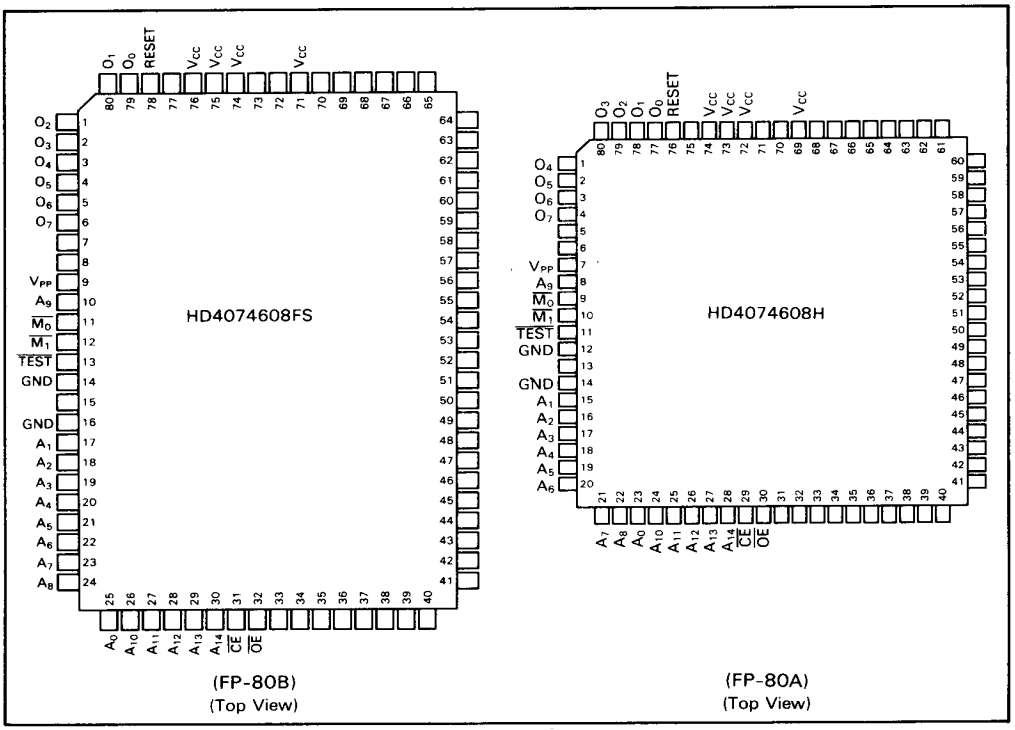


Figure 39. PROM Mode Pin Arrangement

Programmable ROM Operation

The MCU on-chip PROM is programmed in PROM mode (figures 40, 41). PROM mode is set by bringing $\overline{TEST}$, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high as shown in figure 40. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 80-to-28-pin socket adapter. Table 33 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporate conversion circuit to use a general perpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits as shown in figure 41. For example, if 8 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming And Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 32 shows how programming and verification modes are selected.

Figure 42 is a programming flowchart, and figure 43 is a timing chart. For precautions on PROM programming, refer to ZTAT MCU On-Chip PROM Characteristics and Precautions for Applications.

Precautions

1. Addresses \$0000 to \$3FFF should be specfied if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. Data in unused addresses should be set to \$FF.

2. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer of socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.

3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Table 32. PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0-O_7
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 33. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	**Type name**	**Maker**	**Type name**	**Package Type**
DATA I/O	121B	Hitachi	HS460ESF01H	FP-80B
	29B		HS460ESF03H Under Development	FP-80A
AVAL Corp	PKW-1000	Hitachi	HS460ESF01H	FP-80B
			HS460ESF03H Under Development	FP-80A

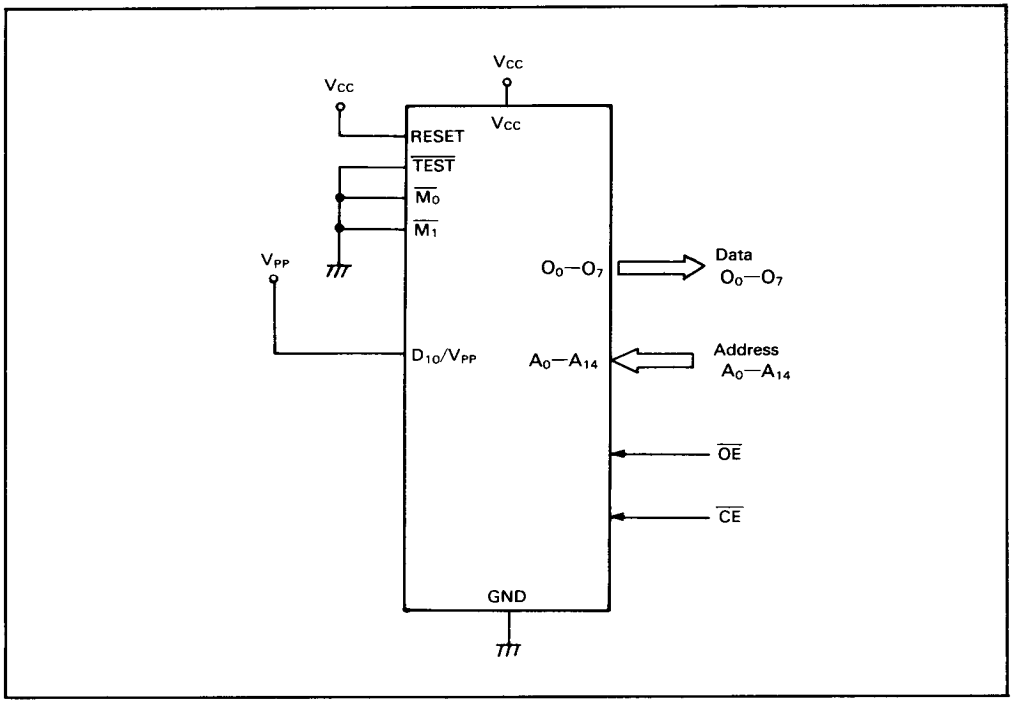


Figure 40. PROM Mode Function Diagram

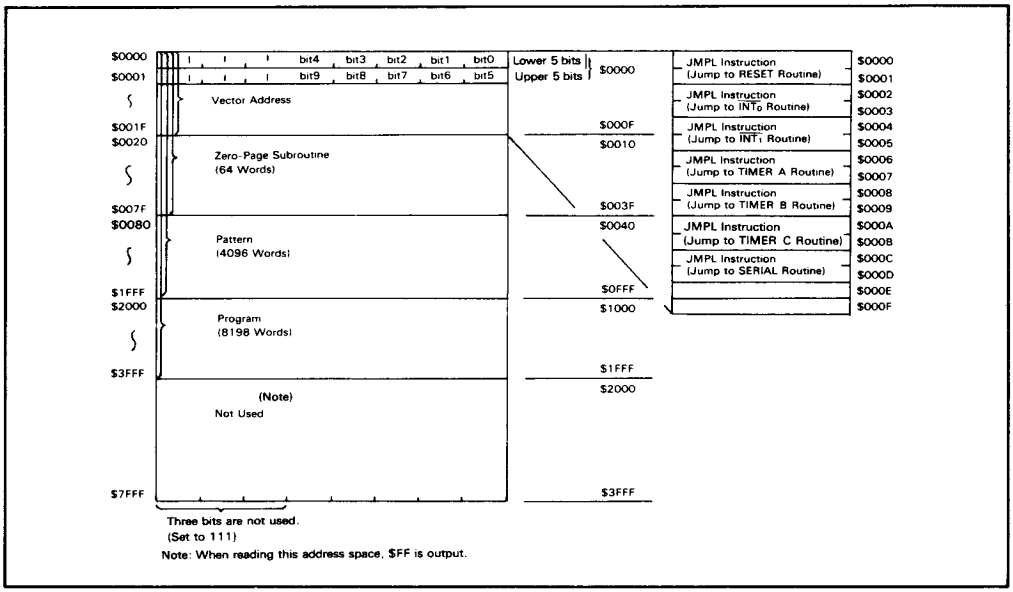


Figure 41. PROM Mode Memory Map

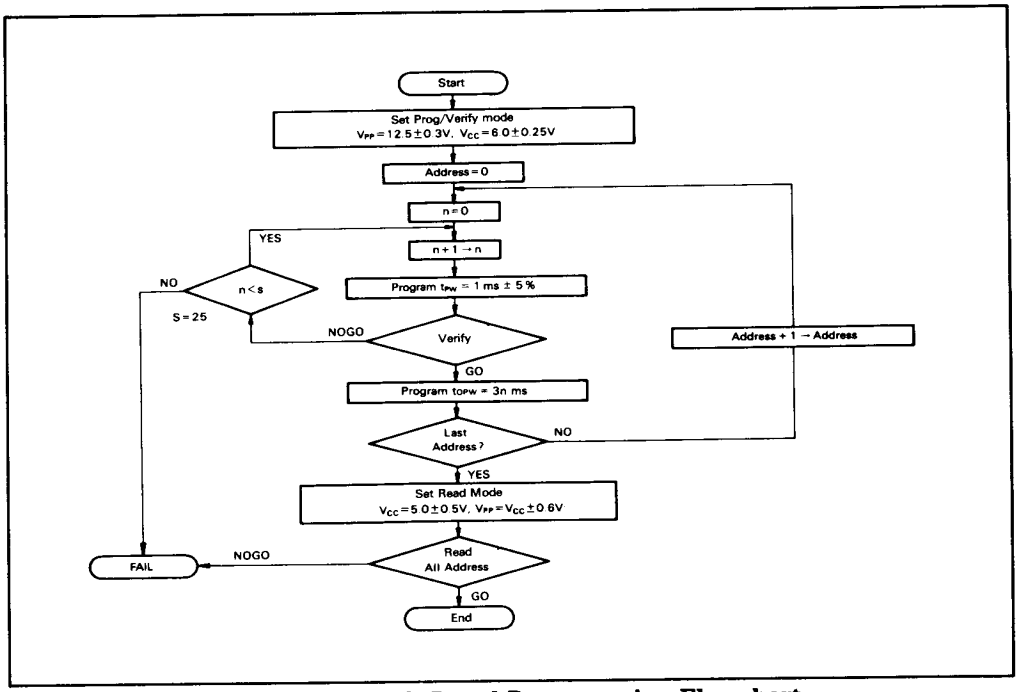


Figure 42. High Speed Programming Flowchart

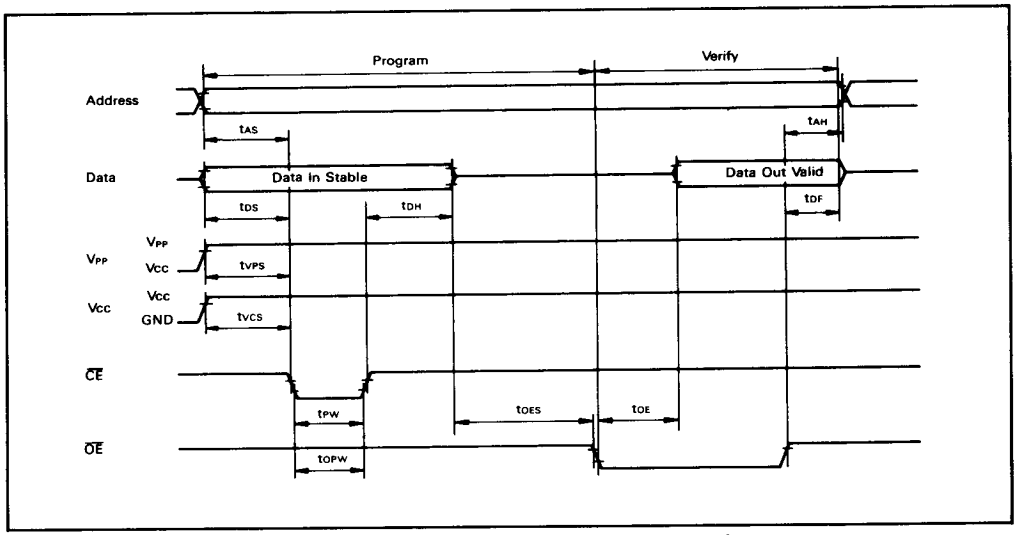


Figure 43. PROM Program/Verify Timing

Programming Electrical Characteristics

DC Characteristics
(V_{CC}=6 V ± 0.25 V, V_{PP}=12.5 V ± 0.3 V, V_{SS}=0 V, Ta=25 °C ± 5 °C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	O_0—O_7, A_0—A_{14}, $\overline{OE}$, $\overline{CE}$	V_{IH}	2.2		V_{CC}+0.3	V	
Input low voltage	O_0—O_7, A_0—A_{14}, $\overline{OE}$, $\overline{CE}$	V_{IL}	−0.3		0.8	V	
Output high voltage	O_0—O_7	V_{OH}	2.4			V	I_{OH}=−200μA
Output low voltage	O_0—O_7	V_{OL}			0.4	V	I_{OL}=1.6mA
Input leakage current	O_0—O_7, A_0—A_{14}, $\overline{OE}$, $\overline{CE}$	$\|I_{LI}\|$			2	μA	V_{in}=5.25V/0.5V
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics
(V_{CC}=6 V ± 0.25 V, V_{PP}=12.5 V ± 0.3 V, Ta=25 °C ± 5 °C, unless otherwise noted.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time	t_{AS}	2			μs	Figure 42*
$\overline{OE}$ set-up time	t_{OES}	2			μs	
Data set-up time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} set-up time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

* Input Pulse level 0.8 to 2.2V
Input rising/falling time ≦ 20ns
Timing reference level { input : 1.0V, 2.0V
output : 0.8V, 2.0V

Precautions on PROM Programming

Principles of PROM Programming/ Erasing

The ZTAT microcomputer has the same type of the memory cell as the EPROM. The PROM is programmed by applying high voltage to the control gate and drain and injecting hot electrons into the floating gate, in the same way in the EPROM programming. The electrons in the floating gate remains stabilized, surrounded by the energy barrier of SiO_2 film. By this electrons, the threshold voltage in the memory cell changes and the corresponding bit goes to 0.

The hot electrons are reduced as over time. This reduction is caused by:

1. Ultraviolet light ·····The electrons are discharged by the ultraviolet light (erasure principle)
2. Heat ·····The electrons, which are excited by heat, are discharged
3. Application of high voltage···The number of electrons is reduced due to the high voltage which is applied to the control gate and drain

If there is any failure in the oxide film, the charge is markedly reduced; however, in general, such reduction does not occur, since devices which failed are usually excluded during screening tests.

When the memory cell does not have any hot electrons in the floating gate, the corresponding bit goes to 1.

PROM Programming

PROM programming should be performed under specified voltage and timing conditions. The higher the program voltage (V_{PP}) and the longer the program pulse width (t_{PW}), the more electrons will be injected into the memory cell. If an overvoltage is applied, a P-N junction may be permanently damaged. It is especially important to note that an overshoot occurs in the PROM writer. Moreover, negative voltage noise causes a parasitic transistor effect, which can reduce the apparent breakdown voltage.

During PROM programming, the ZTAT microcomputer is electrically connected with the PROM writer via the socket adapter. The user should ensure the following:

1. Confirm that the socket adapter is firmly connected to the PROM writer before beginning PROM programming.
2. Do not touch the socket adapter and the LSI during programming; this can cause faulty contacts, resulting in programming errors.

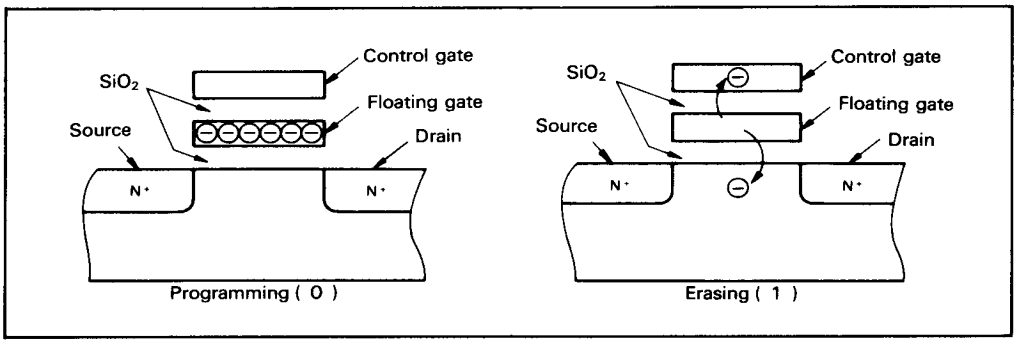


Figure 44. Cross Section of PROM Memory Cell

PROM Reliability after Programming

In general, semiconductor devices retain their reliability, if some initial failures can be rejected. Initial failures can be rejected by adequate screening. "Baking" the device under high-temperature conditions is a screening method which eliminates initial short-time data hold failures in the memory cell (See "Principles of PROM Programming/Erasing"). ZTAT microcomputer devices realize good reliability because they have been subjected to such screening during the water fabrication process. It is recommended that the user expose the device to 150°C at one atmosphere after programming in order to verify device performance.

Figure 45 shows the recommended screening procedure.

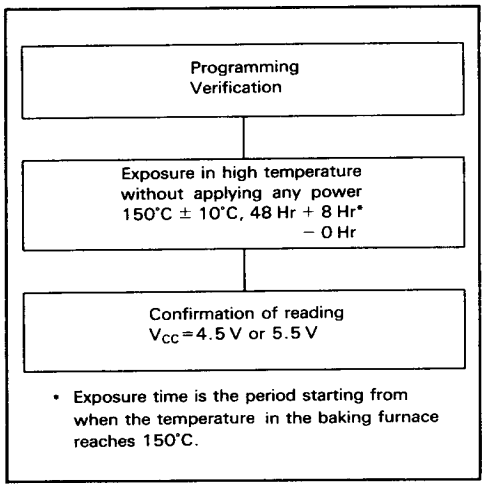


Figure 45. Recommended Screening Procedure

(note) If programming errors occur sequentially during PROM programming, the user should suspend programming and determine whether there is any trouble with the PROM writer or the socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi of the trouble.

RAM Addressing Mode

As shown in figure 46, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from $040 to $04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 47.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address $0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on page boundary (256n + 255) (figure 48), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at $0000-$003F. When a CAL instruction is executed, 6-bit immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 49). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

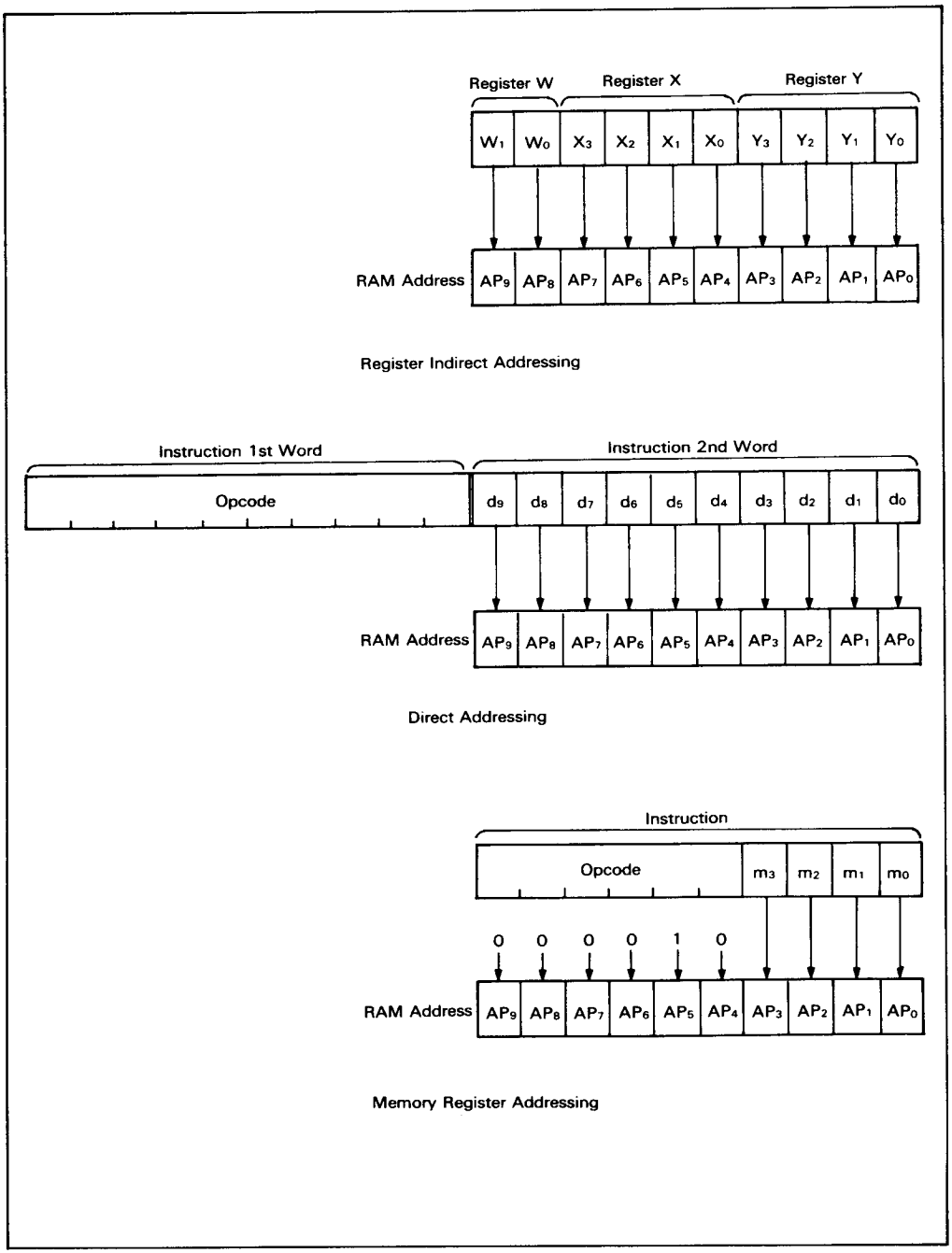


Figure 46. RAM addressing Mode

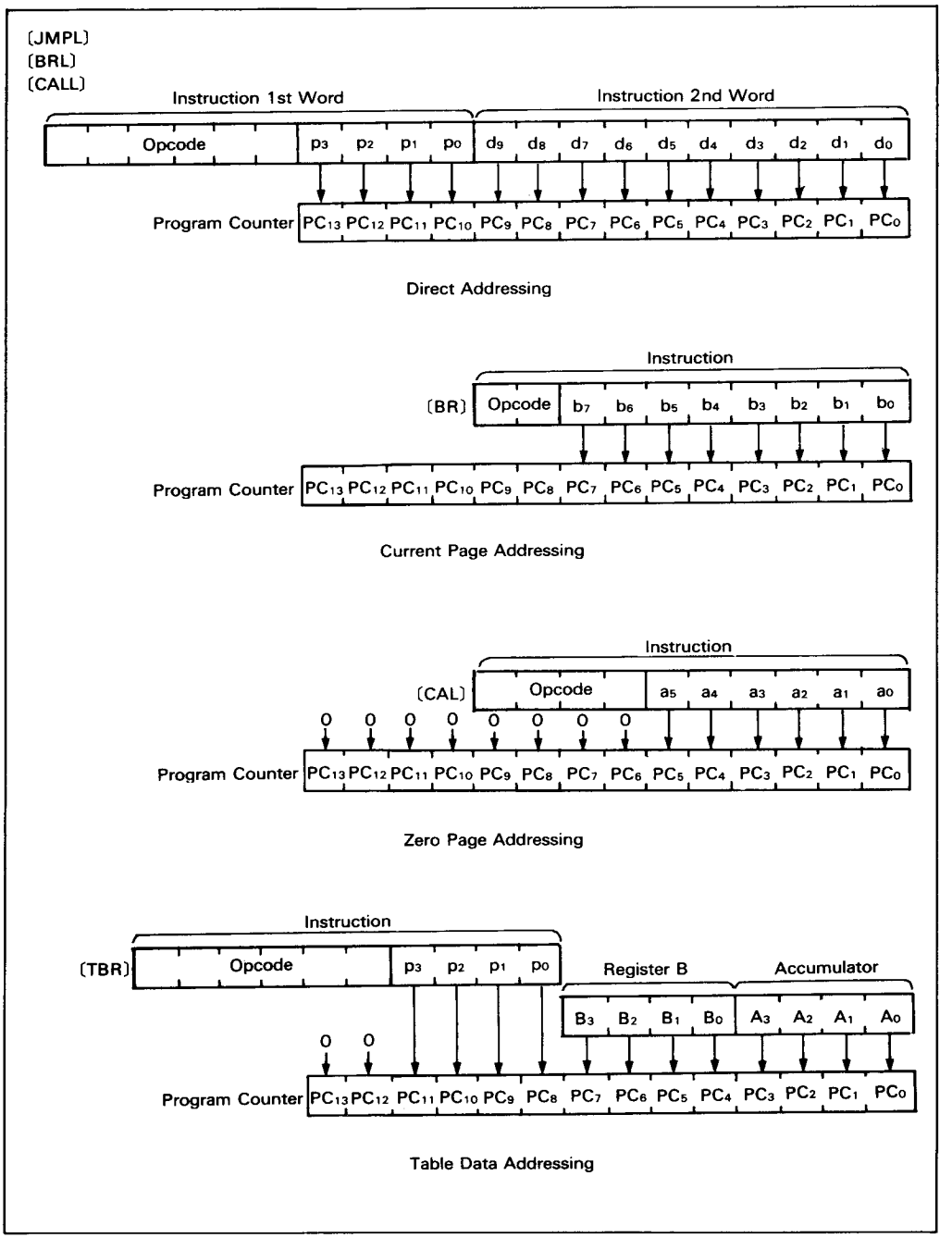


Figure 47. ROM Addressing Mode

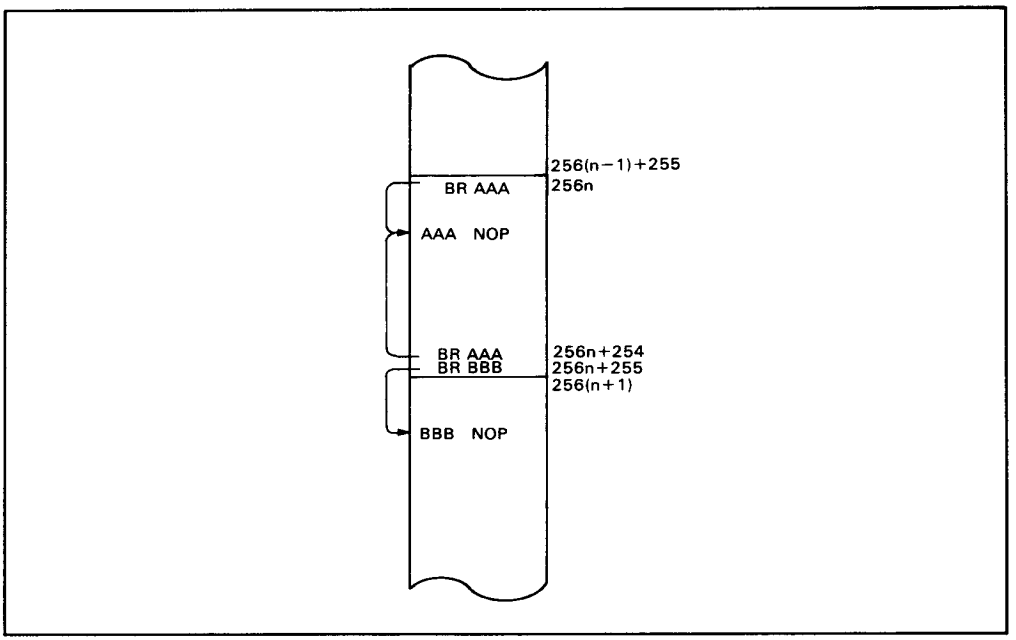


Figure 48. The Branch Destination by BR Instruction on the Boundary between Pages

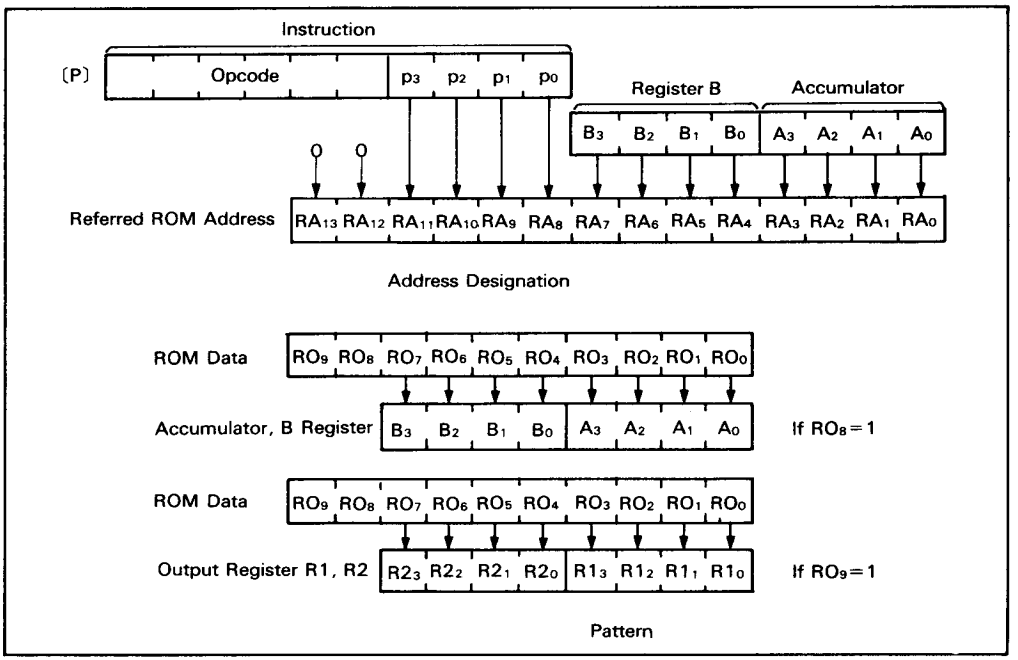


Figure 49. P Instruction

Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction
6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 34-43 list their functions, and table 44 is an opcode map.

Table 34. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M, Y+1→Y	NZ	1/1

Table 35. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 36. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX, Y↔SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 37. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X↔SPX, Y↔SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y−1→Y (X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X↔SPX, Y↔SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X↔SPX, Y↔SPY)		1/1

Note: (XY) and (X) have the following meaning:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).
The op-code X or Y is assembled as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X↔SPX, Y↔SPY

(2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY (X) is given below).
The op-code X is assembled as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 38. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$+1 →A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$ → B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B→A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∩ M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∪ M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ⊕ M→A	NZ	2/2

Note: ∩ : Logical AND
∪ : Logical OR
⊕ : Exclusive OR

Table 39. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 40. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 41. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 42. Input/Output Instructions

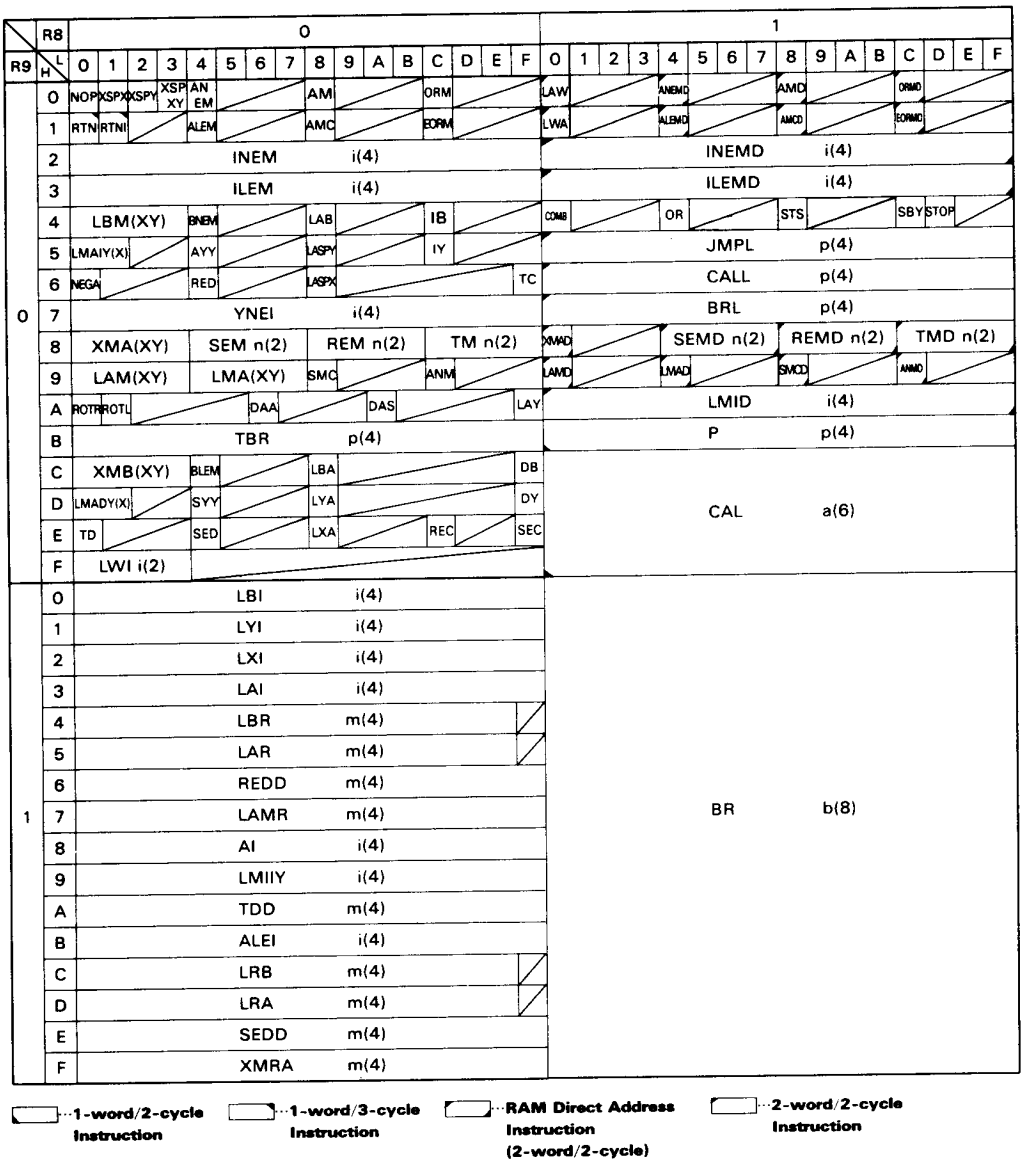
Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 43. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode/Watch Mode*	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode/Watch Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

*: Only when shifted from sub-active mode.

Table 44. Opcode Map



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to + 7.0	V	
Programming Voltage	V_{PP}	−0.3 to + 14.0	V	2
Terminal Voltage	V_T	−0.3 to V_{CC} + 0.3	V	
Total Allowance of Input Current	ΣI_O	100	mA	3
Total Allowance of Output Current	$-\Sigma I_O$	50	mA	4
Maximum Input Current	I_O	4	mA	5, 6
		30	mA	5, 7
Maximum Output Current	$-I_O$	4	mA	8, 9
Operating Temperature	T_{opr}	−20 to + 75	°C	
Storage Temperature	T_{stg}	−55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	−25 to + 80	°C	

Notes: 1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. D_{10} (V_{PP}) of the HD4074608.
3. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
4. Total allowance of output current is the sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. R0-R3
7. D_0-D_9
8. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
9. D_0-D_9, R0−R3.

Electrical Characteristics

DC Characteristics

(HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	0.9 V_{CC}		V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.3		V_{CC} + 0.3	V	External clock operation	
		SI	0.9 V_{CC}		V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	− 0.3		0.1 V_{CC}	V		
		OSC_1	− 0.3		0.3	V	External clock operation	
		SI	− 0.3		0.1 V_{CC}	V		
Output High Voltage	V_{OH}	SCK, TIMO SO	V_{CC}−1.0			V	$-I_{OH}$=0.5mA	
Output Low Voltage	V_{OL}	SCK, TIMO SO			0.4	V	I_{OL}=0.4mA	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, TIMO, OSC_1			1	μA	V_{in} = 0 V to V_{CC}	1
Stop Mode Hold Voltage	V_{stop}	V_{CC}	2			V	Without 32kHz oscillator	7
Current Dissipation in Active Mode	I_{CC1}	V_{CC}		400	1000	μA	V_{CC} = 3 V f_{osc}=400kHz	2
	I_{CC2}	V_{CC}		500	1500	μA	V_{CC} = 3 V DTMF: active f_{osc}=400kHz	3
	I_{CC3}	V_{CC}		1	2	mA	V_{CC} = 3 V f_{osc}=400kHz D_{12}, D_{13} analog input mode	4
Current Dissipation in Standby Mode	I_{stby}	V_{CC}		200	500	μA	V_{CC} = 3 V LCD: ON f_{osc}=400kHz	5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		1	10	μA	V_{CC} = 3 V Without 32kHz oscillator	
Current Dissipation in Sub-active Mode	I_{sub}	V_{CC}		50	100	μA	V_{CC} = 3 V	
				35	70	μA	LCD: ON	6
Current Dissipation in Watch Mode (1)	I_{wtc1}	V_{CC}		5	15	μA	V_{CC} = 3 V LCD: OFF	
Current Dissipation in Watch Mode (2)	I_{wtc2}	V_{CC}		15	35	μA	V_{CC} = 3 V LCD: ON	

Notes:
1. Excluding output buffer current.
2. The MCU is in the reset state. Input/output current does not flow.
   - MCU in reset state
   - RESET, $\overline{TEST}$: V_{CC}
3. The MCU operates and I/O current does not flow.
   - D_{12}, D_{13} digital input mode
   - DTMF operates (Current flowing from VT_{ref} to the GND is excluded.)
4. The D_{12} and D_{13} pins are analog input mode and I/O current does not flow.
   - VC_{ref}/D_{11}, $COMP0/D_{12}$, $COMP1/D_{13}$: GND
   - DTMF does not operate
5. The timer operates and I/O current does not flow.
   - MCU is in standby mode
   - Input/output is in reset state
   - Serial interface: Stop
   - D_{12}, D_{13}: digital input mode
   - DTMF: stop
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
6. Applies to the HD404608.
7. RAM data retention

Input/Output Characteristics for Standard Pin (HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D_{10}–D_{13} R0–R3	0.7 V_{CC}		V_{CC}+0.3		V	
Input Low Voltage	V_{IL}	D_{10}–D_{13} R0–R3	−0.3		0.3 V_{CC}		V	
Output High Voltage	V_{OH}	R0–R3	V_{CC}−1.0			− I_{OH} = 0.5 mA	V	
Pull-up MOS Current	$-I_P$	R0–R3	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	μA	
Output Low Voltage	V_{OL}	R0–R3			0.4	I_{OL} = 0.4 mA	V	
Input/Output Leakage Current	$\|I_{IL}\|$	D_{10}			20	V_{in} = 0V to V_{CC}	μA	2
		R0–R3 D_{11}–D_{13}			1			1
Input High Voltage	V_{IHA}	D_{12}, D_{13} (Analog Compare mode)	VC_{ref} + 0.1				V	
Input Low Voltage	V_{ILA}	D_{12}, D_{13} (Analog Compare mode)			VC_{ref} − 0.1		V	
Analog Input Reference Voltage Scope	VC_{ref}	VC_{ref}	0		V_{CC}−1.2		V	

Notes: 1. Output buffer current is excluded.
2. The maximum value of the HD404608 is 1 μA.

Input/Output Characteristics for High Voltage Pin (HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D_0–D_9	0.7 V_{CC}		V_{CC}+0.3		V	
Input Low Voltage	V_{IL}	D_0–D_9	−0.3		0.3 V_{CC}		V	
Output High Voltage	V_{OH}	D_0–D_9	V_{CC}−1.0			− I_{OH} = 0.5 mA	V	
Pull-up MOS Current	$-I_P$	D_0–D_9	5	40	90	V_{CC}=3V, V_{in}=0V	μA	
Output Low Voltage	V_{OL}	D_0–D_9			2.0	I_{OL} = 15 mA V_{CC}=4.5V to 6V	V	
					0.4	I_{OL} = 0.4 mA		
Input/Output Leakage Current	$\|I_{IL}\|$	D_0–D_9			1	V_{in} = 0V to V_{CC}	μA	1

Note: Output buffer current are excluded.

Liquid Crystal Circuit Characteristics
(HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Segment Driver Descending Voltage	V_{ds}	SEG1 – SEG32			0.6	V	I_d = 3 μA	1
Common Driver Descending Voltage	V_{dc}	COM1 – COM4			0.3	V	I_d = 3 μA	1
LCD Power Supply Divide Resistor	R_{well}		100	300	900	kΩ	Between V1 and GND	
LCD Voltage	V_{LCD}	V1			V_{CC}	V		2, 3

Notes: 1. Descending voltage from the power supply pins V1, V2, V3, and GND to the segment and common pins.
2. Keep the relation $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq GND$ when V_{LCD} is supplied by external power supply.
3. V_{LCD} min = 2.7 V (HD404608)
   V_{LCD} min = 3.0 V (HD4074608)

DTMF Characteristics
(HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
TONE Output Voltage (1)	V_{OR}	TONER	500	660		mVrms	VT_{ref}–GND=2.0 V, R_L=100 kΩ	1
TONE Output Voltage (2)	V_{OC}	TONEC	520	690		mVrms	VT_{ref}–GND=2.0 V, R_L=100 kΩ	1
TONE Output Distortion	$\%_{DIS}$			3	7	%	Short circuit between TONER and TONEC, R_L=100 kΩ	2
TONE Output Ratio	dB_{CR}			2.5		dB	Short circuit between TONER and TONEC, R_L=100 kΩ	2

Notes: 1. See figure 50.
2. See figure 51.

AC Characteristics

(HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC_1, OSC_2		400		kHz	Devided into 4	
				800		kHz		
		X1, X2		32.768		kHz		
Instruction Cycle Time	t_{cyc}			10		μs	fosc = 400kHz	
				5		μs	fosc = 800kHz	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2			30	ms	fosc = 400kHz	1
					30	ms	fosc = 800kHz	1
		X1, X2			3	S	T_a = −10 to +60°C	2
External Clock Frequency	f_{CP}	OSC_1		400		kHz		
				800		kHz		
External Clock High	t_{CPH}	OSC_1	1100			ns	f_{CP} = 400kHz	3
			550			ns	f_{CP} = 800kHz	3
External Clock Low	t_{CPL}	OSC_1	1100			ns	f_{CP} = 400kHz	3
			550			ns	f_{CP} = 800kHz	3
External Clock Rise Time	t_{CPr}	OSC_1			150	ns	f_{CP} = 400kHz	3
					75	ns	f_{CP} = 800kHz	3
External Clock Fall Time	t_{CPf}	OSC_1			150	ns	f_{CP} = 400kHz	3
					75	ns	f_{CP} = 800kHz	3
$\overline{INT_0}$ High Level Width	t_{IOH}	$\overline{INT_0}$	2			t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_0}$ Low Level Width	t_{IOL}	$\overline{INT_0}$	2			t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_1}$ High Level Width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		4
$\overline{INT_1}$ Low Level Width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		4
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		5
Input Capacitance	C_{in}	D_{10}			90	pF	f = 1MHz, V_{in} = 0V	8
		All pins except D_{10}			15	pF	f = 1MHz, Vin = 0V	
RESET Fall Time	t_{RSTf}				20	ms		5
Analog Comparator stabilization time	t_{CSTB}	D_{12}, D_{13} (Analog input mode)			2	t_{cyc}		7

Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7 V (HD4074608: V_{CC} is 3.0 V) after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC}. Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.
2. Oscillation stabilization time it the time until the oscillator stabilizes after V_{CC} reaches 2.7 V (HD4074608: V_{CC} is 3.0 V) after power-on. Time required to stabilize the oscillator (t_{RC}) must be obtained. Since t_{RC} depends on the crystal circuit constant and stray capacitance, please get the manufacturer's advice.
3. See figure 52.
4. See figure 53. The unit t_{cyc} is applied when the MCU is in the standby mode or active mode.
5. See figure 54.
6. See figure 53. The unit t_{SUBcyc} is applied when the MCU is in the watch mode or sub-active mode. t_{SUBcyc} = 244.14 μs (when 32.768 kHz crystal oscillation is used.)
7. Analog comparator stabilization time is the time until the analog comparator stabilizes and correct data can be read after entering D_{12}/D_{13} into analog input mode.
8. The maximum value of the HD404608 is 15 pF.

Serial Interface Timing Characteristics

(HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = −20 to +75°C, unless otherwise noted)

AT Transfer Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	1			t_{cyc}		1.2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{SCK}$	0.5			t_{Scyc}		1.2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{SCK}$			200	ns		1.2
Serial Output Data Delay Time	t_{DSO}	SO			500	ns		1.2
Serial Input Data Set-up Time	t_{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	300			ns		1

AT Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{SCK}$	0.5			t_{Scyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{SCK}$			200	ns		1
Serial Output Data Delay Time	t_{DSO}	SO			500	ns		1.2
Serial Input Data Set-up Time	t_{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	300			ns		1
Transfer Clock Completion Detect Time	t_{SCKHD}	$\overline{SCK}$	1			t_{cyc}		3

Notes: 1. See figure 55.
2. See figure 56.
3. Transfer Clock Completion Detect Timer is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before Transfer Clock Completion Detect Time has passed.

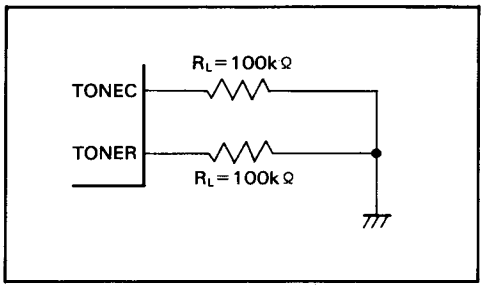


Figure 50. TONE Output Load Circuit

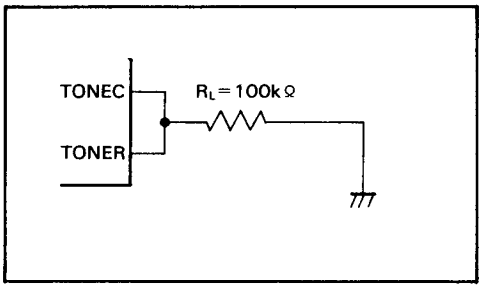


Figure 51. Distortion dB_{CR} Load Circuit

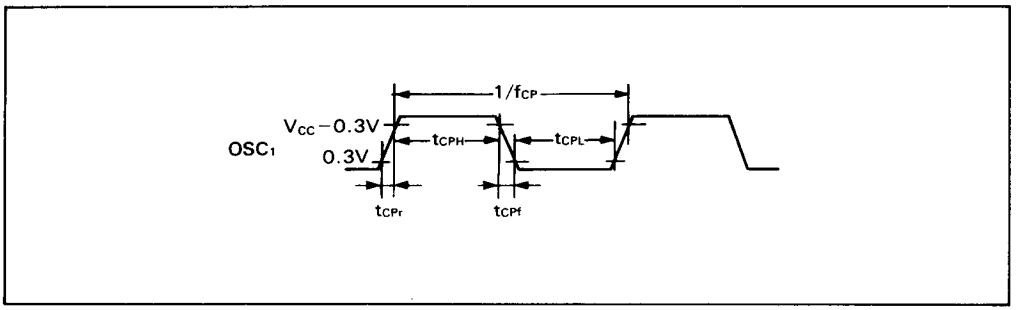


Figure 52. External Clock Timing

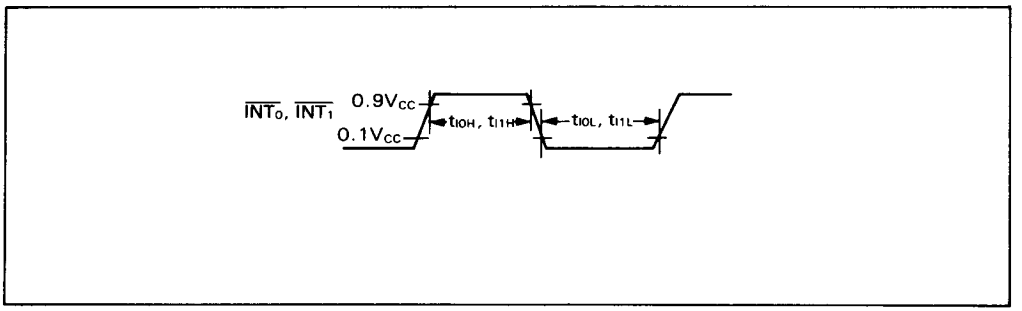


Figure 53. Interrupt Timing

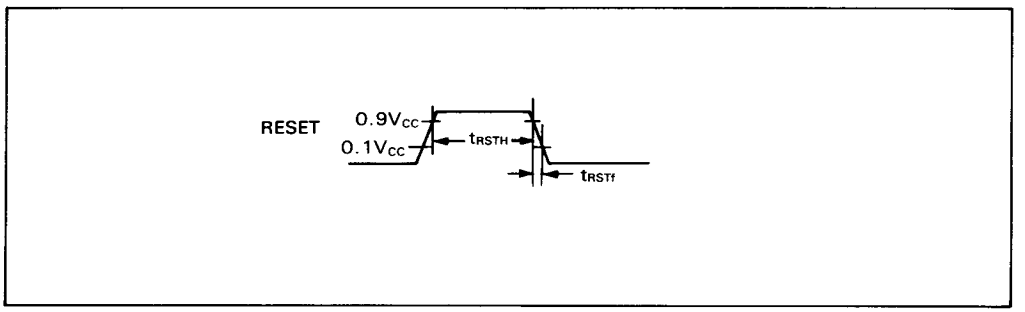


Figure 54. Reset Timing

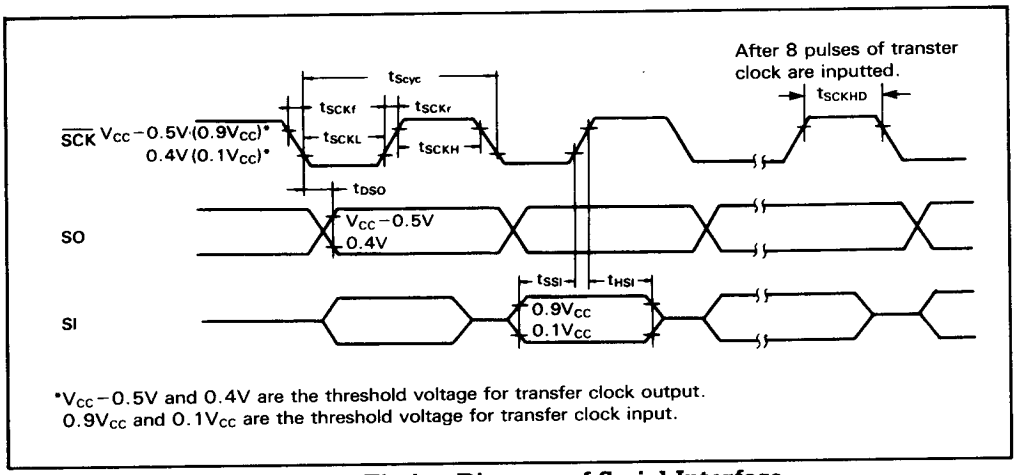


Figure 55. Timing Diagram of Serial Interface

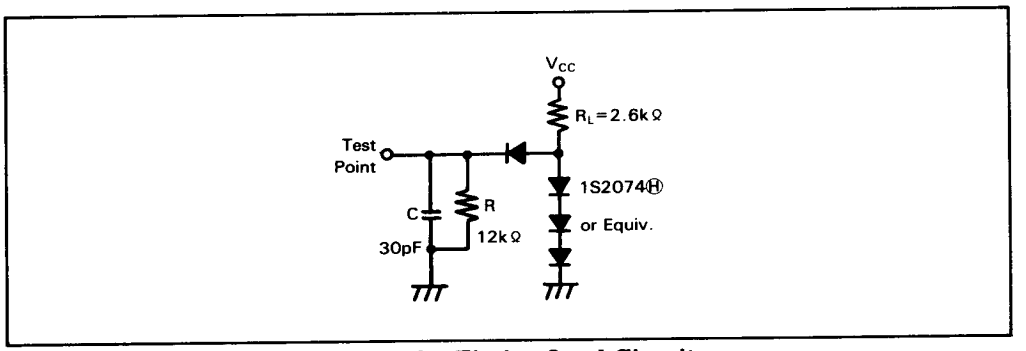


Figure 56. Timing Load Circuit

HD404608 Option List

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number	
Hitachi's Entry	HD404608

Note: Please enter check marks in ☐ (■, ×, ✓).

(1) Functional Option

☐ With 32 kHz CPU Operation and With a Watch Time Base
☐ Without 32 kHz CPU Operation and With a Watch Time Base
☐ Without 32 kHz CPU Operation and Without a Watch Time Base

(2) Package

☐ FP-80A
☐ FP-80B

(3) ROM Code Media

ROM Code Media
■ EPROM On-Package Microcomputer Type

(4) Oscillator

Main	☐ Ceramic Filter Oscillator (f= kHz) ☐ External Clock (f= kHz)
Sub	☐ 32.768kHz Crystal Oscillator ☐ Not Used