HD404272 Series

Description

The HD404272 Series of CMOS 4-bit microcomputers have the same architecture as the HMCS400 Series.

These microcomputers incorporate high-voltage I/O pins, ROM, RAM, 2-channel comparator, 2 timer/counters and a serial interface.

The HD404272 Series includes two chips: HD404272 with 5-V operation; HD40L4272 with low-voltage operation.

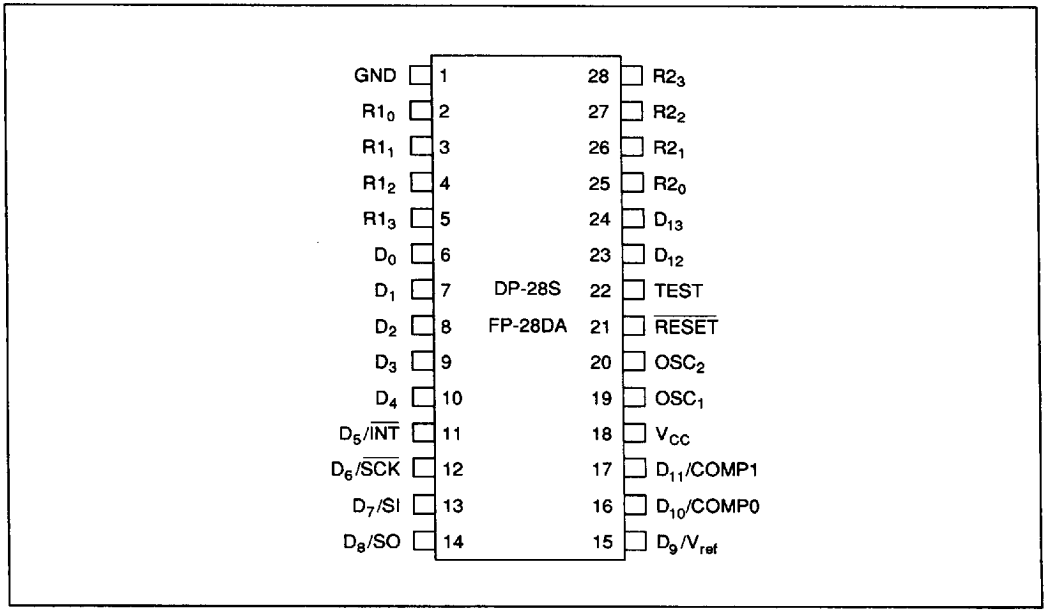
Features

- HMCS400C CPU (software-compatible with the HMCS400 Series)
- 2048-word × 10-bit mask ROM
- 128-digit × 4-bit RAM
- 21 I/O pins and one input pin
  - — 7 standard I/O pins
  - — 14 high-voltage I/O pins
  - — 1 high-voltage input pin
- Two timer/counters
  - — 8-bit free-running or watchdog timer
  - — 8-bit auto-reloading timer/event counter
- Clock-synchronous 8-bit serial interface
- Two-channel voltage comparator
  - — Two analog input pins
  - — Internal reference voltage generator
- External interrupt pin
- Low-power dissipation modes
  - — Standby mode
  - — Stop mode
- Built-in oscillator
  - — Resistor or ceramic oscillator (an external clock is also possible)
- Minimum instruction cycle time
  - — 0.89 µs (f_{OSC} = 4.5 MHz, V_{CC} = 3.5 V–6.0 V) (HD404272)
  - — 3.55 µs (f_{OSC} = 1.125 MHz, V_{CC} = 2.5 V–6.0 V) (HD40L4272)
- Packages
  - — DP-28S (28 pin shrink-type plastic DIP)
  - — FP-28DA (28-pin SOP)

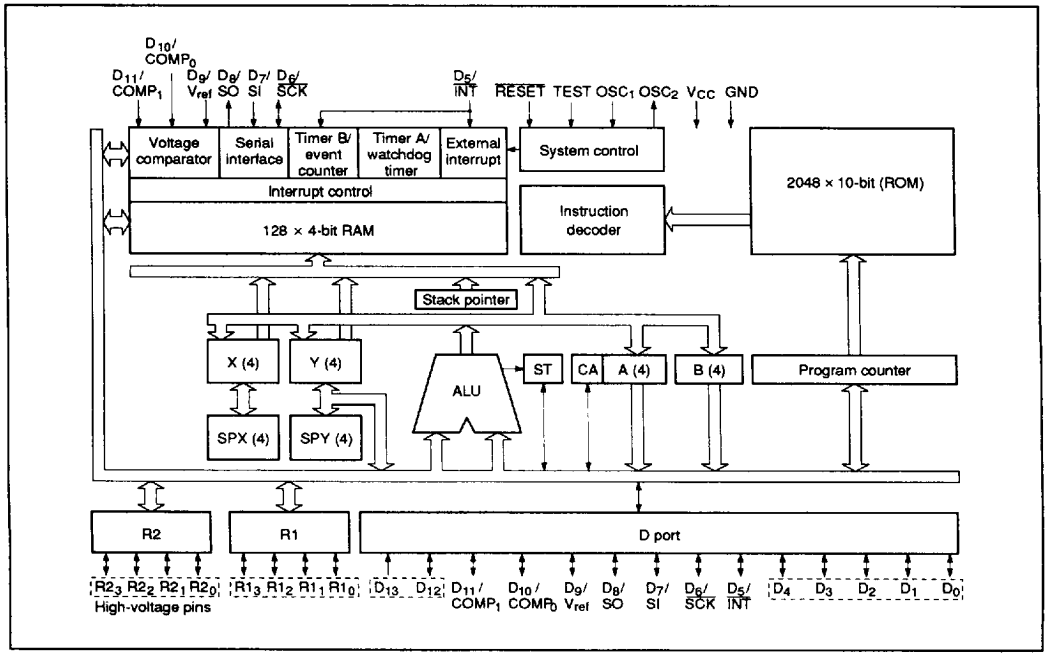
Type of Products

Part No.	Type	Operation Voltage	Package
HD404272S	Mask ROM	3.5 V to 6.0 V	DP-28S
HD404272FP			FP-28DA
HD40L4272S		2.5 V to 6.0 V	DP-28S
HD40L4272FP			FP-28DA

Pin Arrangement



Block Diagram



Pin Description

Item	Symbol	Pin Number	I/O	Function
Power supply	V_{CC}	18		Power supply pin.
	GND	1		Ground connection pin.
Test	TEST	22	I	Pin used for test purposes only. Connect it to ground.
Reset	$\overline{RESET}$	21	I	MCU reset pins.
Oscillator	OSC_1,	19	I	Pins for the internal oscillator circuit. Connect them to a resistor or a ceramic oscillator, or connect OSC_1 to an external oscillator circuit. The internal oscillator is selected by mask option.
	OSC_2	20	O	
Ports	D_5–D_{11}	11–17	I/O	Standard-voltage input/output ports addressable by individual bits and multiplexed with peripheral functions.
	D_0–D_4, D_{12}, D_{13}	6–10, 23, 24	I/O	Individually addressable high-voltage ports. All are I/O ports except for D_{13} which is an input-only port.
	$R1_0$–$R1_3$, $R2_0$–$R2_3$	2–5, 25–28	I/O	High-voltage input/output ports addressable in 4-bit units.
Interrupt	$\overline{INT}$	11	I	Input pin for external interrupt. It is also used as an external event input for timer B. It is multiplexed with pin D_5.
Serial interface	$\overline{SCK}$	12	I/O	Serial interface clock input/output pin. It is multiplexed with pin D_6.
	SI	13	I	Serial interface receive data input pin. It is multiplexed with pin D_7.
	SO	14	O	Serial interface transmit data output pin. It is multiplexed with pin D_8.
Analog comparator	V_{ref}	15	I	Reference voltage pin to input the threshold voltage of the analog input pins.
	COMP0, COMP1	16, 17	I	Analog input pins for the voltage comparator.

Memory Map

ROM Memory Map

The areas in ROM are described below with its memory map shown in figure 1.

Vector Address Area: Locations $0000 through $0009 can be used for JMPL instructions to branch to the starting address of an initialization program for interrupt programs. After MCU reset or an interrupt is performed, the program is executed from a vector address.

Zero-Page Subroutine Area: Locations $0000 through $003F can be used for subroutines. The CAL instruction branches to subroutines within this area.

Pattern Area: The P instruction allows reference to ROM data in this area as a pattern.

Program Area ($0000 to $07FF)

RAM Memory Map

In addition to data and stack areas, interrupt control bits and special function registers are also mapped in RAM memory. The RAM memory map shown in figure 2 is described below.

Interrupt Control Bits Area ($000 to $002): The interrupt control bits area (figure 3) is used for interrupt control. This area and CMR (location $003) register is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($003 to $00C): The special function registers are the mode or data registers for external interrupt, the serial interface, the timer/counters and comparator. These registers are also used as data control registers for I/O ports. These registers are classified into three types: write-only, read-only, and read/write, as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions (except for CMR register).

Data Area ($020 to $07F): The 16 digits of $020 through $02F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area ($0E0 to $0FF): Locations $0E0 through $0FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when a subroutine call (CAL or CALL instruction) or interrupt is performed. This area can be used as an 8-level nesting stack in which one level requires 4 digits. Figure 4 shows the stack area levels. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. When this area is not used as a stack, it becomes available as a data area.

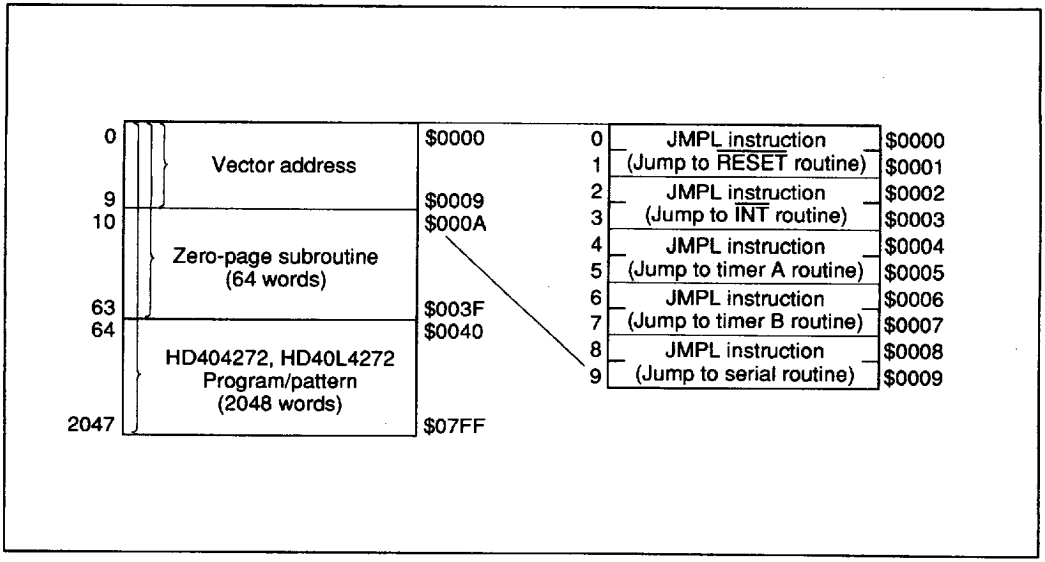


Figure 1 ROM Memory Map

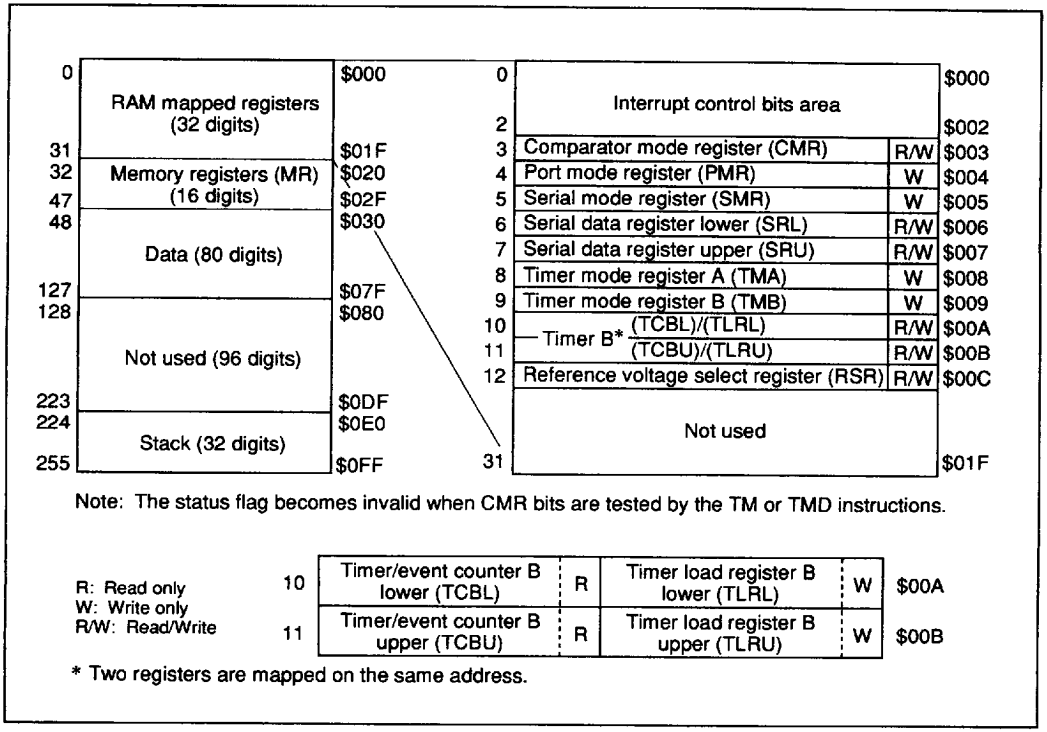


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM of external $\overline{INT}$ (IMEX)	IF of external $\overline{INT}$ (IFEX)	Reset SP bit (RSP)	Interrupt enable flag (IE)	$000
1	IM of timer B (IMTB)	IF of timer B (IFTB)	IM of timer A (IMTA)	IF of timer A (IFTA)	$001
2	Not used	Not used	IM of serial (IMS)	IF of serial (IFS)	$002

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction.
The status flag becomes invalid when the unused bits and RSP bit are tested by the TM or TMD instruction.

Figure 3 Configuration of Interrupt Control Bits Area

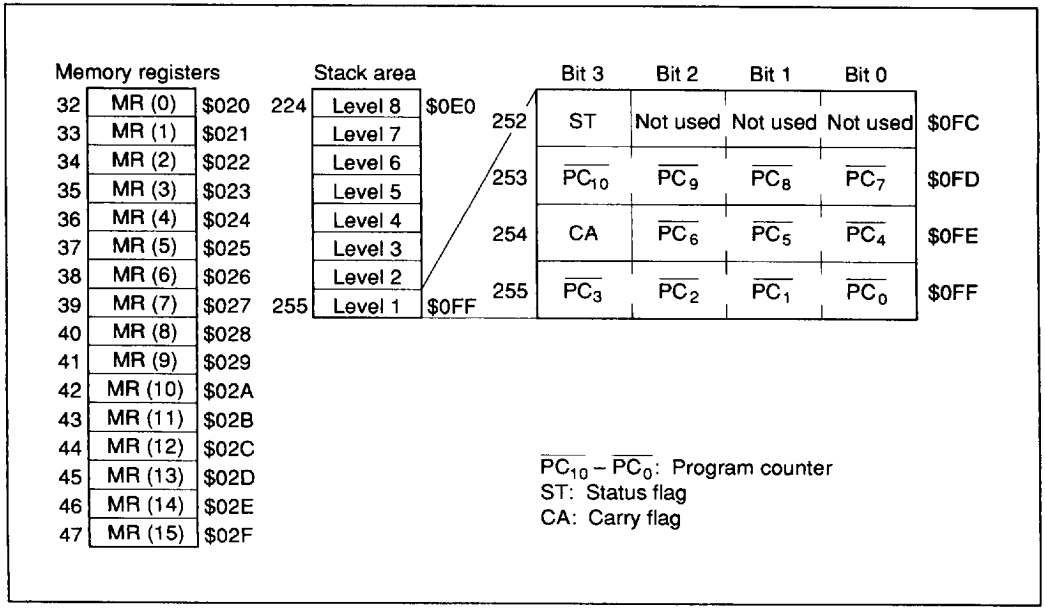


Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has eight registers and two flags for CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

X Register (X), Y Register (Y): The X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, the carry flag is pushed onto the stack and is pulled from the stack only by the RTNI instruction.

Status Flag (ST): The status flag holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for arithmetic or compare instructions. The status flag is also used as a branch condition for the BR, BRL, CAL, and CALL instructions. The value of the status flag remains

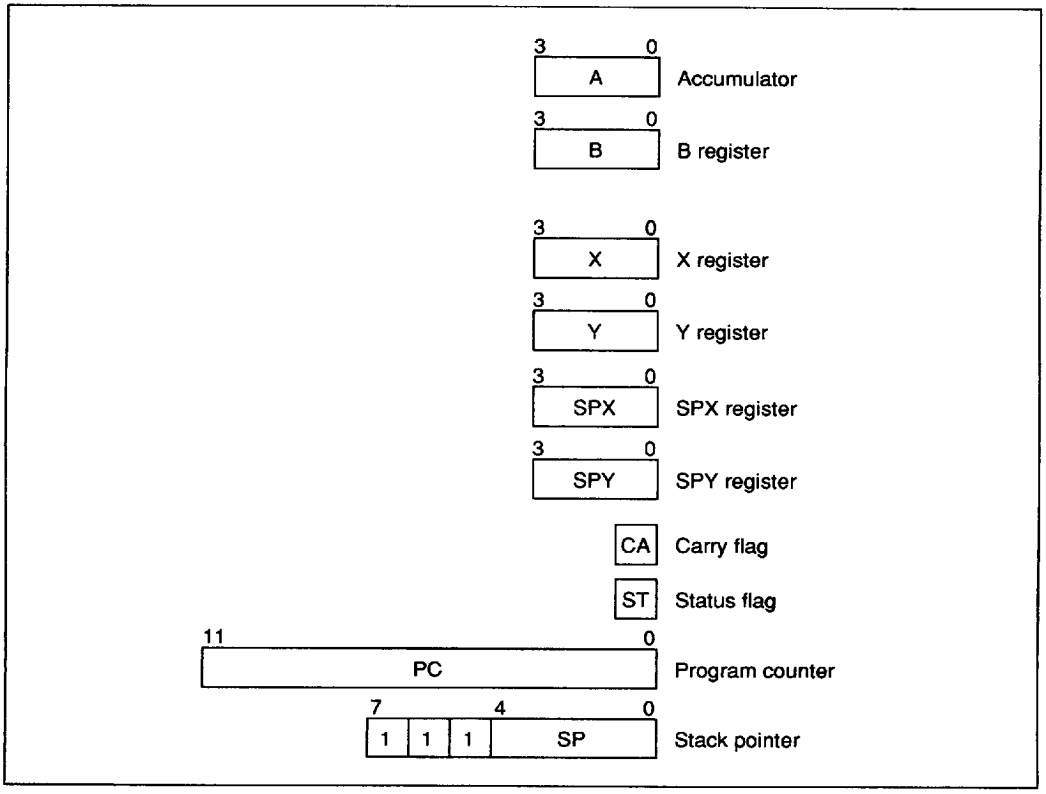


Figure 5 Registers and Flags

unchanged until the next arithmetic, compare, or bit test instruction is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction was either executed or not. During an interrupt, the status flag is pushed onto the stack and can be pulled from the stack only by the RTNI instruction.

Program Counter (PC): The program counter is a 12-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stack area (up to 8 levels).

The stack pointer is initialized to RAM address $FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is pulled from it. The stack can only be used up to 8 levels deep because the upper 3 bits of the stack pointer are fixed at 111.

Table 1 Initial Values After MCU Reset

Item			Initial Value by MCU Reset ($\overline{\text{RESET}}$ = 0)	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address
Status flag (ST)			1	Enable branching with conditional branch instructions
Stack pointer (SP)			$0FF	Stack level is 0
I/O pins, output registers	Standard	Without pull-up MOS	1	Enable input
		With pull-up MOS	1	Enable input
		CMOS	1	—
	High-voltage	Without pull-down MOS	0	Enable input
		With pull-down MOS	0	Enable input
Interrupt flags and mask		Interrupt enable flag (IE)	0	Inhibit all interrupts
		Interrupt request flag (IF)	0	No interrupt request
		Interrupt mask (IM)	1	Mask interrupt request
Mode registers		Port mode register (PMR)	000	See Port Mode Register section
		Serial mode register (SMR)	0000	See Serial Mode Register section
		Timer mode register A (TMA)	0000	See Timer Mode Register A section
		Timer mode register B (TMB)	0000	See Timer Mode Register B section
		Comparator mode register (CMR)	00	See Comparator Mode Register section
Comparator		Reference voltage select register (RSR)	0000	See Reference Voltage Select Register section
Timer/counters, serial interface		Prescaler	$000	—
		Timer counter A (TCA)	$00	—
		Timer counter B (TCB)	$00	—
		Timer load register B (TLR)	$00	—
		Octal counter	000	—

The stack pointer is initialized to $FF by either MCU reset or RSP bit reset by the REM/REMD instruction.

Reset

The MCU is reset by pulling the $\overline{\text{RESET}}$ pin low. At power-on or when cancelling the stop mode, the reset period must satisfy t_{RC} for the oscillator to stabilize. In other cases, at least two instruction cycles are required for the MCU to be reset.

Table 1 shows the components initialized by the MCU reset, and the status of each component.

Table 2 shows how registers recover from the stop mode.

Take note that the reset signal is not acknowledged immediately at power-on by the MCU but at the time the oscillator has stabilized, so during this period the statuses within the MCU and at the I/O pins are not defined.

Table 2 Initial Values After MCU Reset

Item		After MCU Reset to Recover from Stop Mode	After MCU Reset to Recover from Other Modes
Carry flag	(CA)	The contents of the items before MCU reset are not retained and must be initialized by software.	The contents of the items before MCU reset are not retained and must be initialized by software.
Accumulator	(A)		
B register	(B)		
X/SPX registers	(X/SPX)		
Y/SPY registers	(Y/SPY)		
Serial data register	(SR)		
RAM		The contents of RAM before MCU reset (just before the STOP instruction) are retained.	The contents of RAM before MCU reset are not retained and must be initialized by software.

Interrupts

Four interrupt sources are available on the MCU: an external request ($\overline{INT}$), timer/counters (timers A and B), and the serial interface. For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. An interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Operation: The interrupt control bits are mapped on $000 through $002 of the RAM. These bits are accessible by RAM bit manipulation instructions. The interrupt request flag (IF) cannot be set by software. At MCU reset initialization, the IE and IF are cleared to 0, and IM is set to 1.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 during this period, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. Also in the second cycle and third cycle, the carry flag, status flag, and program counter are pushed onto the stack. Included in the third cycle is the generation of the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

Table 3 Vector Addresses and Interrupt Priority

Reset/Interrupts	Priority	Vector Addresses
$\overline{RESET}$	—	$0000
$\overline{INT}$	1	$0002
Timer A	2	$0004
Timer B	3	$0006
Serial	4	$0008

Table 4 Interrupt Conditions

Interrupt Control Bits	$\overline{INT}$	Timer A	Timer B	Serial
IE	1	1	1	1
IFEX · $\overline{IMEX}$	1	0	0	0
IFTA · $\overline{IMTA}$	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	1

* indicates don't care

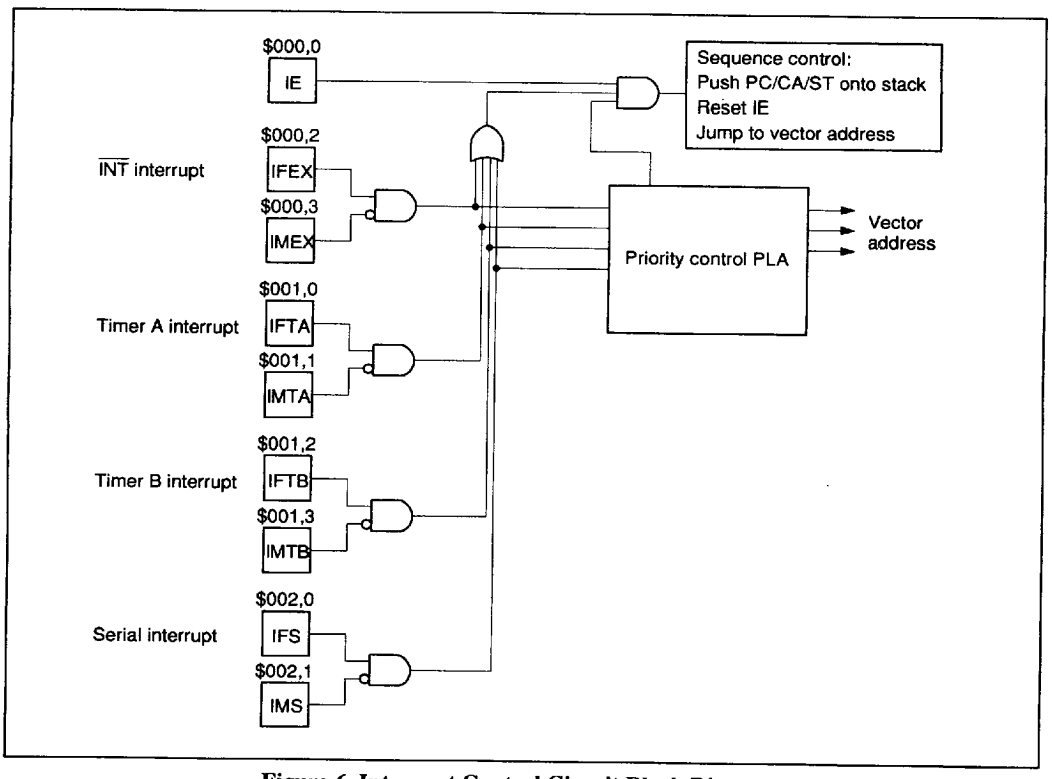


Figure 6 Interrupt Control Circuit Block Diagram

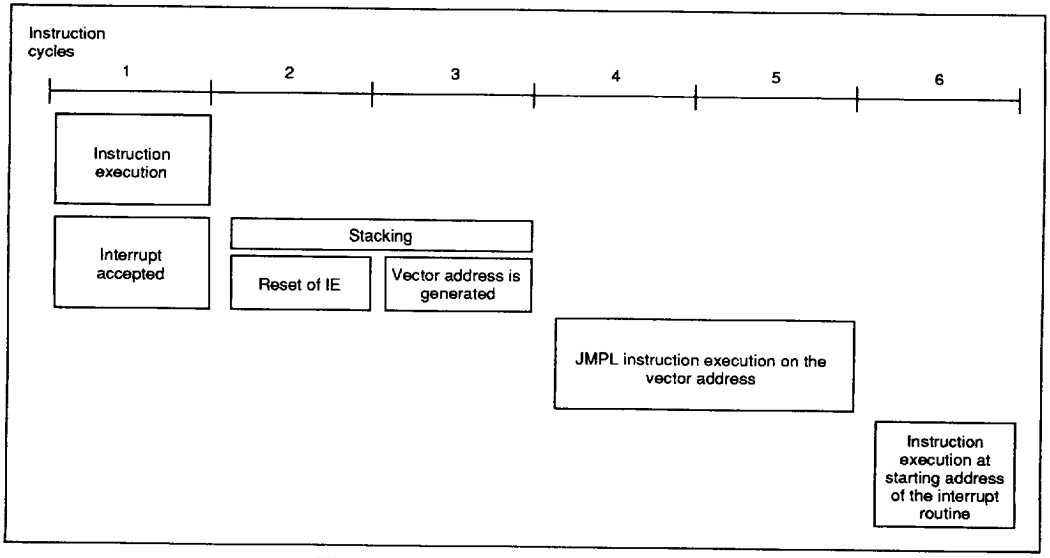


Figure 7 Interrupt Processing Sequence

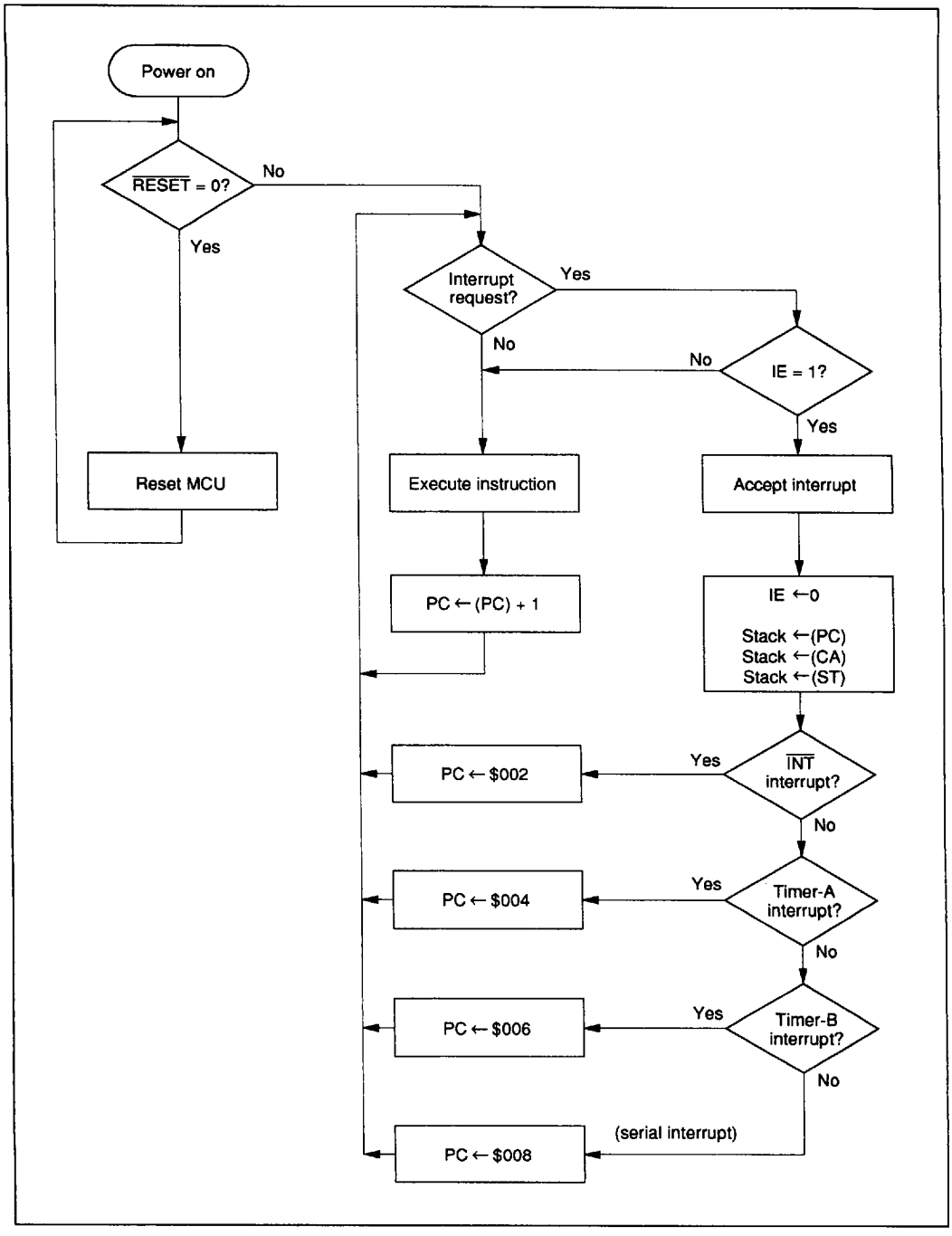


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag (table 5) enables or disables interrupt requests. It is reset by an interrupt and set by the RTNI instruction.

External Interrupt ($\overline{INT}$): The external interrupt request input ($\overline{INT}$) can be selected by the port mode register (PMR: $004). Setting bit 2 of PMR causes the $D_5/\overline{INT}$ pin to be used as $\overline{INT}$.

The external interrupt request flag IFEX (table 6) is set at the falling edge of $\overline{INT}$ input.

The $\overline{INT}$ input can be used as a clock signal input to timer B, which counts up at each falling edge of the $\overline{INT}$ input. When using $\overline{INT}$ as the timer B external event input, the external interrupt mask IMEX (table 7) has to be set so that the $\overline{INT}$ interrupt request will not be accepted.

External Interrupt Request Flag (IFEX: $000, Bit 2): The external interrupt request flag is set at the falling edge of the $\overline{INT}$ input.

External Interrupt Mask (IMEX: $000, Bit 3): The external interrupt mask (table 7) masks the external interrupt request.

Timer A Interrupt Request Flag (IFTA: $001, Bit 0): The timer A interrupt request flag (table 8) is set by the timer A overflow output.

Timer A Interrupt Mask (IMTA: $001, Bit 1): The timer A interrupt mask (table 9) prevents an interrupt request from being generated by the timer A interrupt request flag.

Table 5 Interrupt Enable Flag

IE	Interrupt Enable/Disable
0	Disabled
1	Enabled

Table 6 External Interrupt Request Flag

IFEX	Interrupt Request
0	No
1	Yes

Table 7 External Interrupt Mask

IMEX	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 8 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Table 9 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $001, Bit 2): The timer B interrupt request flag (table 10) is set by the overflow output of timer B.

Timer B Interrupt Mask (IMTB: $001, Bit 3): The timer B interrupt mask (table 11) prevents an interrupt request from being generated by the timer B interrupt request flag.

Serial Interrupt Request Flag (IFS: $002, Bit 0): The serial interrupt request flag (table 12) will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter.

Serial Interrupt Mask (IMS: $002, Bit 1): The serial interrupt mask (table 13) masks the interrupt request.

Port Mode Register (PMR: $004): The 3-bit write-only port mode register controls the $D_5/\overline{INT}$, D_7/SI, and D_8/SO pins as shown in table 14. The port mode register is initialized to $0 by MCU reset. Therefore these pins are initially used as ports. Note that if unusable bit 3 are set, the MCU may malfunction.

Table 10 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Table 11 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

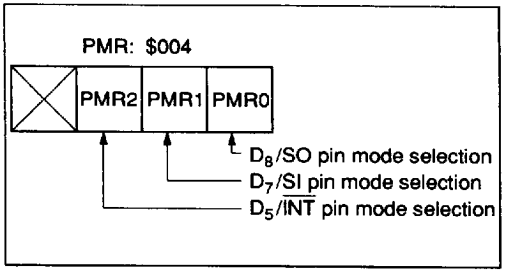
Table 12 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Table 13 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 14 Port Mode Register



PMR2	$D_5/\overline{INT}$ Pin
0	Used as D_5 port input/output pin
1	Used as $\overline{INT}$ input pin

PMR1	D_7/SI Pin
0	Used as D_7 port input/output pin
1	Used as SI input pin

PMR0	D_8/SO Pin
0	Used as D_8 port input/output pin
1	Used as SO output pin

Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 15). Figure 9 shows a mode transition diagram of these modes.

Standby Mode: Executing the SBY instruction places the MCU into standby mode. In standby mode, the oscillator circuit, interrupts, timer/counters, and serial interface remain active. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 15 Low-Power Dissipation Mode Function

Low-Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Registers, Flags	Interrupt Function
Standby mode	SBY instruction	Active	Stop	Retained	Active
Stop mode	STOP instruction	Stop	Stop	Reset*1	Stop

Table 15 Low-Power Dissipation Mode Function (cont)

Low-Power Dissipation Mode	RAM	Input/ Output Pins	Timer/ Counters, Serial Interface	Comparator	Cancellation Method
Standby mode	Retained	Retained*2	Active	Stop	$\overline{\text{RESET}}$ input, interrupt request
Stop mode	Retained	High impedance*3	Stop	Stop	$\overline{\text{RESET}}$ input

Notes: 1. The MCU recovers from stop mode by $\overline{\text{RESET}}$ input. Refer to table 1 for the contents of the flags and registers.
2. If an I/O circuit is active, an I/O current may flow, depending on the state of the I/O pin in standby mode. This current is in addition to the current dissipation in standby mode.
3. The voltage of high breakdown voltage pins with pull-down MOS are pulled down.

The standby mode may be cancelled by enabling $\overline{\text{RESET}}$ or by asserting an interrupt request. In the former case, the MCU is reset. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction. After this instruction is completed and if the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 10 shows the flowchart of the standby mode.

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and all functions of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 11, the $\overline{\text{RESET}}$ input must be applied for at least t_{RC} for the oscillation to stabilize. (Refer to the AC Characteristics table.) After stop mode is cancelled, the RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, X/SPX and Y/SPY registers, carry flag, and serial data register will not retain their contents.

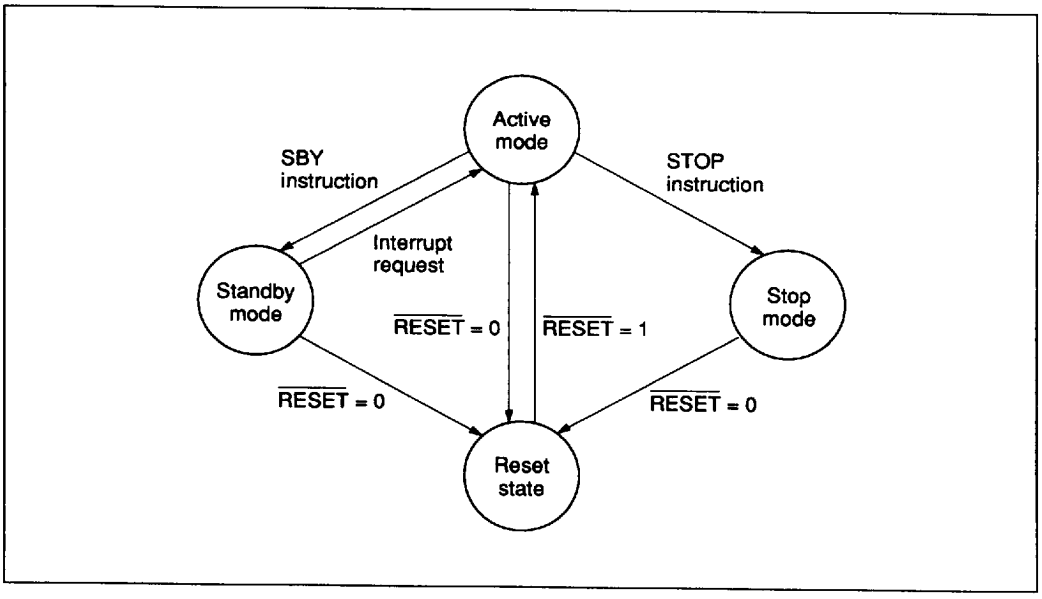


Figure 9 MCU Operation Mode Transition

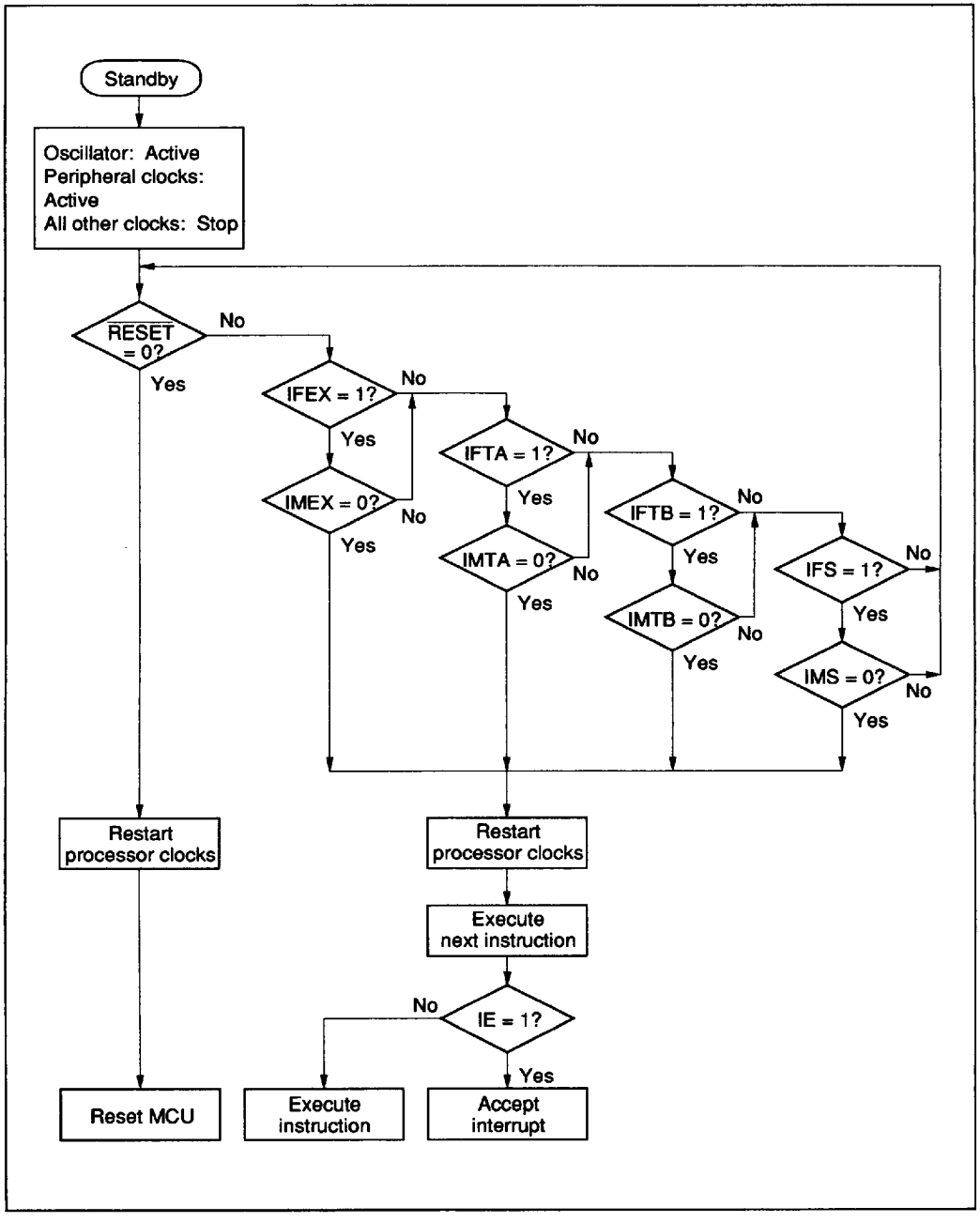


Figure 10 MCU Operating Flowchart in Standby Mode

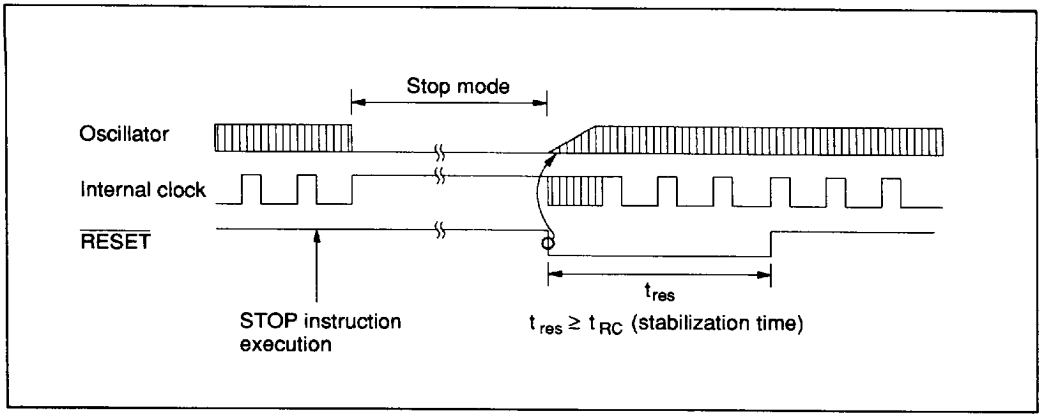


Figure 11 Timing of Stop Mode Cancellation

Internal Oscillator Circuit

Figure 12 shows a block diagram of the internal oscillator circuit. Through mask options, either a ceramic oscillator or resistor can be selected as the oscillator type and connected to OSC_1 and OSC_2. See figure 13 for the layout of the ceramic oscillator . For other cases, an external clock operation is available.

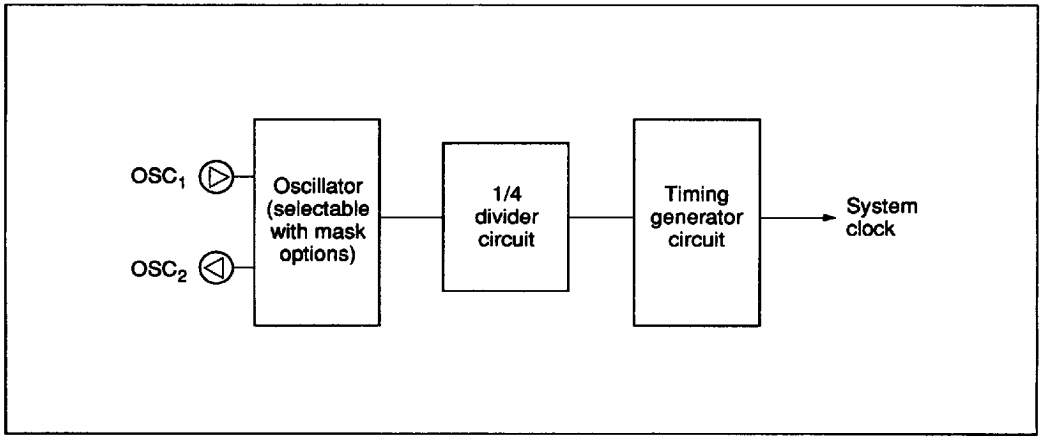
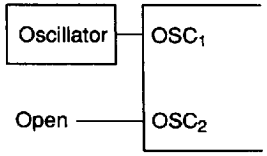
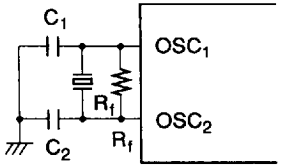
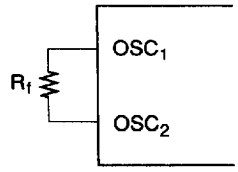


Figure 12 Internal Oscillator Circuit

Table 16 Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator		Ceramic oscillator: CSA4.00MG (MURATA) $C_1 = C_2$: 30 pF ±20% R_f: 1 MΩ ±20% Ceramic oscillator CSB1000J (MURATA) $C_1 = C_2$: 220 pF ±20% R_f: 1 MΩ ±20%
Resistor		R_f: 20 kΩ ±1%

Notes: The circuit parameters listed above are dependent on the ceramic oscillator and the floating capacitance when designing the board. In employing the resonator, consult with the ceramic oscillator manufacturer to determine the circuit parameters.

The wiring between OSC_1, OSC_2, and the elements should be as short as possible without crossing over other wires. Refer to the layout of the ceramic oscillator in figure 13.

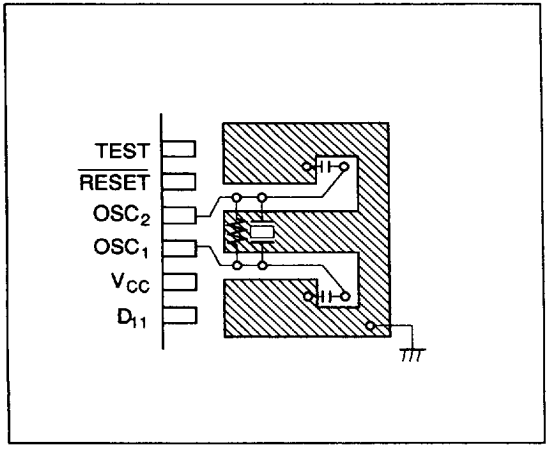


Figure 13 Layout of the Ceramic Oscillator

Input/Output

The MCU has 7 standard I/O pins, 14 high-voltage I/O pins and 1 high-voltage input-only pin.

As for the circuit types and mask options, see tables 18 and 19.

To input to these ports, the pin types and output level setting must be selected as listed in table 17.

Output Circuit Operation of with Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 14 is used to shorten the rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on (in figure 14) and shorten the rise time. The write pulse keeps PMOS on for two-eighths of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in stop mode, MOSs (A), (B), and (C) turn off. When the $\overline{HLT}$ signal is 1, the pins' states are maintained.

D Port: The D port has 14 discrete I/O pins, each of which can be addressed independently. The D port can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions.

Pins D_5 to D_{11} are multiplexed with pins $\overline{INT}$, $\overline{SCK}$, SI, SO, V_{ref}, $COMP_0$, and $COMP_1$, respectively. Setting, resetting, or testing non-existing ports results in invalid data.

R Ports: The R ports are I/O pins that are accessed in 4-bit units. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. Writing into non-existing ports will not affect the MCU, however, the values read from the non-existing ports cannot be guaranteed.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

- If without pull-down MOS (PMOS open drain) is selected for high-voltage pins, connect to V_{CC} on the printed circuit board.
- If without pull-up MOS is selected for standard pins, connect to GND on the printed circuit board.

Table 17 Data Input from Common Input/Output Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard pins	CMOS (C)	No	—
	Without pull-up MOS (NMOS open drain) (B)	Yes	1
	With pull-up MOS (A)	Yes	1
High voltage pins	Without pull-down MOS (PMOS open drain) (D)	Yes	0
	With pull-down MOS (E)	Yes	0

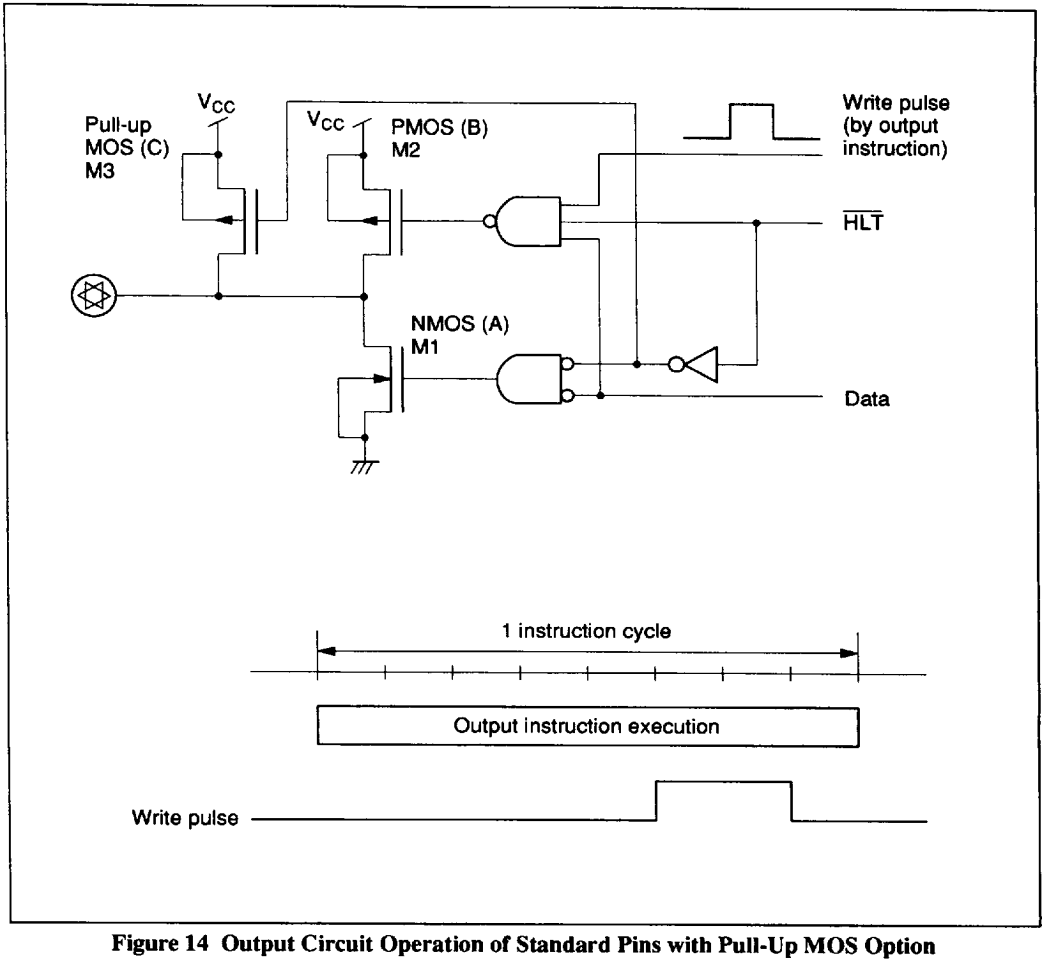
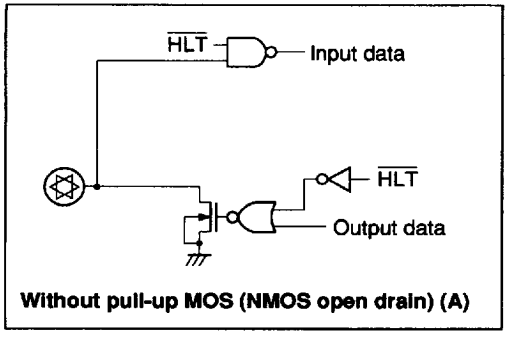


Figure 14 Output Circuit Operation of Standard Pins with Pull-Up MOS Option

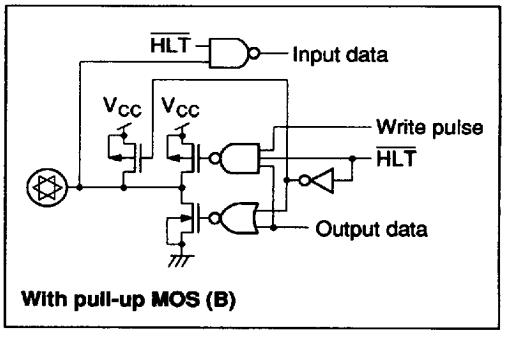
Table 18 I/O Pin Circuit Types

Standard Pins

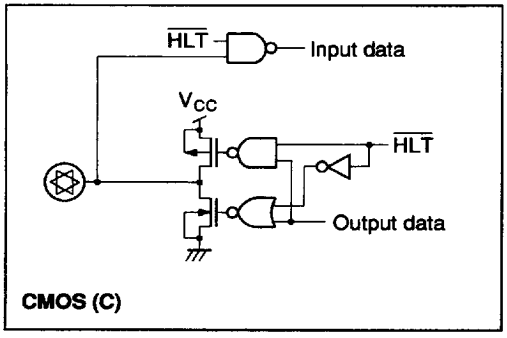
I/O Common Pins (D_5–D_{11})



Without pull-up MOS (NMOS open drain) (A)

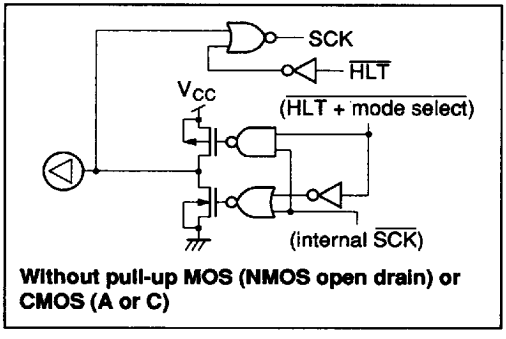


With pull-up MOS (B)

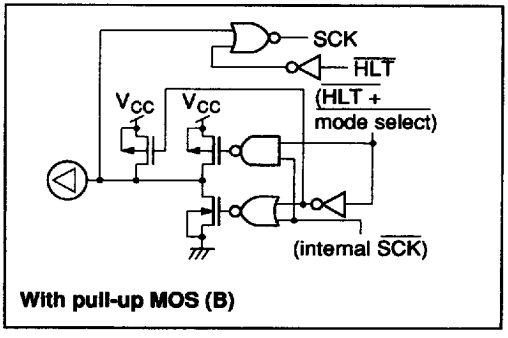


CMOS (C)

I/O Common Pins ($\overline{SCK}$ (output mode))



Without pull-up MOS (NMOS open drain) or CMOS (A or C)



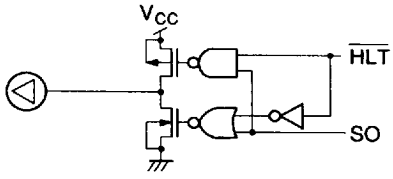
With pull-up MOS (B)

Note: When selecting ports D_5, D_6, and D_7 as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled even if selecting mask option B (with pull-up MOS).

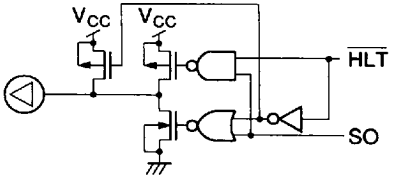
Table 18 I/O Pin Circuit Types (cont)

Standard Pins

Output Pins (SO)

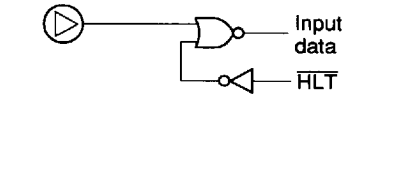


Without pull-up MOS (NMOS open drain) or CMOS (A or C)

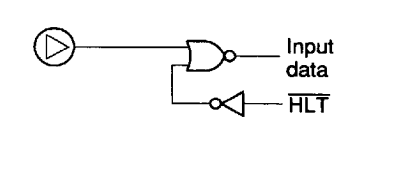


With pull-up MOS (B)

Input Pins ($\overline{INT}$, SI, $\overline{SCK}$ (input mode)

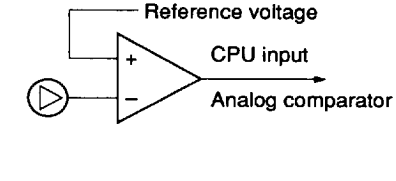


Without pull-up MOS (NMOS open drain) or CMOS (A or C)



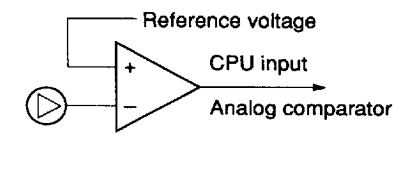
With pull-up MOS (B)

Input pins ($COMP_0$, $COMP_1$)



Without pull-up MOS (NMOS open drain) or CMOS (A or C)

Input pins ($COMP_0$, $COMP_1$)

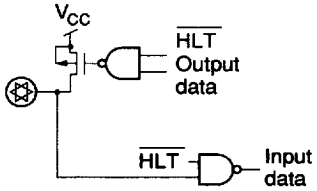
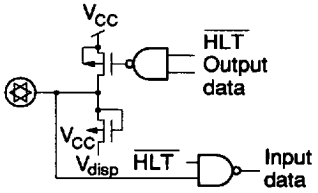


With pull-up MOS (B)

Note: When selecting ports D_5, D_6, and D_7 as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled even if selecting mask option B (with pull-up MOS).

Table 18 I/O Pin Circuit Types (cont)

High-Voltage I/O Pins (D_0–D_4, D_{12}, R1, R2)

	Without Pull-Down MOS (PMOS open drain) (D)	With Pull-Down MOS (E)
I/O Common Pins		

High-Voltage Input Pin (D_{13})

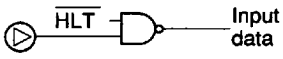
Input Pins	

Table 19 Optional I/O Pin Circuit Types

Product Type	A	B	C	D	E	
Mask ROM HD404272 HD40L4272	Optional			Optional		Selectable as input port or V_{disp}
Pin	Standard I/O pins			High-voltage I/O pins (except for D_{13})		D_{13} pin

Timers

The MCU contains a prescaler and two timer/counters (timers A and B) as shown in figure 15. The prescaler is an 11-bit counter, timer A is an 8-bit free-running or watchdog timer, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The system clock signal is input to the prescaler. At MCU reset, the prescaler is initialized to $000 and starts dividing the system clock frequency.

The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR).

Timer A Operation

Timer A's function is selected via the mask option.

When timer A is used as a free-running timer, it counts up every input clock signal after timer A has been initialized to $000 by MCU reset. When the next clock signal is input after timer A counts up to $0FF, timer A is set to $000 again, and generates an overflow output. This sets the timer A interrupt request flag (IFTA: $001, bit 0) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal. The clock signals input to timer A are selected by timer mode register A (TMA: $008).

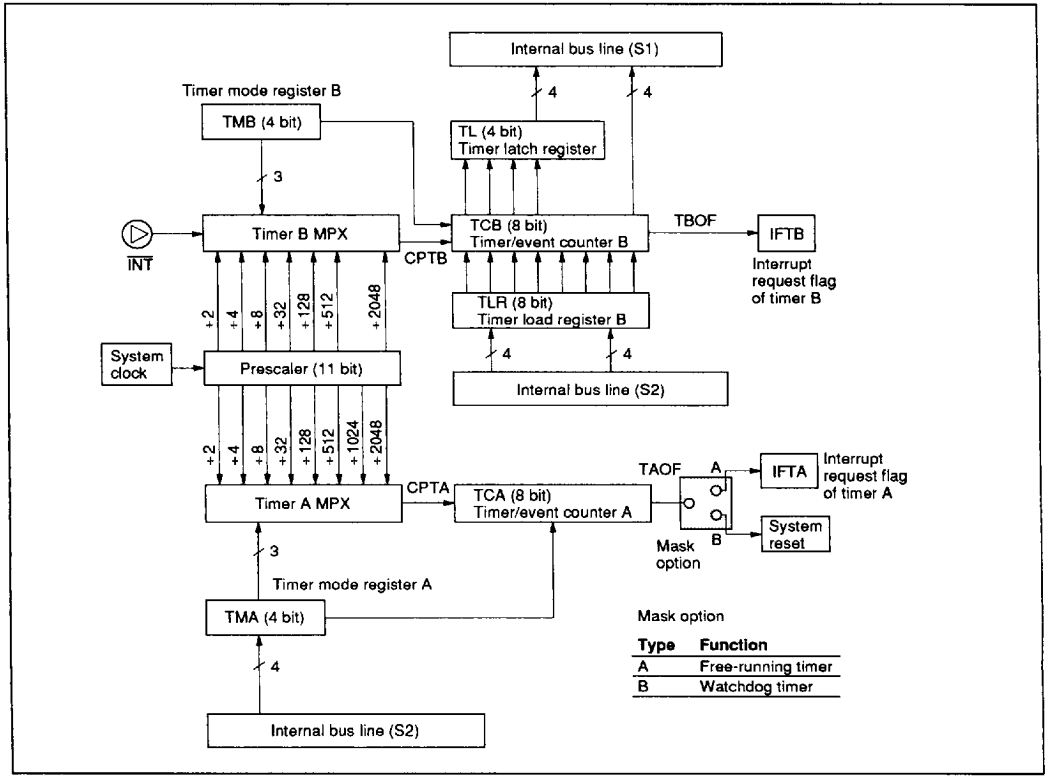


Figure 15 Timer/Counters Block Diagram

Note that when timer A is used as a free-running timer, if setting bit 3 of timer mode resister A may cause the MCU to be malfunction.

When timer A is used as a watchdog timer, the input clock is specified as 1/2048 output divided by the prescaler. The watchdog timer is initialized to $000 at MCU reset, then counts up every input clock signal. If a clock signal is applied after the timer becomes $0FF, an overflow is generated and the MCU is reset.

After reset, the MCU re-executes the program from the beginning. The program must set bit 3 of timer mode register A to reset timer counter A.

Timer B Operation: Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $D_5/\overline{INT}$ as $\overline{INT}$ and set the external interrupt mask (IMEX) to prevent an external interrupt request from occurring.

Timer B is initialized by software according to the data written in timer load register B. Timer B counts up at every input clock signal. When the next clock signal is input after timer B is set to $FF, timer B will generate an overflow output. Then, if the auto-reload function is selected, timer B is initialized to the value of timer load register B. If it is not selected, timer B goes back to $000. The timer B interrupt request flag (IFTB: $001, bit 2) will hold the overflow output.

Timer Mode Register A (TMA: $008): Four-bit write-only timer mode register A selects the timer function for timer A and the prescaler divide ratio of timer A's clock input as shown in table 20. Timer mode register A is initialized to $0 by MCU reset.

Table 20 Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 21 Timer Mode Register B

TMB3	Auto-Reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT}$ (external event input)

Timer Mode Register B (TMB: $009): Four-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal as shown in table 21. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Timer B should be initialized by writing data into timer load register B after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 16.

Timer B Load Register (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B) (figure 2).

The timer/event counter can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

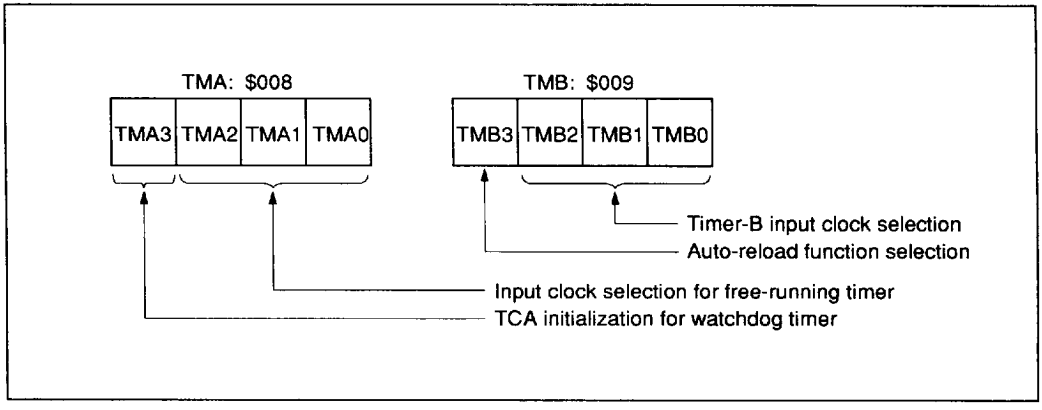


Figure 16 Mode Registers Configuration and Function

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, serial mode register, octal counter, and multiplexer, as illustrated in figure 17. Pin $D_6/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to 000. The counter starts to count at the falling edge of the transmit clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the octal counter is reset to 000 after eight transmit clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: $005): The 4-bit write-only serial mode register controls the $D_6/\overline{SCK}$, prescaler divide ratio, and transmit clock source as shown in table 22.

A write signal sent to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from using the transmit clock, and it also resets the octal counter to 000 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request

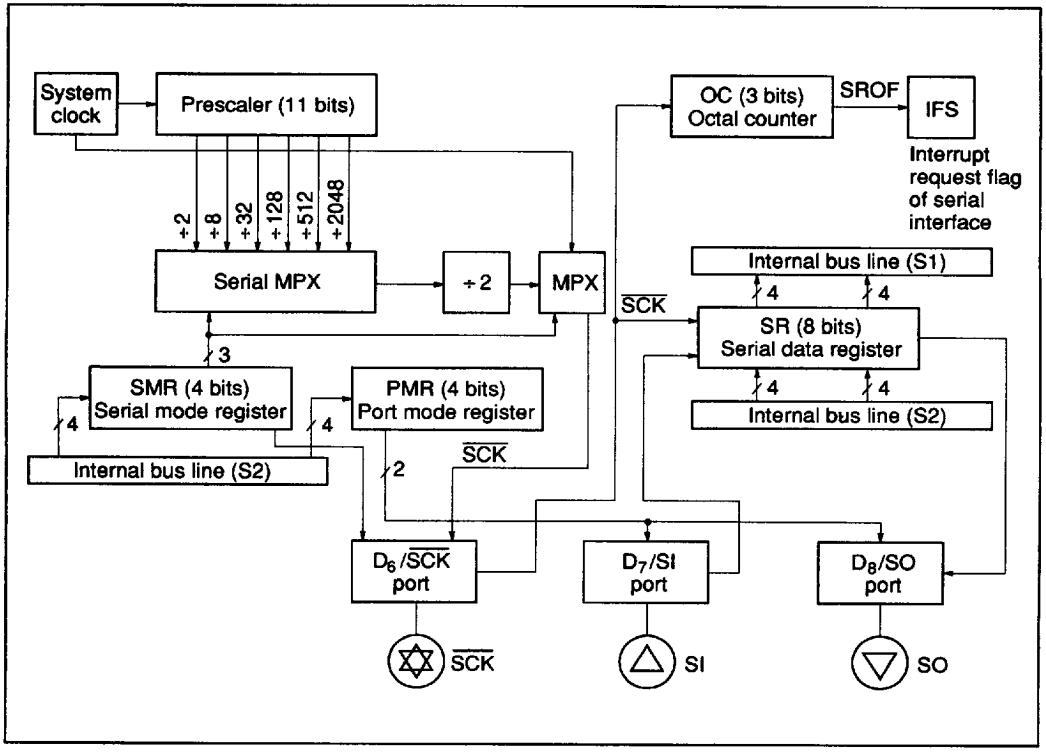


Figure 17 Serial Interface Block Diagram

flag.
The contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it is necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

Serial Data Register (SRL: $006, SRU: $007): The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data will be input from the SI pin to the serial data register, to LSB first, synchronously with the rising edge of the transmit clock. Figure 18 shows the I/O timing chart for the transmit clock signal and the data.

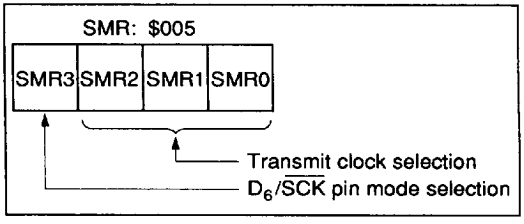
The read/write operations of the serial data register should be performed after the completion of data transmission/reception. Otherwise, the data may not be guaranteed.

Selecting and Changing the Operation Mode: Table 23 shows the serial interface operation modes which are determined by a combination of the values in the port mode register and in the serial mode register. Initialize the serial interface by the write signal to the serial mode register when the operation mode is changed.

Operating State of the Serial Interface: The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 19.

Table 22 Serial Mode Register

SMR3	$D_6/\overline{SCK}$
0	Used as D_6 port input/output pin
1	Used as $\overline{SCK}$ input/output pin



			Transmit Clock			
SMR2	SMR1	SMR0	$D_6/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
1	1	1	$\overline{SCK}$ input	External clock	—	—

Table 23 Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

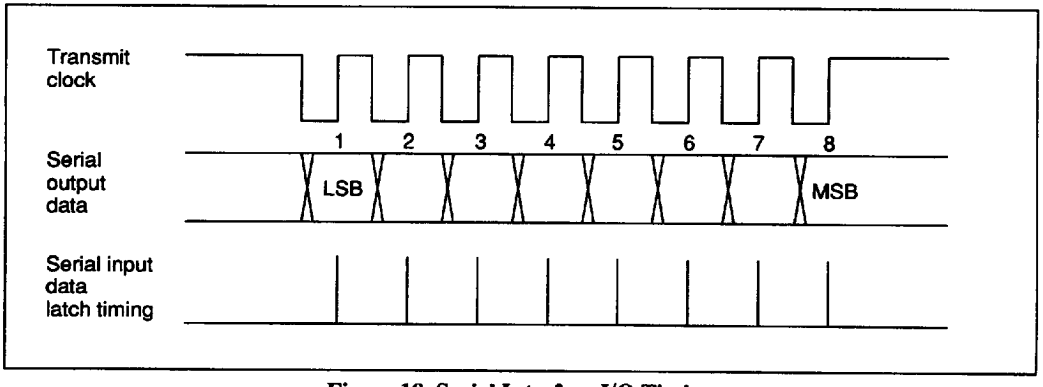


Figure 18 Serial Interface I/O Timing

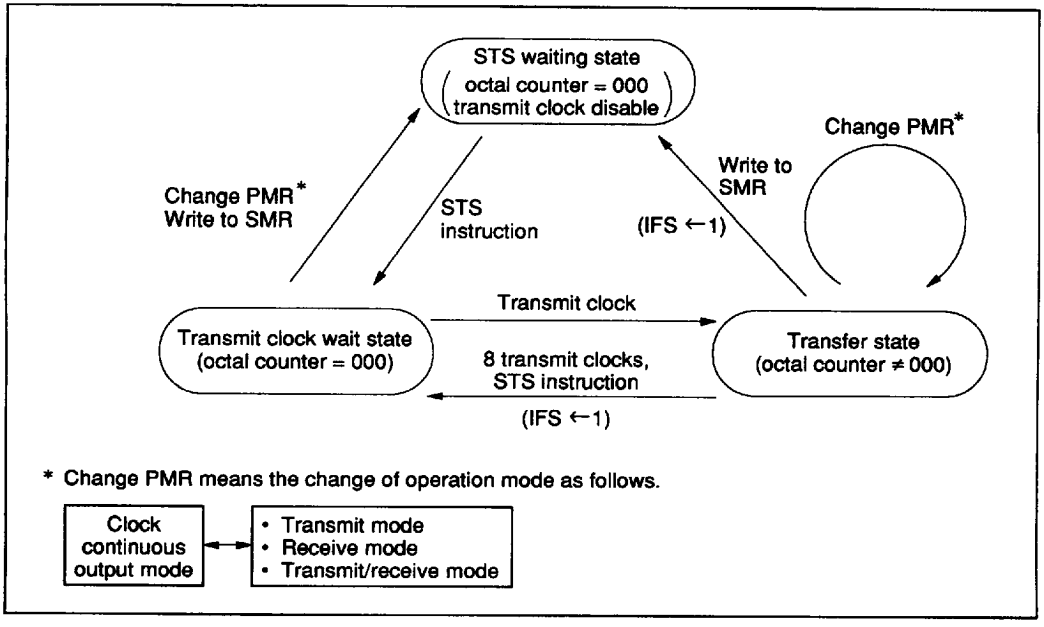


Figure 19 Serial Interface Operation States

The STS waiting state is the initialization of the serial interface. In this state, the serial interface does not operate even if the transmit clock is applied.

If the STS instruction is executed, the serial interface shifts to the transmit clock wait state. In this state the falling edge of the first transmit clock causes the serial interface to shift to the transfer state, in which the octal counter counts up and the serial data register shifts simultaneously. If clock continuous output mode is selected, however, the serial interface stays in the transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or after the execution of the STS instruction, so that the serial interface is returned to the transmit clock wait state and the serial interrupt request flag is set simultaneously.

When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

Transmit Clock Error Detection: The serial interface functions abnormally when the transmit clock is disturbed by external noise. In this case, transmit clock errors can be detected by the procedure shown in figure 20.

If more than 8 transmit clocks are applied in the transmit clock wait state, the state of the serial interface shifts in the following sequence: transfer state, transmit clock wait state, and transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

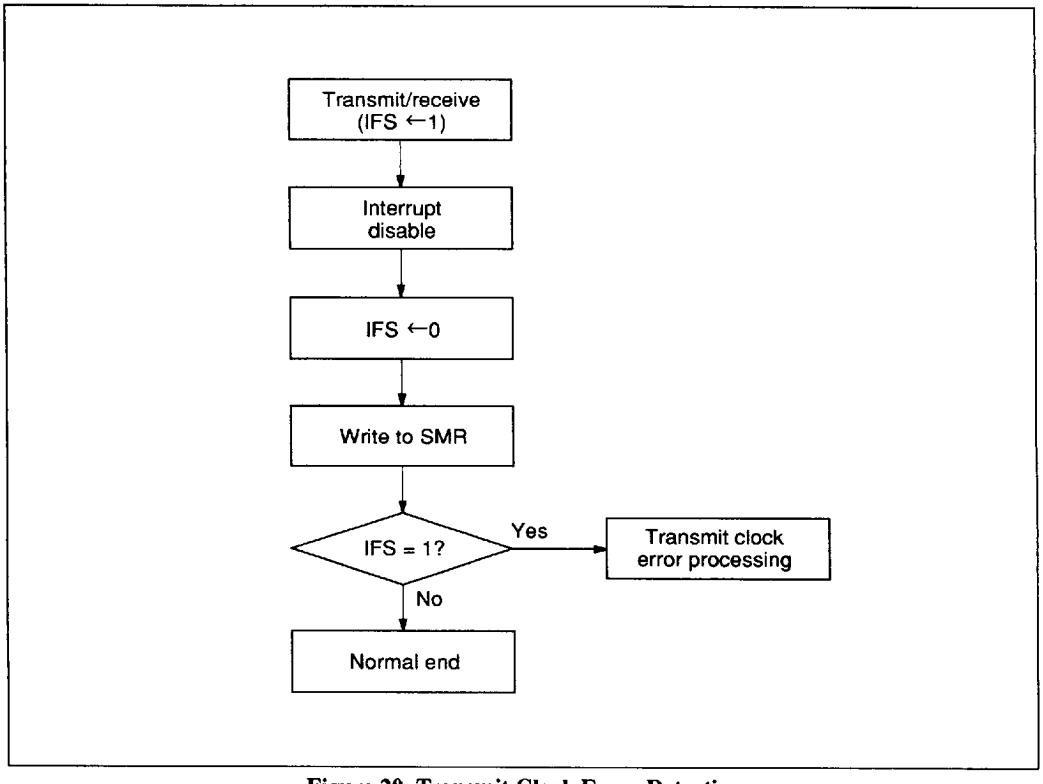


Figure 20 Transmit Clock Error Detection

Comparator

The MCU has two-channel comparators that compare input data with the reference voltage.

Figure 21 shows the comparator block diagram. The comparator block consists of two analog comparators, the comparator mode register (CMR) which selects the comparator operation, the reference voltage select register (RSR) which selects the reference voltage, a ladder resistance which generates the internal reference voltage, and peripheral circuits.

For the $COMP_0$ input, either the external reference voltage or the internal reference voltage, which is generated by dividing V_{CC} with the internal ladder resistance, can be selected as the reference voltage. For the $COMP_1$ input, only the external reference voltage is used; the internal reference voltage cannot be selected.

The power consumption increases after the comparator operation is selected by CMR, because direct current is constantly supplied to assure the analog comparator characteristics. To reduce the power consumption during comparator use, the comparator operation should not be selected by software except when analog comparison is required. In this case, a maximum of two instruction cycles are required after the comparator operation is selected in order for the analog comparator to stabilize and operate correctly. Therefore, the comparison result should be read at least two instruction cycles after the comparator operation is selected.

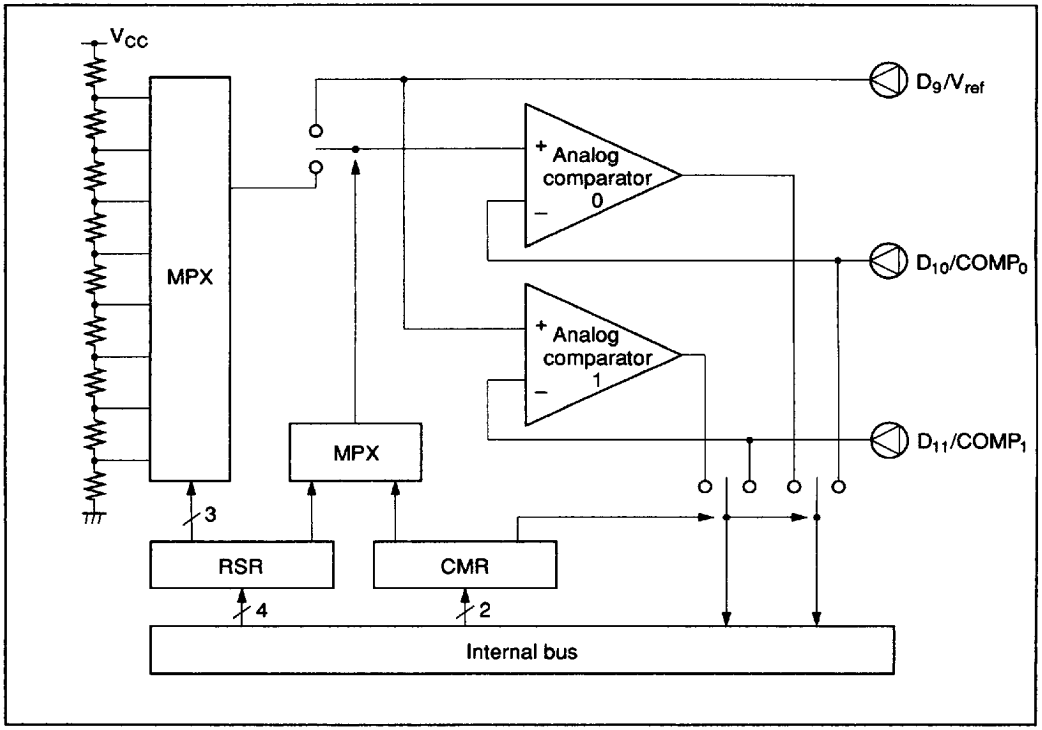


Figure 21 Comparator Block Diagram

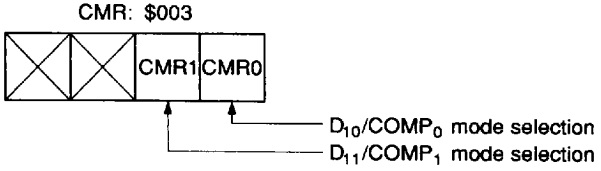
The comparison result is obtained by executing the TD or TDD instruction. When the analog input voltage is higher than the reference voltage, a 1 is read as input data from the comparator. The comparator automatically stops operating in standby and stop modes.

Comparator Mode Register (CMR: $003): This 2-bit register selects the $D_{10}/COMP_0$ and $D_{11}/COMP_1$ functions.

CMR is only affected by the bit manipulation instructions (set by the SEM or SEMD instruction and reset by the REM or REMD instruction). It is initialized to $0 by MCU reset. Therefore, it becomes input/output mode after MCU reset.

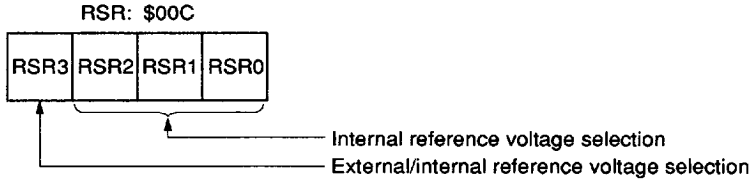
Reference Voltage Select Register (RSR: $00C): This 4-bit read/write register selects the $COMP_0$ reference voltage for the analog comparator from the eight-level internal voltage or the external voltage. It is initialized to $0 by MCU reset.

Notes for Use: When using the analog comparator, carefully program the data output instruction and data input into the port next to $COMP_0$ and $COMP_1$ to assure precise and stabilized comparator operation.



CMR		Mode Selection	
Bit 1	Bit 0	$D_{10}/COMP_0$	$D_{11}/COMP_1$
0	0	D_{10}	D_{11}
0	1	$COMP_0$	D_{11}
1	0	D_{10}	$COMP_1$
1	1	$COMP_0$	$COMP_1$

Figure 22 Comparator Mode Register



RSR				
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Reference Voltage**
0	0	0	0	1/11 V_{CC}
0	0	0	1	2/11 V_{CC}
0	0	1	0	3/11 V_{CC}
0	0	1	1	4/11 V_{CC}
0	1	0	0	5/11 V_{CC}
0	1	0	1	6/11 V_{CC}
0	1	1	0	7/11 V_{CC}
0	1	1	1	8/11 V_{CC}
1	—	—	—	External V_{ref} (D_9/V_{ref})

— indicates 0 or 1

Figure 23 Reference Voltage Select Register

Addressing Modes

RAM Addressing Modes

As shown in figure 24, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The contents (8 bits) of the X and Y registers are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, the first word contains the opcode, the second word (10 bits) is used as the RAM address.

Memory Register Addressing: The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 25.

Direct Addressing Mode: The program can branch to any address in ROM memory by executing the JMPL, BRL, or CALL instruction. These instructions replace the 12 program counter bits (PC_{11} to PC_0) with 12-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. The program can branch to an address on the current page by executing the BR instruction. This instruction replaces the lower eight bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

When the BR instruction falls on a page boundary (256n + 255), executing the BR instruction transfers the PC contents to the next page (figure 26) according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000–$003F. When the CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order six bits (PC_{11} to PC_6).

Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 27). When bit 8 of the ROM data is 1 (RO_8 = 1), 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1 (RO_9 = 1), 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1 (RO_8 = 1, RO_9 = 1), ROM data are written into the accumulator, B register, and R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

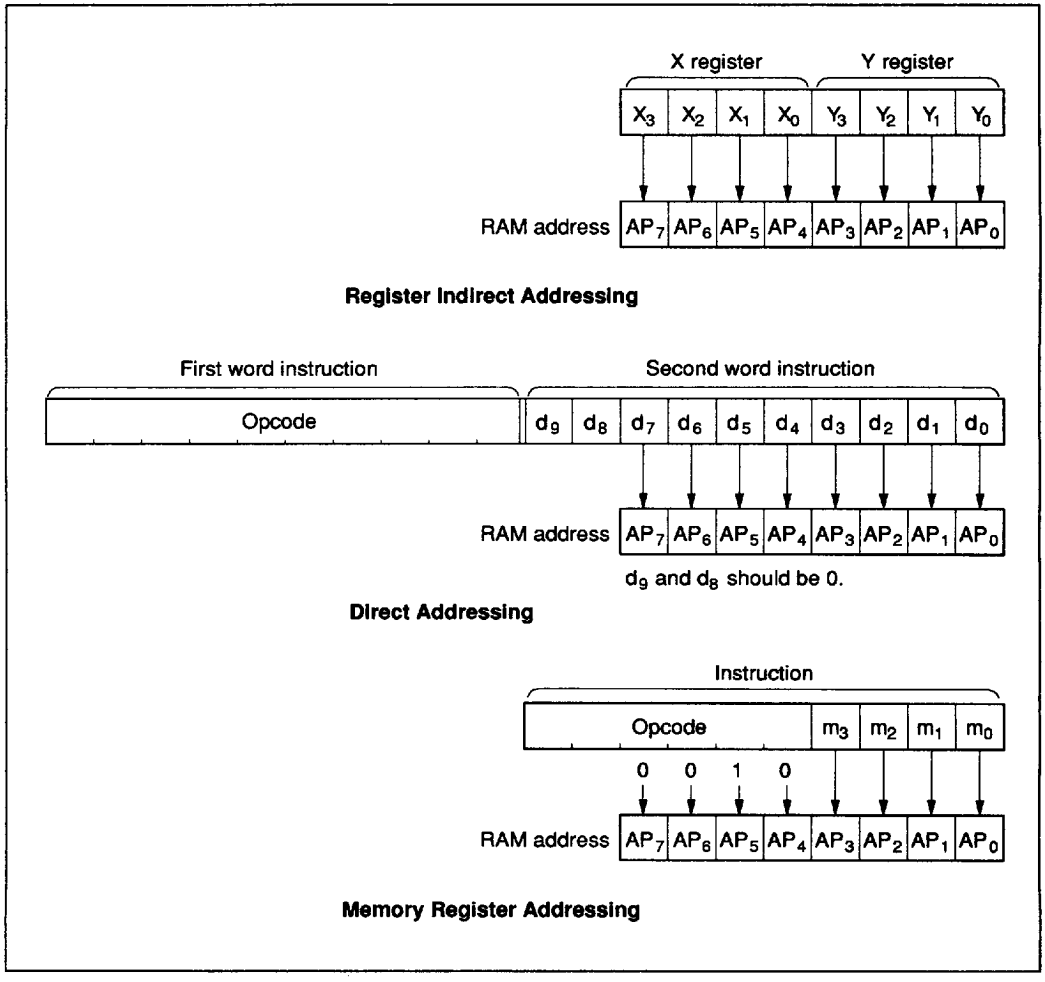


Figure 24 RAM Addressing Modes

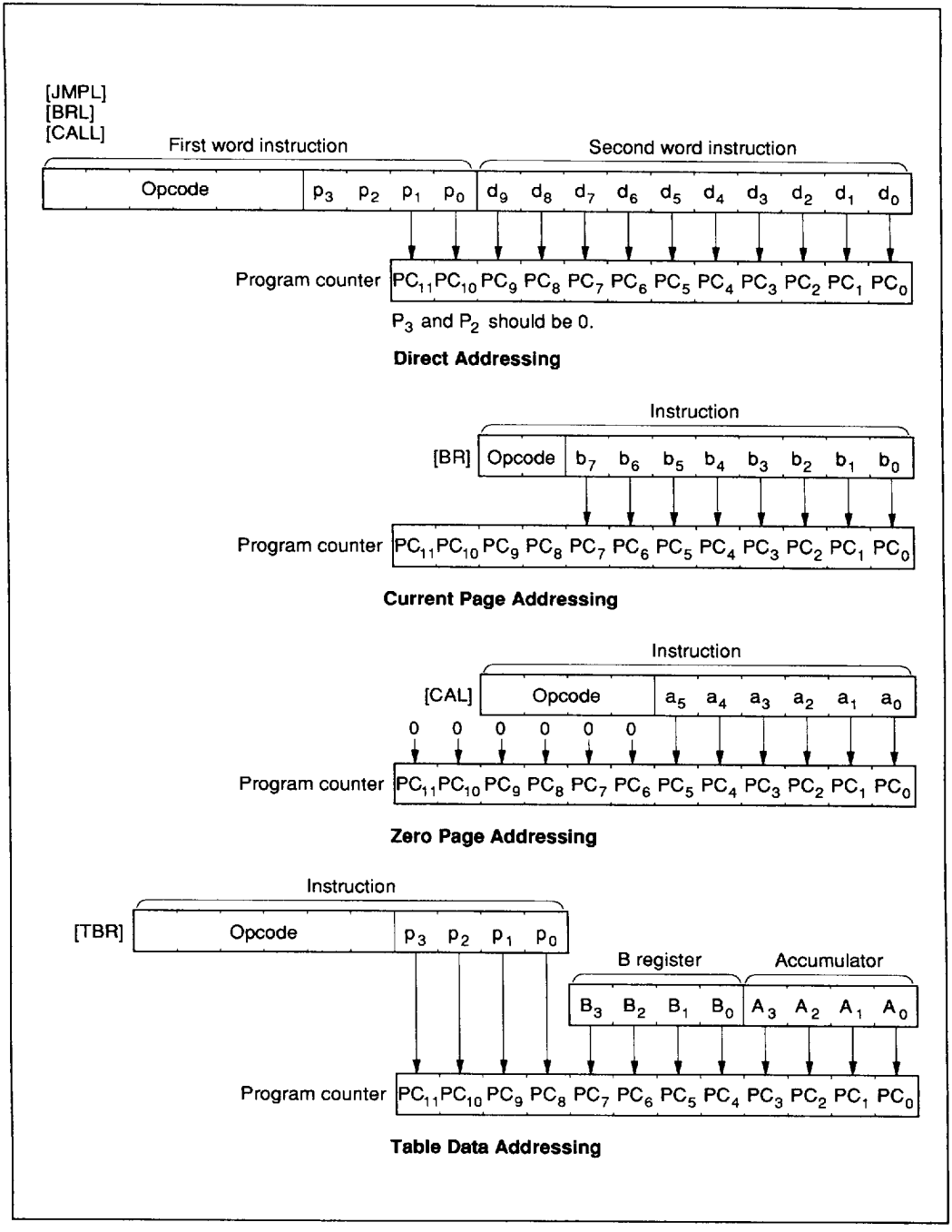


Figure 25 ROM Addressing Modes

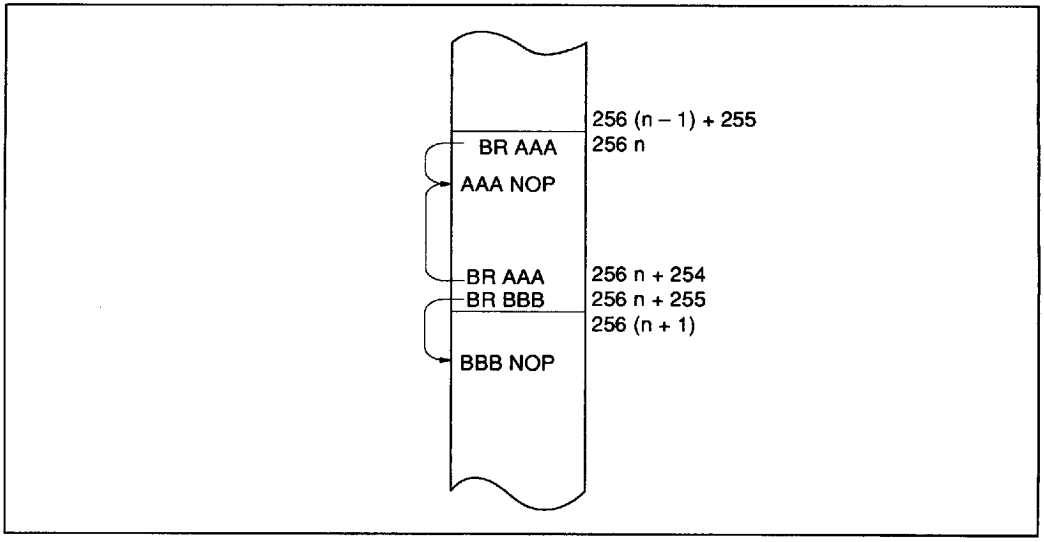


Figure 26 BR Instruction Branch Destination on a Page Boundary

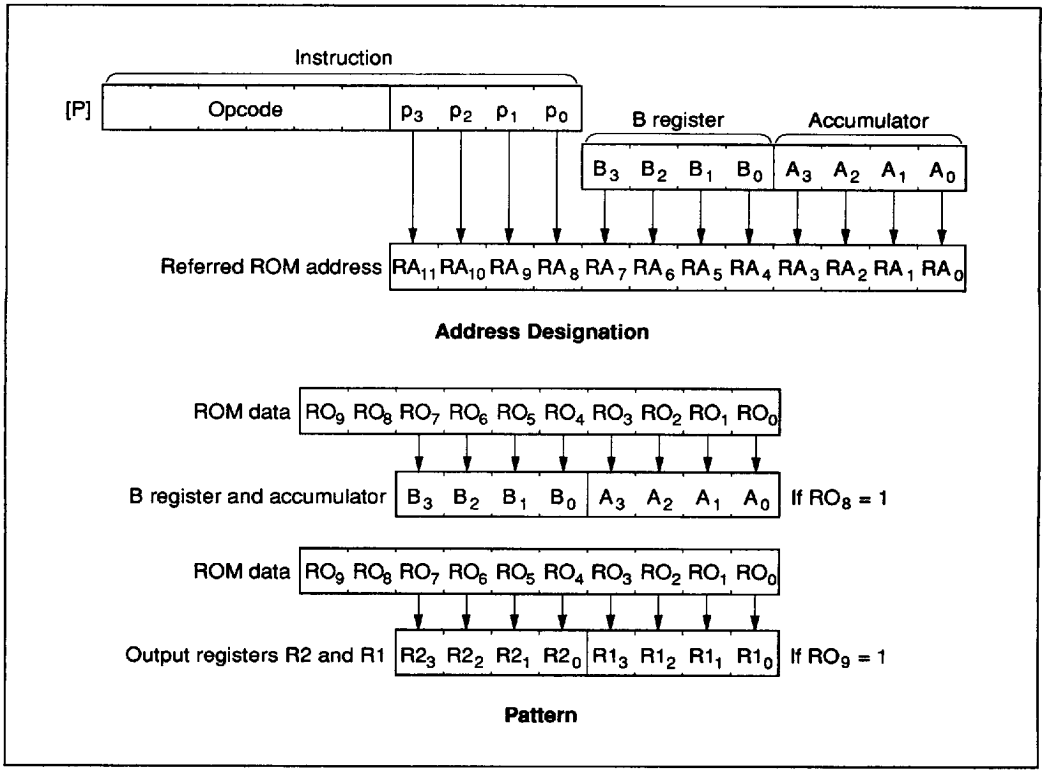


Figure 27 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
		V_{CC} – 45 to V_{CC} + 0.3	V	2
Total permissible input current	ΣI_o	100	mA	3
Total permissible output current	$-\Sigma I_o$	30	mA	4
Maximum input current	I_o	4	mA	5, 6
Maximum output current	$-I_o$	4	mA	6, 7
		8	mA	7, 8
		30	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristic tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

All voltages are with respect to GND.

1. Standard pins
2. High-voltage pins
3. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
4. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
5. The maximum input current is the maximum currents flowing from any I/O pins to GND.
6. Applies to D_5–D_{11}.
7. The maximum output current is the maximum currents flowing from V_{CC} to any I/O pins.
8. Applies to $R1_0$–$R1_3$, $R2_0$–$R2_3$.
9. Applies to D_0–D_4, D_{12}.

Electrical Characteristics

DC Characteristics (HD404272: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD40L4272: V_{CC} = 2.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified)

Preliminary Specifications
Subject to change

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{INT}$, SCK	0.9 V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	HD404272	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V	HD40L4272	
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{INT}$, SCK	–0.3	—	0.2 V_{CC}	V		
		SI	–0.3	—	0.3 V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	HD404272	
			–0.3	—	0.3	V	HD40L4272	
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 1.0	—	—	V	HD404272: $-I_{OH}$ = 1.0 mA	
			V_{CC} – 0.5	—	—	V	HD40L4272: $-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 0.5 mA	
Input/output leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$, SI, SO OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	3.5	mA	HD404272: V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
			—	—	1.0	mA	HD40L4272: V_{CC} = 3 V, f_{OSC} = 1 MHz	2, 5
	I_{CMP}	V_{CC}	—	—	5.5	mA	HD404272: V_{CC} = 5 V, f_{OSC} = 4 MHz, comparators active	3, 5
			—	—	1.6	mA	HD40L4272: V_{CC} = 3 V, f_{OSC} = 1 MHz, comparator active	3, 5

Notes on next page.

DC Characteristics (HD404272: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD40L4272: V_{CC} = 2.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C unless otherwise specified) (cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	1.7	mA	HD404272: V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
			—	—	0.5	mA	HD40L4272: V_{CC} = 3 V, f_{OSC} = 1 MHz	4, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in(\overline{RESET})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in(TEST)}$ = 0 V to 0.3 V	6
Stop mode retain voltage	V_{STOP}	V_{CC}	2	—	—	V		
Input high voltage	V_{IHA}	$COMP_0$ $COMP_1$	VC_{ref} + 0.1	—	—	V		
Input low voltage	V_{ILA}	$COMP_0$ $COMP_1$	—	—	VC_{ref} – 0.1	V		
Comparator input reference voltage scope	VC_{ref}	V_{ref}	—	—	V_{CC} – 1.2	V		
Deviation of internal reference voltage	V_{OFS}	—	–0.1	—	0.1	V	V_{CC} = 4.5 V to 6.0 V	7

Notes: 1. Excluding output buffer current and pull-up MOS current.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test condition: MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   D_0 to D_4, D_{12}, D_{13}, R1, R2 at V_{disp} voltage
   D_5 to D_{11} at V_{CC}

3. I_{CMP} is the source current when no I/O current is flowing while the comparator is in operation.
   Test condition: MCU: Comparator active
   Pins: $\overline{RESET}$ at V_{CC}, TEST at GND
   D_0 to D_4, D_{12}, D_{13}, R1, R2 at V_{disp} voltage
   D_5 to D_8 at V_{CC}, D_9 to D_{11} at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test condition: MCU: Input/output in reset state
   MCU in standby mode
   Pins: $\overline{RESET}$ at V_{CC}, TEST at GND
   D_0 to D_4, D_{12}, D_{13}, R1, R2 at V_{disp} voltage
   D_5 to D_{11} at V_{CC}

5. Power dissipation is in proportion to f_{OSC} while the MCU is operating or is in standby mode. The value of the dissipation current when f_{OSC} = x MHz is given by the following equation: Maximum value (f_{OSC} = x MHz) = x/4 × maximum value (HD404272: f_{OSC} = 4 MHz, HD40L4272: f_{OSC} = 1 MHz)

6. Excluding pull-down MOS current.

7. The reference voltage is the expected internal VC_{ref} voltage selected by the reference voltage select register (RSR).
   Example: when RSR = $1 reference voltage is 2/11 × V_{CC}.

Input/Output Characteristics for Standard Pins (HD404272: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C; HD40L4272: V_{CC} = 2.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_5–D_{11}	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_5–D_{11}	–0.3	—	0.3 V_{CC}	V		
Output high voltage	V_{OH}	D_5–D_{11}	V_{CC} – 1.0	—	—	V	HD404272: $-I_{OH}$ = 1.0 mA	1
			V_{CC} – 0.5	—	—	V	HD40L4272: $-I_{OH}$ = 0.5 mA	1
Output low voltage	V_{OL}	D_5–D_{11}	—	—	0.4	V	HD404272: I_{OL} = 0.5 mA; HD40L4272: I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	D_5–D_{11}	—	—	1	µA	V_{in} = 0 V to V_{CC}	2
Pull-up MOS current	$-I_{PU}$	D_5–D_{11}	40	80	160	µA	HD404272: V_{CC} = 5 V, V_{in} = 0 V	3
			10	25	60	µA	HD40L4272: V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. Applied to I/O pins selected as CMOS output by mask option.
2. Excluding output buffer current and pull-up MOS current.
3. Applies to I/O pins with pull-up MOS selected as mask option.

Input/Output Characteristics for High Voltage Pins (HD404272: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C; HD40L4272: V_{CC} = 2.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_4, D_{12}, D_{13}, R1, R2	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_4, D_{12}, D_{13}, R1, R2	V_{CC} – 40	—	0.3 V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_4, D_{12}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 1.0	—	—	V	HD404272: $-I_{OH}$ = 4 mA; HD40L4272: $-I_{OH}$ = 2.5 mA	
		R1, R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 2 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 1.0	—	—	V	HD404272: $-I_{OH}$ = 0.8 mA; HD40L4272: $-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_4, D_{12}, R1, R2	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
		D_0–D_4, D_{12}, R1, R2	—	—	V_{CC} – 37	V	150 KΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_0–D_4, D_{12}, D_{13}, R1, R2	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_{PD}	D_0–D_4, D_{12}, R1, R2	125	—	900	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-down MOS by mask option.
2. Applied to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Excluding pull-down MOS current and output buffer current.

AC Characteristics (HD404272: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C; HD40L4272: V_{CC} = 2.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency (ceramic oscillator)	f_{OSC}	OSC_1, OSC_2	1	4	4.5	MHz	HD404272	
			0.4	1	1.125	MHz	HD40L4272	
Oscillation frequency (resistor oscillator)	f_{OSC}	OSC_1, OSC_2	1	—	3.0	MHz	HD404272 Rf = 20 kΩ ±1%	
Instruction cycle time (ceramic oscillator)	t_{cyc}	—	0.89	1	4	µs	HD404272 divided by 4	
			3.55	4	10	µs	HD40L4272 divided by 4	
Instruction cycle time (resistor oscillator)	t_{cyc}	—	1.33	—	4	µs	HD404272 divided by 4	
Oscillator stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
Oscillator stabilization time (resistor oscillator)	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	HD404272	
Capacitance between pins	C_{RF}	OSC_1, OSC_2	—	—	1	pF	HD404272	
External clock high and low level widths	t_{CPH}, t_{CPL}	OSC_1	92	—	—	ns	HD404272	2
		OSC_1	425	—	—	ns	HD40L4272	2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}$ high width	t_{IH}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{INT}$ low width	t_{IL}	$\overline{INT}$	2	—	—	t_{cyc}		3
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
Input capacitance	C_{in}	All pins	—	—	30	pF	f = 1 MHz, V_{in} = 0 V, T_a = 25°C	
Comparator stabilization time	t_{CSTB}	$COMP_0$	—	—	2	t_{cyc}		

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage (HD404272: 3.5 V; HD40L4272: 2.5 V) at power-on to when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode release, $\overline{RESET}$ must be kept low for at least t_{RC}. Since t_{RC} dpends on the ceramic oscillator's circuit constant and stray capacitance, please consult with the ceramic oscillator manufacturer when designing the reset circuit.
2. Refer to figure 28
3. Refer to figure 29
4. Refer to figure 30

Serial Interface Timing Characteristics (HD404272: V_{CC} = 3.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C; HD40L4272: V_{CC} = 2.5 V to 6.0 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to 75°C unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 32	1
Transmit clock high and low widths	t_{SCKH} t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 32	1
Transmit clock rise and fall times	t_{SCKr} t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HD404272 load shown in figure 32	1
			—	—	300	ns	HD40L4272 load shown in figure 32	1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	Load shown in figure 32	1
			—	—	600	ns	HD40L4272 load shown in figure 32	1
Serial input data set-up time	t_{SSI}	SI	300	—	—	ns	HD404272	1
			1000	—	—	ns	HD40L4272	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HD404272	1
			500	—	—	ns	HD40L4272	1

During Transmit Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high and low widths	t_{SCKH} t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise and fall times	t_{SCKr} t_{SCKf}	$\overline{SCK}$	—	—	100	ns	HD404272	1
			—	—	300	ns	HD40L4272	1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	HD404272 load shown in figure 32	1
			—	—	600	ns	HD40L4272 load shown in figure 32	1
Serial input data set-up time	t_{SSI}	SI	300	—	—	ns	HD404272	1
			1000	—	—	ns	HD40L4272	1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns	HD404272	1
			500	—	—	ns	HD40L4272	1

Note: 1. Refer to figure 31

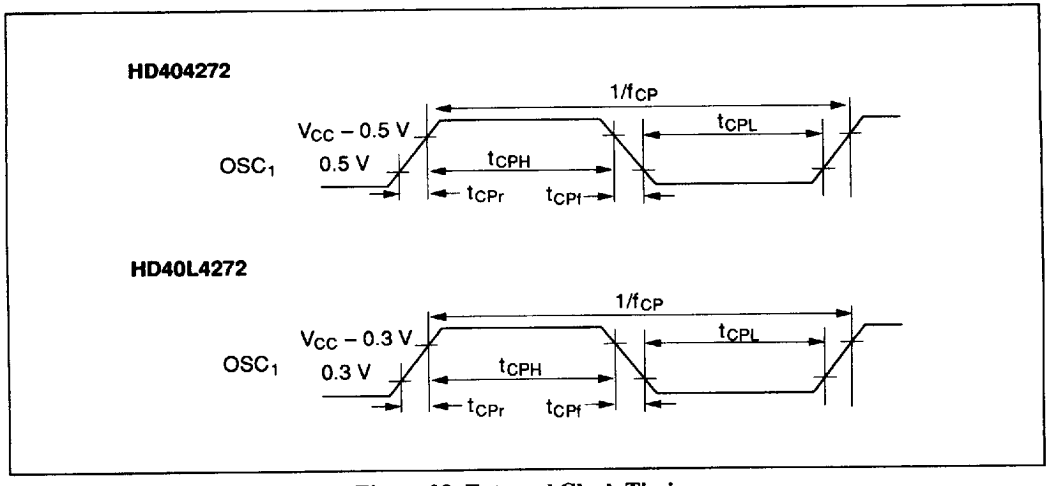


Figure 28 External Clock Timing

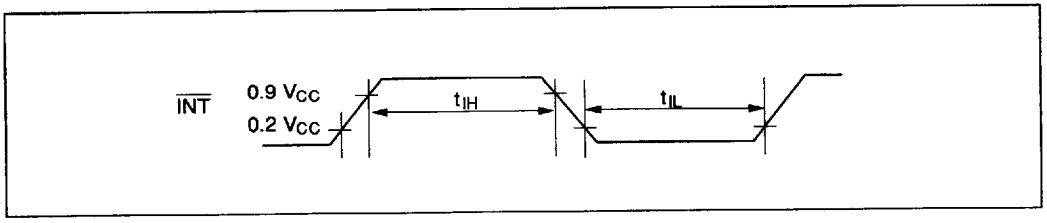


Figure 29 Interrupt Timing

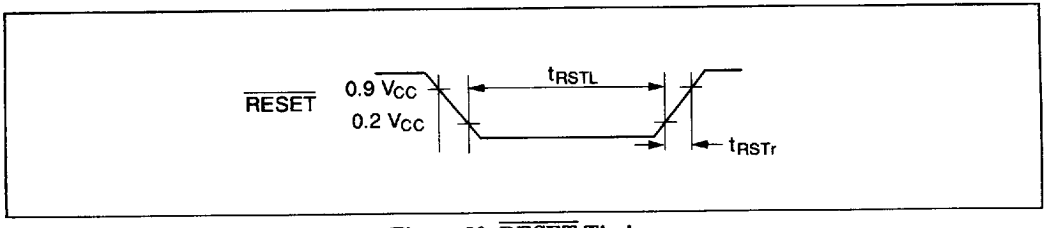
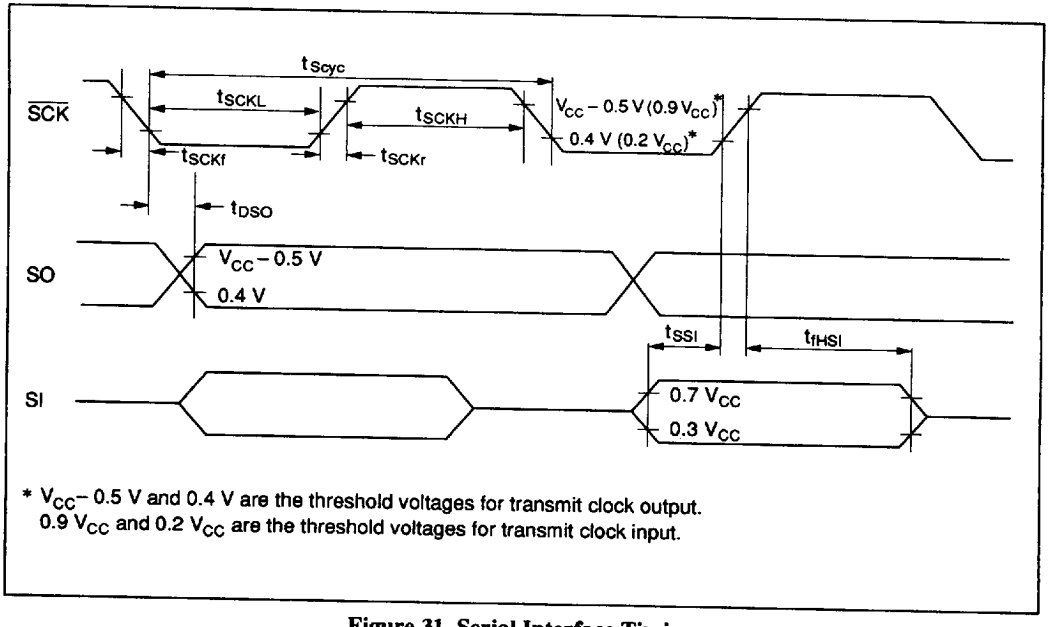


Figure 30 $\overline{\text{RESET}}$ Timing



* V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
0.9 V_{CC} and 0.2 V_{CC} are the threshold voltages for transmit clock input.

Figure 31 Serial Interface Timing

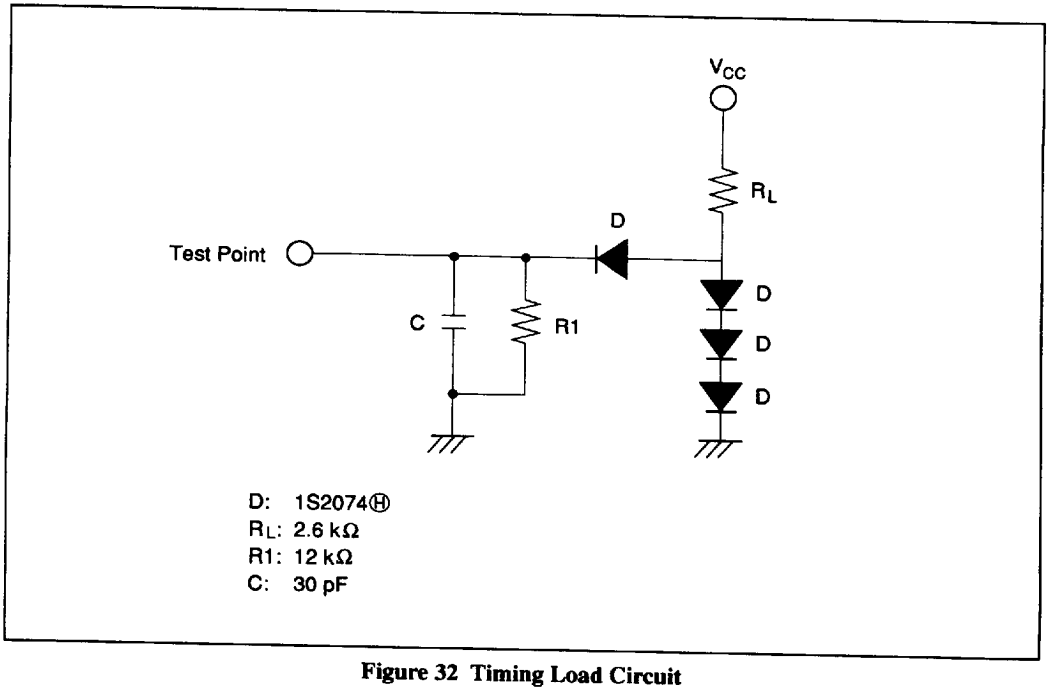


Figure 32 Timing Load Circuit

HD404272, HD40L4272 Option List

Please check off the appropriate applications and enter the necessary information.

Order date	
Customer name	
Department	
Name	
ROM code name	
LSI type name	

☐ 5-V operation: HD404272
☐ Low-voltage operation: HD40L4272

1. I/O Options

Note: I/O option masked by ▨ are not available.

Pin Name	I/O	I/O Option				
		A	B	C	D	E
D0	I/O	▨	▨	▨		
D1	I/O	▨	▨	▨		
D2	I/O	▨	▨	▨		
D3	I/O	▨	▨	▨		
D4	I/O	▨	▨	▨		
D5	I/O				▨	▨
D6	I/O				▨	▨
D7	I/O				▨	▨
D8	I/O				▨	▨
D9	I/O				▨	▨
D10	I/O				▨	▨

Pin Name	I/O	I/O Option				
		A	B	C	D	E
D11	I/O				▨	▨
D12	I/O	▨	▨	▨		
D13	▨	Use checklist D13/Vdisp				
R10	I/O	▨	▨	▨		
R11	I/O	▨	▨	▨		
R12	I/O	▨	▨	▨		
R13	I/O	▨	▨	▨		
R20	I/O	▨	▨	▨		
R21	I/O	▨	▨	▨		
R22	I/O	▨	▨	▨		
R23	I/O	▨	▨	▨		

A: Without pull-up MOS (open drain NMOS) B: With pull-up MOS
C: CMOS (Input is disabled)
D: High voltage I/O without pull-up MOS E: High voltage I/O with pull-up MOS

2. D13/Vdisp

☐ Input port
☐ Vdisp supply

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

3. Timer A

☐ Free-running timer operation
☐ Watchdog timer operation

4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), then using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).

☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. Oscillator

HD404272		HD40L4272	
☐ External clock	f = MHz	☐ External clock	f = MHz
☐ Resistor	f = MHz	▨	▨
☐ Ceramic oscillator	f = MHz	☐ Ceramic oscillator	f = MHz

6. Stop Mode

☐ Used
☐ Not used

7. Package

☐ DP-28S
☐ FP-28DA