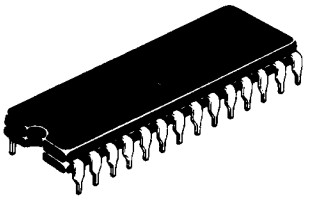
HMCS42C(HD44700), HMCS42CL(HD44708)

The HMCS42C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, and I/O on single chip. The HMCS42C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS42C provides the flexibility of microcomputers for battery powered and battery back-up applications.

■ FEATURES

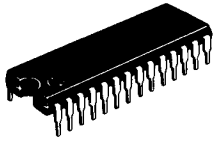
- 4-bit Architecture
- 512 Words of Program ROM (10 bits/Word)
  32 Words of Pattern ROM (10 bits/Word)
- 32 Digits of Data RAM (4 bits/Digit)
- 22 I/O Lines
- Instruction Cycle Time: HMCS42C; 10 μs
  HMCS42CL; 20 μs
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  — Table Look Up Capability —
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator
- Built-in Power-on Reset Circuit (HMCS42C only)
- Low Operating Power Dissipation; 1.5mW typ.
- Stand-by Mode (Halt Mode); 50 μW max.
- CMOS Technology
- Single Power Supply: HMCS42C; 5V±10%
  HMCS42CL; 2.5V to 5.5V

HMCS42C,HMCS42CL



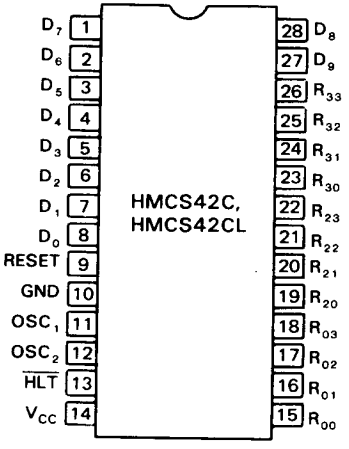
(DP-28)

HMCS42C



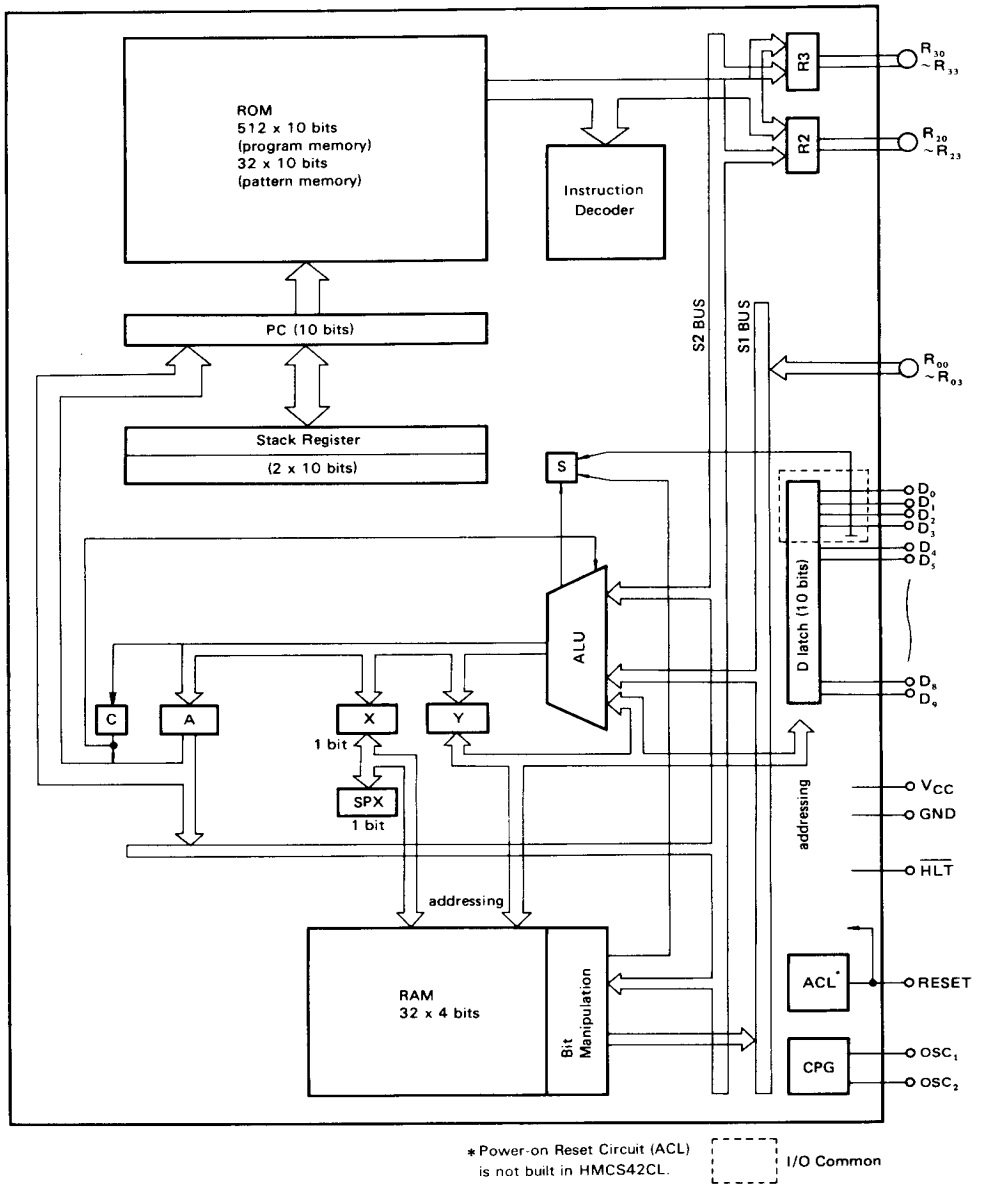
(DP-28S)

■ PIN ARRANGEMENT



(Top View)

■ **BLOCK DIAGRAM**



■ HMCS42C ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Pin Voltage (1)	V_{T1}	−0.3 to V_{CC}+0.3	V	Except for pins specified by V_{T2}
Pin Voltage (2)	V_{T2}	−0.3 to +10.0	V	Applied to only open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{o1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{o2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2". If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to GND.
[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

• ELECTRICAL CHARACTERISTICS-1 (V_{CC}=5V±10%, Ta=−20 to +75°C)

Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}−1.0	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		V_{CC}−1.0	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL}=1.6mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$=1.0mA	2.4	–	–	V	4
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$=0.01mA	V_{CC}−0.3	–	–	V	5
Output "High" Current	I_{OH}	V_{OH}=10V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	–	–	1.0	μA	2, 7
		V_{in}=0 to 10V	–	–	3		7
Pull up MOS Current	$-I_P$	V_{CC}=5V	60	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in}=V_{CC}, Ceramic Filter Oscillation	–	–	1.6	mA	
Supply Current (2)	I_{CC2}	V_{in}=V_{CC}, R_f Oscillation External Clock Operation	–	–	0.8	mA	
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$=1.0V, V_{in}=0 to V_{CC}	–	–	1	μA	2, 7
		$\overline{HLT}$=1.0V, V_{in}=0 to 10V	–	–	3	μA	8
Standby Supply Current	I_{CCS}	V_{in}=V_{CC}, $\overline{HLT}$=0.2V	–	–	10	μA	9
External Clock Operation							
External Clock Frequency	f_{cp}		200	400	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{cp}	9.1	10	20	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{OSC}	R_f=91kΩ±2%	300	–	500	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{OSC}	8.0	–	13.3	μs	
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{OSC}	Ceramic Filter	392	–	408	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{OSC}	9.8	–	10.2	μs	

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.

[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the With Pull up MOS or CMOS type of I/O or Output pins.
[NOTE 6] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 7] I/O current is excluded.
[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at $V_{CC}=5V\pm10\%$ in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

• **ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75°C)

Reset and Halt

Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit
Halt Duration Voltage	V_{DH}	$\overline{HLT}=0.2V$	2.3	–	–	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$, $\overline{HLT}=0.2V$, $V_{DH}=2.3V$	–	–	10	μA
Halt Delay Time	t_{HD}		100	–	–	μs
Operation Recovery Time	t_{RC}		100	–	–	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		–	–	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		–	–	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	–	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	0.1	–	–	ms
		Ceramic Filter Oscillation	4	–	–	
Power Supply Rise Time	t_{rcc}	Built-in Reset, $\overline{HLT}=V_{CC}$	0.1	–	10	ms
Power Supply OFF Time	t_{OFF}	Built-in Reset, $\overline{HLT}=V_{CC}$	1	–	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset, $V_{CC}=4.5$ to 5.5V, $\overline{HLT}=V_{CC}$ (R_f Oscillation, External Clock Operation)	1	–	–	ms
		External Reset $V_{CC}=4.5$ to 5.5V, $\overline{HLT}=V_{CC}$ (Ceramic Filter Oscillation)	4	–	–	
RESET Pulse Width (2)	t_{RST2}	External Reset $V_{CC}=4.5$ to 5.5V, $\overline{HLT}=V_{CC}$	$2\cdot T_{inst}$	–	–	μs
RESET Rise Time	t_{rRST}	External Reset $V_{CC}=4.5$ to 5.5V, $\overline{HLT}=V_{CC}$	–	–	20	ms
RESET Fall Time	t_{fRST}	External Reset $V_{CC}=4.5$ to 5.5V, $\overline{HLT}=V_{CC}$	–	–	20	ms

[NOTE] All voltages are with respect to GND.

■ HMCS42CL ELECTRICAL CHARACTERISTICS (V_{CC}=2.5V to 5.5V)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Pin Voltage (1)	V_{T1}	−0.3 to V_{CC}+0.3	V	Except for pins specified by V_{T2}
Pin Voltage (2)	V_{T2}	−0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{o1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{o2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to GND.
[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

• ELECTRICAL CHARACTERISTICS-1 (V_{CC}=2.5 to 5.5V, Ta=−20 to +75°C)

Item	Symbol	Test Conditions		Value min	Value typ	Value max	Unit	Note
Input "Low" Voltage	V_{IL}			–	–	0.15·V_{CC}	V	
Input "High" Voltage (1)	V_{IH1}			0.85·V_{CC}	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}			0.85·V_{CC}	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL}=0.4mA		–	–	0.4	V	
Output "High" Voltage	V_{OH}	$-I_{OH}$=0.08mA		V_{CC}−0.4	–	–	V	4
Output "High" Current	I_{OH}	V_{OH}=10V		–	–	3	μA	5
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}		–	–	1.0	μA	2, 6
		V_{in}=0 to 10V		–	–	3		6
Pull up MOS Current	$-I_P$	V_{CC}=3V		10	–	80	μA	
Supply Current	I_{CC}	V_{in}=V_{CC}, V_{CC}=3V (f_{OSC}/f_{cp}=200kHz) R_f Oscillation, External Clock Operation		–	–	100	μA	
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$=0.5V	V_{in}=0 to V_{CC}	–	–	1	μA	2, 6
			V_{in}=0 to 10V	–	–	3	μA	7
Standby Supply Current	I_{CCS}	V_{in}=V_{CC}, $\overline{HLT}$=0.1V	V_{CC}=2.5 to 3.5V	–	–	6	μA	8
			V_{CC}=2.5 to 5.5V	–	–	10	μA	

(to be continued)

Item	Symbol	Test Conditions	Value			Unit	Note
			min	typ	max		
External Clock Operation							
External Clock Frequency	f_{cp}		130	200	240	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{cp}$	16.8	20	30.8	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{OSC}	$R_f=180k\Omega\pm2\%$, $V_{CC}=2.5$ to 3.5V	130	–	250	kHz	
		$R_f=180k\Omega\pm2\%$, $V_{CC}=2.5$ to 5.5V	130	–	350		
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{OSC}$, $V_{CC}=2.5$ to 3.5V	16	–	30.8	μs	
		$T_{inst}=4/f_{OSC}$, $V_{CC}=2.5$ to 5.5V	11.4	–	30.8		

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT, and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This ia applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 6] I/O current is excluded.
[NOTE 7] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 8] I/O current is excluded.
The Standby Supply Current is the supply current at $V_{CC}=2.5$ to 5.5V in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

• **ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75°C)

Reset and Halt

Item	Symbol	Test Conditions	Value		Unit
			min	max	
Halt Duration Voltage	V_{DH}	$\overline{HLT}=0.2V$	2.0	–	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$, $\overline{HLT}=0.1V$ $V_{DH}=2.0V$	–	10	μA
Halt Delay Time	t_{HD}		200	–	μs
Operation Recovery Time	t_{RC}		200	–	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		800	–	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation $V_{CC}=2.5$ to 5.5V	0.2	–	ms
RESET Pulse Width (1)	t_{RST1}	$V_{CC}=2.5$ to 5.5V, $\overline{HLT}=V_{CC}$ (R_f Oscillation, External Clock Operation)	2	–	ms
RESET Pulse Width (2)	t_{RST2}	$V_{CC}=2.5$ to 5.5V $\overline{HLT}=V_{CC}$	$2\cdot T_{inst}$	–	μs
RESET Fall Time	t_{fRST}	$\overline{HLT}=V_{CC}$	–	20	ms
RESET Rise Time	t_{rRST}	$\overline{HLT}=V_{CC}$	–	20	ms

[NOTE] All voltages are with respect to GND.

■ SIGNAL DESCRIPTION

The input and output signals for the HMCS42C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

• V_{CC} and GND

Power is supplied to the HMCS42C using these two pins. V_{CC} is power and GND is the ground connection.

• RESET and $\overline{HLT}$

The status of the Halt and Reset depends on the following truth table.

RESET	$\overline{HLT}$	Operation
0	1	Operating State
1	1	Reset State
0	0	Halt State
1	0	Not Allowable

• OSC_1 and OSC_2

These pins provide control input for the built-in oscillator circuit. A resistor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized.

Refer to OSCILLATOR for recommendations about these pins.

• R_{00} to R_{03}

These 4 lines are arranged into one 4-bit Data Input Channel. It is directly addressed by the operand of input instruction.

Refer to INPUT/OUTPUT for additional information.

• R_{20} to R_{23}, R_{30} to R_{33}

These 8 lines are arranged into two 4-bit Data Output Channels. The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of output instruction.

Refer to INPUT/OUTPUT for additional information.

• D_0 to D_3

These lines are four 1-bit Discrete Input/Output Common pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register. It is also addressed directly by the operand of input/output instruction.

Refer to INPUT/OUTPUT for additional information.

• D_4 to D_9

These lines are six 1-bit Discrete Output pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register.

Refer to INPUT/OUTPUT for additional information.

■ ROM

• ROM Address Space

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS42C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

The ROM address is composed of the program area (page 0 to page 14) and the pattern area (pages 26, 30). (64 words/page.)

The ROM capacity is 544 words (1 word = 10 bits) in all.

Only the program area can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 1.

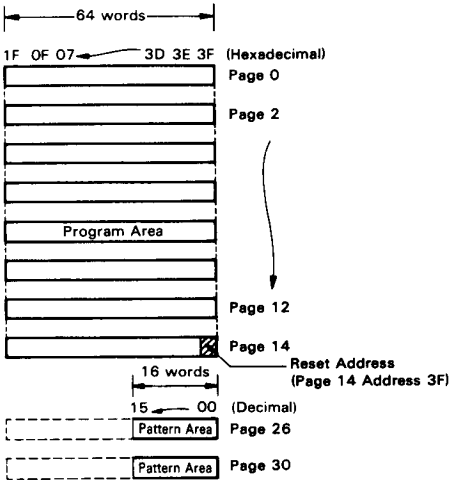


Figure 1 ROM Address Space

• Program Counter (PC)

The program counter is used for addressing the program area. It consists of the page part and the address part as shown in Figure 2.

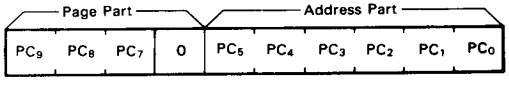


Figure 2 Configuration of Program Counter

Once a certain value is loaded into a page part, it is unchanged until other value is loaded by the program. Any number among 0 to 14 can be set in the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexadecimal system is shown in Table 1. This sequence forms a loop and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the page part is changed.

Table 1 Program Counter Address Part Sequence

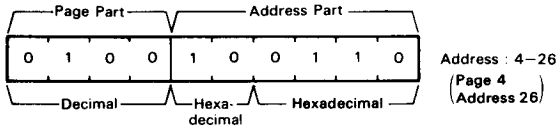
Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

• Designation of ROM Address and ROM Code

The page part is represented by decimal and the address part is divided into 2 parts (2 bits and 4 bits) and represented by hexadecimal.

One word (10 bits) is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10}) and represented by hexadecimal. The examples are shown in Figure 3.

(a) ROM Address



(b) ROM Code

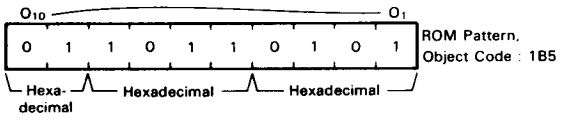


Figure 3 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constants) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

• Reference

ROM addressing for the pattern reference is performed by modifying the program counter with the accumulator, the carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and 0s, while the page part is logically ORed with 0s, C (F/F) and the lower bit of the operand p (p_0). The upper bit (p_1) of the operand is for referring to the pattern area.

Non-existing ROM area can not be referred.

The contents of PC is only modified apparently and is not changed. Then the address is counted up after the execution of the pattern instruction and next instruction but one is executed. Therefore, the instruction just after the pattern instruction (P) should be NOP.

The pattern instruction is executed in 2 cycles.

• Generation

The bit pattern of referred ROM address is generated by the following two ways.

(i) The pattern is loaded into Accumulator.

(ii)The pattern is loaded into the data I/O registers R2 and R3.

The command bits (O_9, O_{10}) in the pattern determine which way is taken.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and mode (ii) are simultaneously performed when both O_9 and O_{10} are "1".

The correspondence of each bit of the pattern is shown in Figure 5.

CAUTION

In the program execution, the pattern can not be distinguished from the instruction. When the program is running at the address written as a pattern, the instruction corresponding to the pattern bit is executed. Take care not to execute a pattern as an instruction.

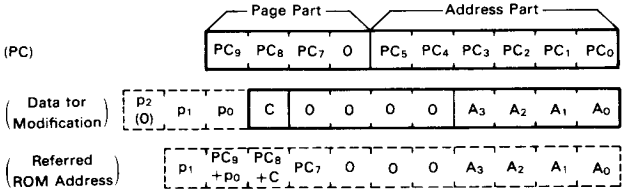


Figure 4 ROM Addressing for Pattern Generation

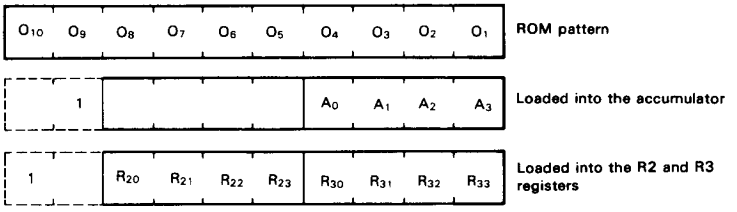


Figure 5 Correspondence of Each Bit of Pattern

Table 2 Example of how to use Pattern Instruction

Before Execution					Referred ROM Address	Pattern	After Execution				Remarks
PC Value	p	C	B	A			B	A	R2	R3	
0-3F	1	0		0	8-00	131		8	–	–	
2-3F	3	1		8	30-08	231		–	C	8	
14-00	2	0/1		9	30-09	331		8	C	8	
10-01	2	0		5	26-05	331		8	C	8	
8-00	2	1		5	28-05						Not allowable

* "–" means that the value does not change after execution of the instruction.
** "0/1" means that either "0" or "1" may be selected.
*** The value of PC and the ROM address are divided into the page and the address parts. The page part is represented by decimal and the address part by hexadecimal.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to an optional address out of the sequence, there are four ways.

They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM output (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter. This instruction is a conditional instruction and executed only when the Status is "1". If it is "0", the instruction is skipped and it becomes "1". The operation is shown in Figure 6.

• LPU

By LPU instruction, a jump between pages is performed.

The lower 4 bits of ROM output are transferred to the page part of the program counter with delay by one-cycle time. Therefore, the cycle just after the issuing of this instruction is on the same page and the page jump is performed at the next cycle.

This instruction is conditional, and is executed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped.

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

The LPU operation is shown in Figure 7.

• BRL

By BRL instruction, the program branches to an address in

any page.

This is a macro instruction composed of LPU and BR and divided into two steps as follows.

```
                                BRL   a – b → LPU  a
<Jump to address b on page a>         BR    b
```

BRL instruction is a conditional instruction because of its characteristics of LPU and BR instructions, and is executed only when the Status is "1". When the Status is "0", this instruction is skipped and the Status becomes "1".

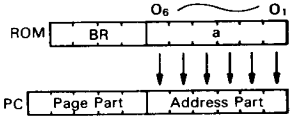


Figure 6 BR Operation

- **TBR (Table Branch)**

By TBR instruction, the program branches referring to the table.

The program counter is modified by Accumulator, the Carry F/F, and the operand p. Accumulator and 0s are assigned into the address part of the program counter. The 0s, Carry F/F, and the operand p_1, p_0 are logically ORed with the page part of the program counter.

TBR modifies the PC in the same way as the pattern instruction (P) does. The method for modification is shown in Figure 8.

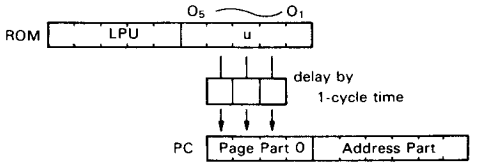


Figure 7 LPU Operation

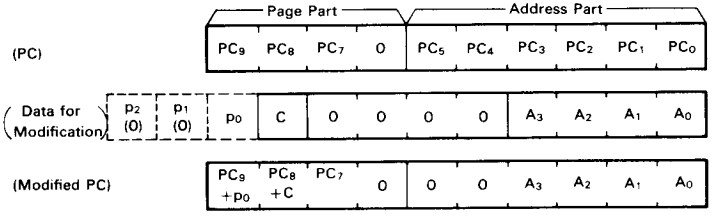


Figure 8 Modification of Program Counter by TBR Instruction

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

- **CAL**

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The program counter is saved in the following order.

$$PC+1 \rightarrow ST1 \rightarrow ST2$$

The page part of PC is 0. The lower 6 bits of ROM output (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter.

CAL instruction is a conditional instruction and executed only when the Status is "1". If it is "0", the instruction is skipped and it becomes "1".

The save condition of the program counter when CAL instruction is executed is shown in Figure 9.

- **CALL**

By CALL instruction, subroutine jump to an address in any page is performed.

This is a macro instruction of LPU and CAL. The subroutine jump to the page specified by LPU enables the subroutine jump to an optional address.

```
                                CALL  a – b → LPU  a
<Subroutine jump to address b on page a>      CAL  b
```

CALL instruction is conditional because of its characteristics of LPU and CAL instructions and is executed when the Status is "1". If the Status is "0", this instruction is skipped and the Status becomes "1".

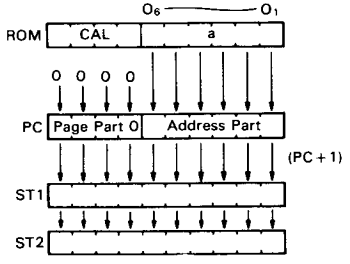


Figure 9 Subroutine Jump Stacking Order

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 32 digits (128 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by the matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits, 13 digits (MR0, MR4 to MR15), are called "Memory Register (MR)". The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 10.

If an instruction consists of a simultaneous read/write operation of RAM (exchange between the contents of RAM and those

of the register), the writing data doesn't affect the reading data because read operation precedes write operation.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset, or tested. The bit assignment is specified by the operand n of the instruction.

X	f \ d / Y	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0																MR0
4	4	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4				

← digit No.

↑ file No.

Figure 10 RAM Address Space

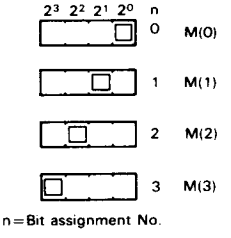


Figure 11 RAM Bit and Operand n

■ REGISTER

The HMCS42C has four registers and two latches available to the programmer. The latches are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

• Status F/F (S)

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

• Accumulator (A; A Register) and Carry F/F (C)

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F respectively. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

• X Register (X)

The result of ALU operation (1 bit) is loaded into this register. The X register is exchangeable with the SPX register. The X register addresses the RAM file and composed of 1-bit (0 or 4) register.

• SPX Register (SPX)

The SPX register is exchangeable with the X register.

The SPX register is used to stack the contents of the X register and expand the addressing system of RAM in combination with the X register. It is composed of 1-bit (0 or 4) register.

• Y Register (Y)

The result of ALU operation (4 bits) is loaded into this register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digit and 1-bit Discrete I/O.

■ INPUT/OUTPUT

• 4-bit Data Input/Output Channel (R)

The HMCS42C has one 4-bit Data Input Channel (R0) and two Data Output Channels (R2, R3).

The 4-bit register is attached to R2 and R3 channels.

Channel addressing is performed by the program. The input instruction inputs 4-bit data into the accumulator (A register) through R0 channel.

The data is transferred from the accumulator to the Data I/O Registers R2 and R3 via the bus lines. ROM bit patterns are loaded into the Data I/O Registers R2 and R3 by the pattern instruction.

The block diagram is shown in Figure 12. The I/O timing is shown in Figure 13.

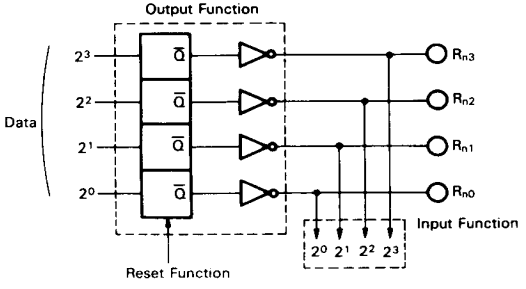


Figure 12 4-bit Data I/O Block Diagram

• 1-bit Discrete Input/Output Pin (D)

The HMCS42C has ten 1-bit Discrete Pins. The D_0 to D_3 are 1-bit Discrete I/O Common Pins and the D_4 to D_9 are 1-bit Dis-

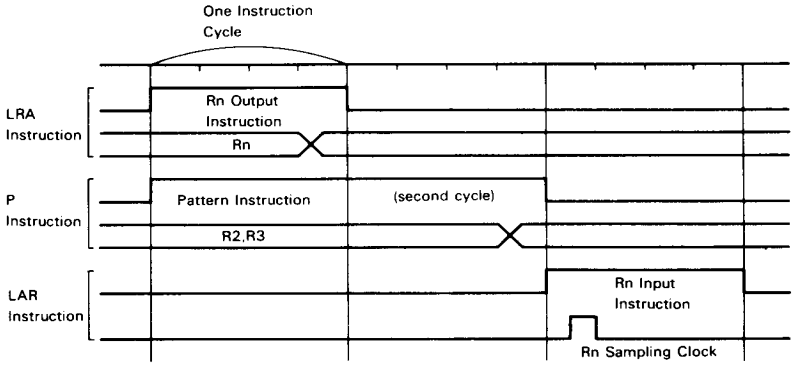


Figure 13 4-bit Data I/O Timing

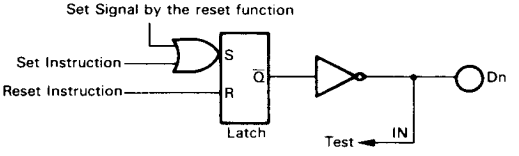


Figure 14 1-bit Discrete I/O Block Diagram

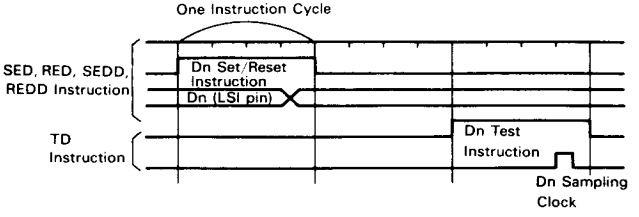


Figure 15 1-bit Discrete I/O Timing

crete Output Pins.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and level ("0" or "1") of the addressed pin can be tested by an input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before execution of input instruction.

The D_0 to D_3 pins are also addressed directly by the operand n of input/output instruction and can be set or reset.

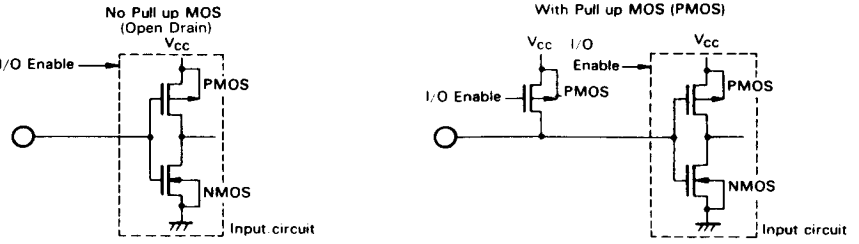
The block diagram is shown in Figure 14 and the I/O timing is in Figure 15.

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain and With Pull up MOS using a mask option as shown in Figure 16.

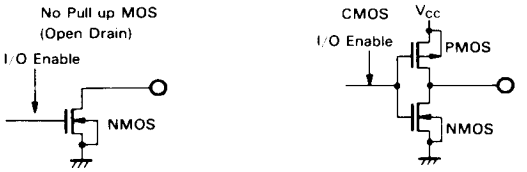
(a) Configuration of Input Pin

Applied Pins ; R_{00} to R_{03}



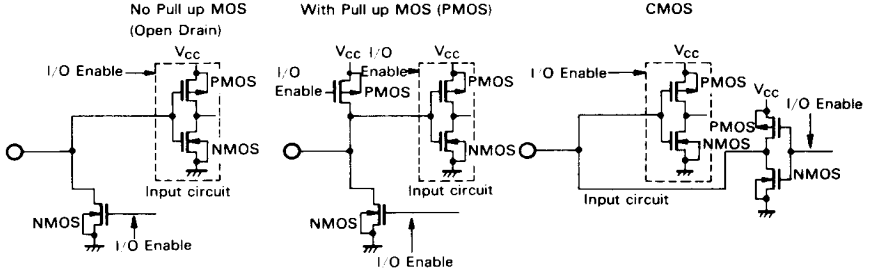
(b) Configuration of Output Pin

Applied Pins ; D_4 to D_9 , R_{20} to R_{23}, R_{30} to R_{33}



(c) Configuration of I/O Pin

Applied Pins ; D_0 to D_3



*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit, Pull up MOS and NMOS output and sets CMOS output to high impedance (PMOS, NMOS; OFF).

Figure 16 I/O Configuration

■ RESET FUNCTION

The status of the Reset depends on the following truth table. Moreover, the HMCS42C has the automatic reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply; Refer to Figure 18. When the Built-in Reset Circuit is used, RESET should be connected to V_{SS}.

HMCS42CL doesn't have the Built-in Reset Circuit.

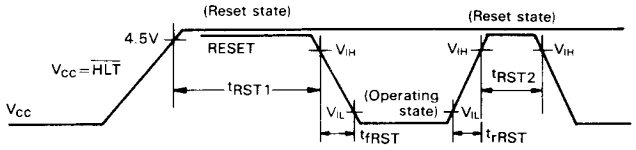
Internal state of the HMCS42C are specified as follows by the reset function.

- Program Counter (PC) is set to address 3F on page 14 (14-3F).
- I/O latch and Registers (D_0 to D_9, R2, R3) are set to "1".

Note that other blocks (Status, Register, RAM, etc.) are not cleared.

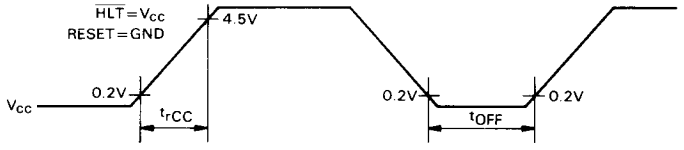
RESET	$\overline{HLT}$	Operation
0	1	Operating State
1	1	Reset State
0	0	Halt State
1	0	Not Allowable

[NOTE] RESET and $\overline{HLT}$ pins should not be changed simultaneously not to malfunction.



· t_{RST1} includes the time required from the power ON until the operation gets into the constant state.
· t_{RST2} is applied when the operation is in the constant state.

Figure 17 RESET Timing



t_{OFF} specifies the period when the power supply is OFF, when a short break of the power supply occurs and the power supply ON/OFF is repeated.

Figure 18 Power Supply Timing for Built-in Reset Circuit

■ HALT FUNCTION

When the $\overline{HLT}$ pin is set to "0" ("Low" level) and the RESET pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, etc.) are held. Refer to the truth table in RESET FUNCTION. Because all internal logic operations stop in this state, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at ROM ordering.

"Enable"
- Output ..... The Status before the Halt State is held.
- Pull up MOS... ON
- Input..... No relation to "Halt"

Since Pull up MOS is ON, Pull up MOS current flows when output is "0" ("Low" level) in the Halt State (NMOS; ON). When an input signal changes, transmission current flows into an input circuit. Also, current flows into Pull up MOS. These currents are added to the Stand-by Supply Current (or Halt Current).

"Disable"
- Output ..... High Impedance (NMOS, PMOS: OFF)
- Pull up MOS... OFF
- Input..... Input Circuit: OFF

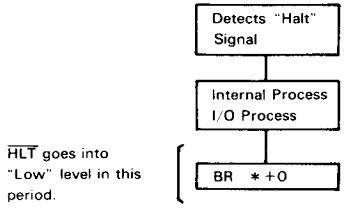
Both input and output are at high impedance state. Since an input circuit is OFF, only the Stand-by Supply Current (or Halt Current) flows even if an input signal changes.

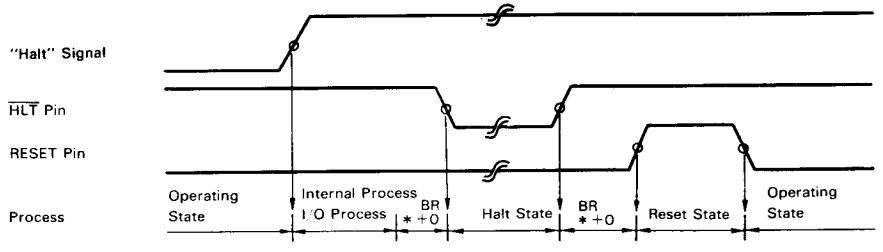
When the $\overline{HLT}$ pin is set to "1" ("High" level), the HMCS-42C gets into operation from the status just before the Halt State. The halt timing is shown in Figure 19.

CAUTION

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

(NOTE)
Release "Halt" according to the following sequence for Ceramic Filter Oscillation. Though abnormal oscillation occurs after releasing "Halt" in the case of Ceramic Filter Oscillation, the system does not malfunction because of executing BR * +0. Reset and restart after that operation.





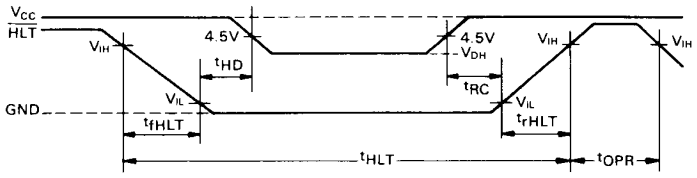


Figure 19 Halt Timing

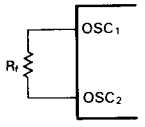
■ OSCILLATOR

The HMCS42C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor R_f or ceramic filter circuit (Internal Clock Operation).

The OSC_1 clock frequency is internally divided by four to produce the internal system clocks.

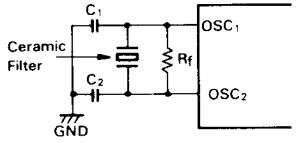
The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 20. There is no need of specifying it by using the mask option.

(a) Internal Clock Operation Using Resistor R_f



Wiring of OSC_1 and OSC_2 pins should be as short as possible because the oscillation frequency is modified by capacitance of these pins.

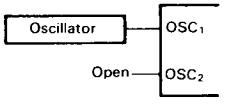
(b) Internal Clock Operation Using Ceramic Filter Circuit
(This is not applied to HMCS42CL)

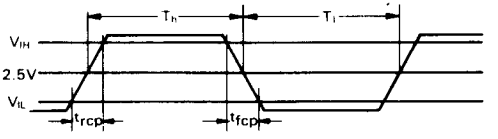


Ceramic Filter : CSB400P (MURATA)
R_f : 1MΩ ± 10%
C_1 : 680pF ± 10% (ceramic capacitor)
C_2 : 470pF ± 10% (ceramic capacitor)

When halt function is applied, keep the "NOTE" in "HALT FUNCTION"
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

(c) External Clock Operation





$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 20 Clock Operation Mode

■ INSTRUCTION LIST

The instructions of the HMCS42C are listed according to their functions, as shown in Table 3.

Table 3 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAY	Y → A	
	LASPX	SPX → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
RAM · Register Instruction	LAM (X)	M → A (X ↔ SPX)	
	XMA (X)	M ↔ A (X ↔ SPX)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
Arithmetic Instruction	AI i	A+i → A	C
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−$\overline{C}$ (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\overline{A}$+1 → A	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M (n)

(to be continued)

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Group	Mnemonic	Function	Status
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D (Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R (p) → A	
	LRA p	A → R (p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (XY) after a mnemonic code has two meanings as follows.

	Mnemonic only	Instruction execution only
	Mnemonic with X	After instruction execution, X ↔ SPX
[Example]	LAM	M → A
	LAMX	M → A, X ↔ SPX

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ ..... ALU Not Zero
   - C ..... ALU Overflow in Addition, that is, Carry
   - NB ..... ALU Overflow in Subtraction, that is, No Borrow
   - Except above ..... Contents of the status column affects the Status F/F directly.
3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F.
   Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1 cycle. The pattern instruction (P) is executed in 2 cycles.

HMCS42C Mask Option List

☐	5V Operation : HMCS42C
☐	3V Operation : HMCS42CL

☆ Mark "✓" in "☐" for the selected spec.

Date	
Customer	
Dept.	
Name	
ROM CODE ID	
LSI Type Name (entered by Hitachi)	

(1) I/O Option

Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks	Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks
D_0	I/O					R_{00}	I				
D_1	I/O					R_{01}	I				
D_2	I/O					R_{02}	I				
D_3	I/O					R_{03}	I				
D_4	O					R_{20}	O				
D_5	O					R_{21}	O				
D_6	O					R_{22}	O				
D_7	O					R_{23}	O				
D_8	O					R_{30}	O				
D_9	O					R_{31}	O				
						R_{32}	O				
						R_{33}	O				

☆ Specify the I/O composition with a mark of "O" in the applicable composition column.
A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) I/O State at "Halt" mode

I/O State	
☐	Enable
☐	Disable

☆ Mark "✓" in "☐" for the selected I/O state.

(3) Package

Package	
☐	DP-28
☐	DP-28S

☆ Mark "✓" in "☐" for the selected package.

Check List of Application

[A] Oscillator (CPG option)

CPG	5V Operation	3V Operation
Resistor	☐ $R_f = 91k\Omega \pm 2\%$	☐ $R_f = 180k\Omega \pm 2\%$
Ceramic Filter	☐ MURATA: CSB400P	
	☐ TDK: FCR400K	
	☐ Kyocera: KBR-400B	
External Clock	☐ $f_{cp} = 200k$ to 440kHz	☐ $f_{cp} = 130k$ to 240kHz

☆ Mark "✓" in "☐" for the selected oscillator.

[B] Halt function (Only when Ceramic Filter is selected in [A].)

	Using Ceramic Filter	
Halt Mode	☐	Not used
	☐	Used (Recovery with Reset)

☆ Mark "✓" in "☐" for the selected spec.

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