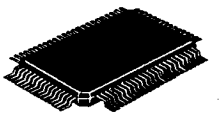
Single-Chip Digital Servo LSI

The HD49212 is a CMOS LSI chip designed for R-DAT (rotary digital audio tape) digital servos. It has the following functions and features.

- HD49212



(FP-80)

Functions

- Drum motor velocity servo, phase servo, offset servo control
- Capstan motor velocity servo, phase servo, offset servo control
- Reel motor ramp voltage control, velocity servo control
- Drum motor follow-up servo for use during high-speed searches
- ATF sync detection, tracking error detection
- FG amp, RF detector, buffer amp for motor driver
- Microprocessor interface

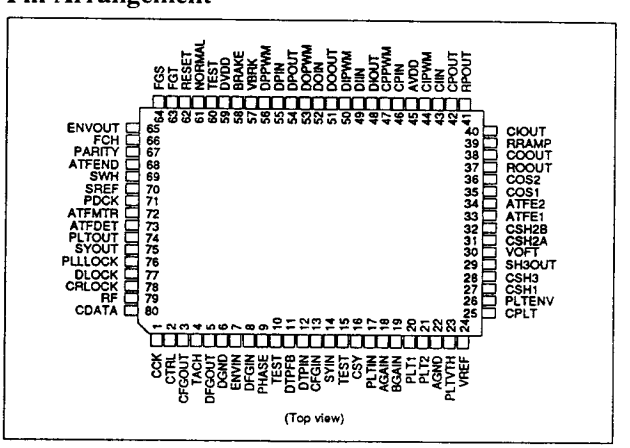
Features

- Analog portion of ATF and other circuits on-chip, allowing single-chip R-DAT servo control
- On-chip offset servo control, making adjustment unnecessary
- Variable-speed playback possible (2x, 3x, 5x, 9x, 16x)
- On-chip 16-level variable-speed high-speed search

Ordering Information

Type No.	Package
HD49212	FP-80

Pin Arrangement



Pin Descriptions

Pin no.	Pin name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
1	CCK	Microprocessor DATA CLOCK	O		Microprocessor	Microprocessor transfer data synchronizing clock input			Digital
2	CTRL	CONTROL	O		Microprocessor	Microprocessor data transfer mode control signal input			Digital
3	CFGOUT	Capstan FG output		O	Monitor	Capstan FG output			Digital
4	TACH			O	Monitor	Tach output			Digital
5	DFGOUT	Drum FG output		O	Monitor	Drum FG output			Digital
6	DGND	Digital GND	–	–	GND	Ground for digital circuitry			
7	ENVIN	Envelope input	O		External linear circuit	RF signal envelope input			Linear
8	DFGIN	Drum FG input	O		External linear circuit	Drum FG input			Linear
9	PHASE	Phase adjust	O		External linear circuit	CR interface pin for mono-multivibrator tach generation			Linear
10	TEST	Test	O		NC	Test input pin			
11	DTPFB	DTP amp feed back		O	External linear circuit	Drum tach amp output			Linear
12	DTPIN	Drum TACH pulse input	O		External linear circuit	Drum tach amp inverted input			Linear
13	CFGIN	Capstan FG input	O		External linear circuit	Capstan FG amp input			Linear
14	SYIN	Sync input	O		External linear circuit	Playback sync input			Linear
15	TEST	Test	O		NC	Test input pin			
16	CSY	C sync comparator	O		External linear circuit	Pin connection for sync-comparator threshold-voltage hold capacitor			Linear
17	PLTIN	Pilot input	O		External linear circuit	Pilot amp positive phase input pin			Linear
18	AGAIN	A-head pilot gain	O		External linear circuit	Inverted input for A-head pilot amp gain adjustment			Linear

Pin Descriptions (cont)

Pin no.	Pin name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
19	BGAIN	B-head pilot gain	○		External linear circuit	Inverted input for B-head pilot amp gain adjustment			Linear
20	PLT1	Pilot amp 1 output		○	External linear circuit	Pilot amp 1 output			Linear
21	PLT2	Pilot amp 2 input	○		External linear circuit	Pilot amp 2 input			Linear
22	AGND	Analog GND	–	–	GND	Ground for analog circuitry			Linear
23	PLTVTH	Pilot comparator threshold voltage	○		External linear circuit	Pilot comparator threshold voltage input			Linear
24	VREF	Reference voltage		○	External linear circuit	$\frac{V_{DD}}{2}$ – output			Linear
25	CPLT	C pilot detector	○		External linear circuit	Pin connection for pilot detector circuit threshold-voltage hold capacitor			Linear
26	PLTENV	Pilot envelop		○	External linear circuit	Pilot detector circuit output			Linear
27	CSH1	C sample-hold 1	○	○	External linear circuit	Pin connection for sample-hold 1 capacitor			Linear
28	CSH3	C sample-hold 3	○	○	External linear circuit	Pin connection for sample-hold 3 capacitor			Linear
29	SH3OUT	Sample-hold 3 output		○	External linear circuit	Sample-hold 3 output			Linear
30	VOFT	ATF offset voltage input	○		External linear circuit	ATF offset voltage input			Linear
31	CSH2A	C sample-hold 2A	○	○	External linear circuit	Pin connection for sample-hold 2A capacitor			Linear
32	CSH2B	C sample-hold 2B	○	○	External linear circuit	Pin connection for sample-hold 2B capacitor			Linear
33	ATFE1	ATF error amp input	○		External linear circuit	ATF error amp inverted input			Linear
34	ATFE2	ATF error amp output		○	External linear circuit	ATF error amp output			Linear
35	COS 1	C capstan offset servo 1	○	○	External linear circuit	Capstan offset servo integrater inverted input			Linear
36	COS 2	C capstan offset servo 2		○	External linear circuit	Capstan off set servo integrater output			Linear

Pin Descriptions (cont)

Pin no.	Pin name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
37	ROOUT	Reel offset servo output		O	External linear circuit	Reel offset servo control voltage buffer output			Linear
38	COOUT	Capstan offset servo output		O	External linear circuit	Capstan offset servo control voltage buffer output			Linear
39	RRAMP	Reel ramp voltage		O	External linear circuit	Reel rising ramp voltage output			Linear
40	CIOUT	Capstan I control output		O	External linear circuit	Capstan I-control voltage buffer output			Linear
41	RPOUT	Reel P control output		O	External linear circuit	Reel P-control voltage buffer output			Linear
42	CPOUT	Capstan P control output		O	External linear circuit	Capstan P-control voltage buffer output			Linear
43	CIIN	Capstan I control input	O		External linear circuit	Capstan I-control PWM low-pass filtered input			Linear
44	CIPWM	Capstan I control PWM output		O	External linear circuit	Capstan I-control PWM output			Digital
45	AV_{DD}	Analog V_{DD}	–	–	+5V	Power supply for analog circuitry			
46	CPIN	Capstan P control input	O		External linear circuit	Capstan P-control PWM low-pass filtered input			Linear
47	CPPWM	Capstan P control PWM output		O	External linear circuit	Capstan P-control PWM output			Digital
48	DIOUT	Drum I control output		O	External linear circuit	Drum I-control voltage buffer output			Linear
49	DIIN	Drum I control input	O		External linear circuit	Drum I-control PWM low-pass filtered input			Linear
50	DIPWM	Drum I control PWM output		O	External linear circuit	Drum I-control PWM output			Digital
51	DOOUT	Drum offset servo output		O	External linear circuit	Drum offset servo control voltage buffer output			Linear
52	DOIN	Drum offset servo input	O		External linear circuit	Drum offset servo PWM low-pass filtered input			Linear
53	DOPWM	Drum offset servo PWM output		O	External linear circuit	Drum offset servo PWM output			Digital
54	DPOUT	Drum P control output		O	External linear circuit	Drum P-control voltage buffer output			Linear

Pin Descriptions (cont)

Pin no.	Pin name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
55	DPIN	Drum P control input	○		External linear circuit	Drum P-control PWM low-pass filtered input			Linear
56	DPPWM	Drum P control PWM output		○	External linear circuit	Drum P-control PWM output			Digital
57	VBRK	Drum brake voltage	○		External linear circuit	Drum brake voltage input			Linear
58	BRAKE	Brake control		○	External linear circuit	Drum brake control output	Brake	Norm	Digital
59	DV_{DD}	Digital V_{DD}	–	–	+5V	Power supply for digital circuitry			
60	TEST	Test	○		Pull-up	Test input	Norm	Test	Pull up
61	NORMAL	Normal	○		Pull-up	Normal mode input	Norm	Test	Pull up
62	RESET	Reset	○		Pull-up	Reset input	Norm	RST	Pull up
63	FGT	Takeup FG	○		Reel FG	Reel FG input			Digital
64	FGS	Supply FG	○		Reel FG	Reel FG input			Digital
65	ENVOUT	Envelope output		○		Envelope comparator output			Digital
66	FCH	Channel frequency	○		HD49211	Channel clock input			Digital
67	PARITY	Parity	○		HD49211	Parity signal input			Digital
68	ATFEND	ATF end		○	HD49211	ATF end output			Digital
69	SWH	Switch head		○	HD49211 HA12133	Switch head output			Digital
70	SREF	Servo reference	○		HD49211	Servo reference input			Digital
71	PDCK	Playback data clock	○		HA12062	Playback signal synchronizing clock input			Digital
72	ATFMTR	ATF monitor		○	Monitor	Playback: ATF monitor Search: HUNT monitor			Digital
73	ATFDET	ATF detection		○	Monitor	Playback: ATF DET monitor Search: Hold monitor			Digital
74	PLTOUT	Pilot output		○	Monitor	Playback: PILOT monitor Search: DION monitor			Digital

Pin Descriptions (cont)

Pin no.	Pin name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
75	SYOUT	Sync output		○	Monitor	Playback: SYNC monitor Search: PDCK half-frequency clock monitor			Digital
76	PLLLOCK	PLL lock			Monitor	PLL lock monitor	○		Digital
77	DLOCK	Drum lock		○	Monitor	Drum lock output	○		Digital
78	CRLOCK	Capstan reel lock		○	Monitor	Capstan/reel lock output	○		Digital
79	RF	RF		○	Monitor	RF signal presence status output	○		Digital
80	CDATA	Microprocessor data input	○		Microprocessor	Microprocessor transfer data input			Digital

Functional Description

Figure 1 shows an example configuration of a system using the HD49212. The HD49212 consists of six different blocks: drum motor control block, capstan motor control block, reel motor control block, ATF control block, high-speed search control block, and microprocessor interface block.

- **Drum motor control block**

This block generates and controls fixed-speed rotation through control of velocity, phase, and offset.

- **Capstan motor control block**

This block generates and controls fixed-speed rotation through control of velocity, phase, and offset. It also performs phase control during playback through control of ATF tracking.

- **Reel motor control block**

This block uses the rotation of the capstan motor control block, and controls tape travel speed during searching.

- **ATF control block**

This block performs ATF latching control during playback. During playback, it becomes the capstan phase control.

- **High-speed search control block**

This block controls tape speed and relative velocity follow-up of drum motor rotation. It also performs hunting control.

- **Microprocessor interface block**

This block receives 24-bit mode data from the system microprocessor to control the HD49212 itself. It also decodes this mode data and transmits it to each of the other blocks.

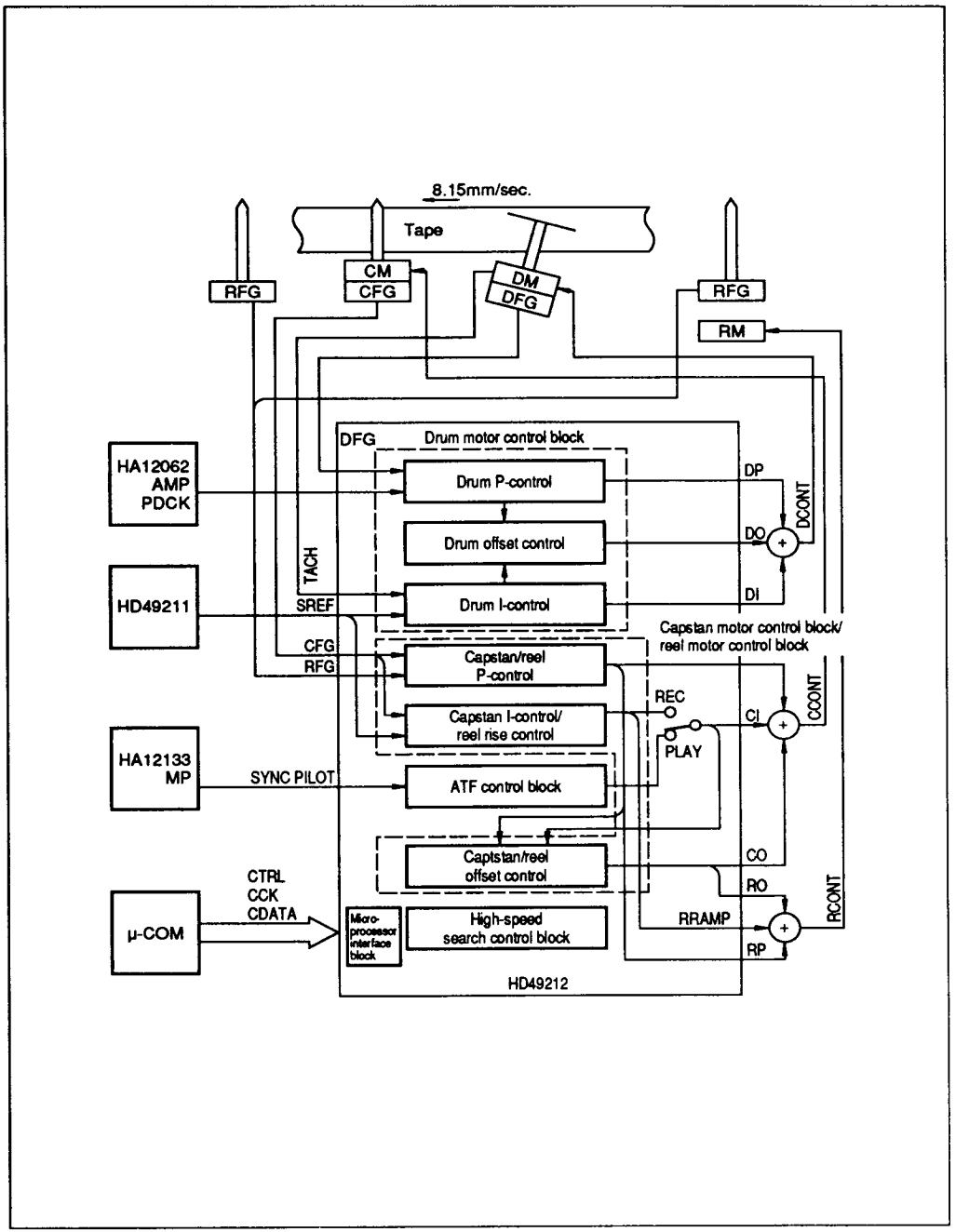


Figure 1 HD49212 System Configuration Example

Table 1 Control Modes

Control		Capstan servo		Drum servo		Reel servo
Mode		REC	PB	REC	PB	
Standard playback	SP	Velocity control: CFG Phase control: CFG SREF Offset control: Velocity / phase	Velocity control: CFG Phase control: ATF Offset control: Velocity / phase	Velocity control: DFG Phase control: TACH SREF Offset control: Velocity / phase (phase offset can be ON/OFF)	Velocity control: DFG Phase control: TACH SREF Offset control: Velocity / phase (phase offset can be ON/OFF)	
	SOFT					—
Variable -speed playback (forward and reverse)	2x speed					
	3x speed					
	5x speed					
	9x speed		Velocity control: CFG Offset control: Velocity (see Note)			
	16x speed	—		—		
High -speed searches (forward and reverse)			—		Velocity control: PDCK Offset control: Velocity	Velocity control 2FG -fixed period control 1FG -fixed rotation rate control plus reel ramp-up control Offset control: Velocity
FF/REW					:DFG Offset control: Velocity	Same as above

Note: For 9x and 16x variable speeds, ATF control will be OFF.

Table 2 Drum and Capstan Servo Parameters

Mode		Drum				Capstan			
		Velocity			Phase	Velocity			Phase
		667FG	800FG	Search		400FG	467FG	633FG	
FG frequency (sampling)	Hz	667	800	2x SWH	33.3	400	467	633	33.3
Data bits	bit	8	8	6	9	9	9	9	
PWM carrier frequency	kHz	18.375	18.375	75.5	9.188	9.188	9.188	9.188	9.188
Detection range ±ΔP	%	3.63	4.35	25	2.9	17.4	20.3	27.6	5.8
KP	mV/rad/sec V/rad	16.45	11.42	0.0433	13.7	5.71	4.2	2.28	6.85

Table 3 Drum Offset Servo Parameters

Mode		Velocity	Phase	Search FWD	Search REV
Main loop bits	bits	8	9	6	6
Data shift	bits	–2	–2	+2	+3
Data bits	bits	12	12	12	12
Servo bandwidth	Hz	1.66	0.166	1.0	0.64
PWM carrier frequency	kHz	1.148	1.148	1.148	1.148

Table 4 Capstan Velocity Gain Control

Mode	SP						SOFT					
Traveling velocity	×1	×2	×3	×5	×9	×16	×1	×2	×3	×5	×9	×16
Gain after control	1	1	2/3	4/5	4/9	1/16	2/3	2/3	8/9	8/15	8/27	1/6
Carrier frequency	A	B	B	C	C	C	A	B	C	C	C	C

A = 9.1875 kHz B = 18.375 kHz C = 36.75 kHz

Microprocessor Interface Block

Block Overview

The microprocessor interface block receives and decodes the mode data from the microprocessor. It then transmits the decoded signals to each of the blocks as control signals.

Functional Description

Microprocessor interface pin functions

The HD49212 and the microprocessor interface with each other through three pins: CCK, CTRL and CDATA. The signal lines to these three pins are also used be the signal processing LSI (HD49211). Taking the CTRL pin to "H" at the start and end of communications will control the selection or non-selection of the HD49212, and will allow for the transfer of each word of data (8 bits).

Table 5 Transfer for Mode Changes

Changed positions	Transfer format
1-8 bit	Can be changed with a 1-word transfer
9-16 bit	Can be changed with a 2-word transfer
17-24 bit	Can be changed with a 3-word transfer

Mode data transfer timing

Mode data transfer timing is shown is Figure 3. When transferring a mode setting, first set the CTRL line to "H", and then transfer one data word. Then, by making the final CDATA bit is "H", the HD49212 servo LSI is selected and the HD49212 will take the data to follow.

During initialization, three words of mode data must be transferred, but after that the mode can be changed by transferring only the necessary number of words. Thus, for a 12-bit mode change, it is possible to change the mode by transferring two words (16 bits).

For all transfers, whether 1, 2, or 3 words, after the final word is sent CTRL must be brought to "H", and 8 bits of data with the MSB "L" must be transferred.

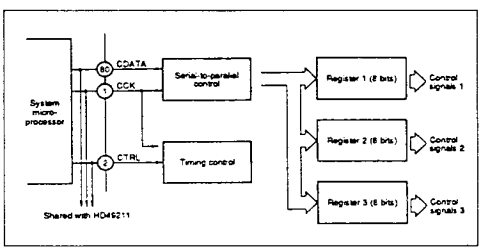


Figure 2 Microprocessor Interface Block Diagram

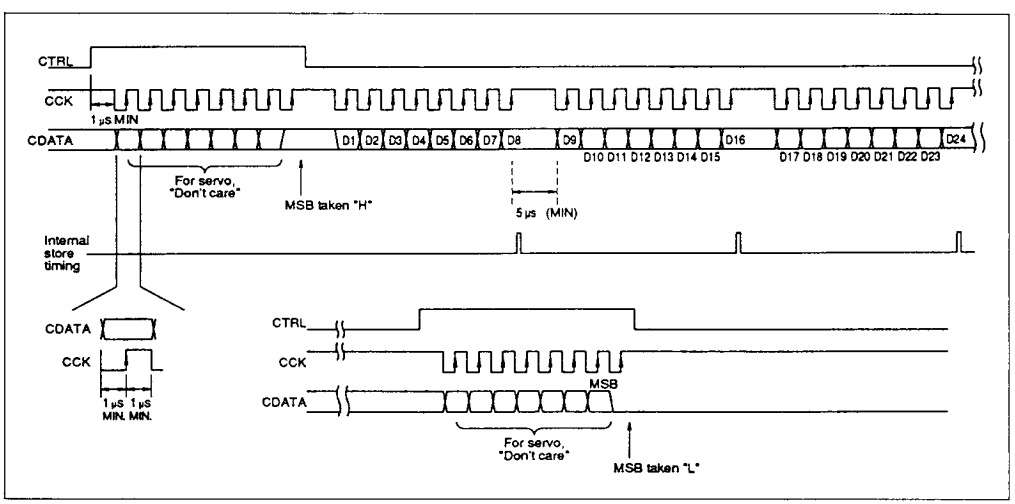


Figure 3 Mode Data Transfer Timing

Mode data specifications

Table 6 shows all mode data specifications.

- **ATF (bit D1)**

This bit performs on/off ATF control during playback.

ATF = "H": ATF ON
"L": ATF OFF

Also, when ATF, REV, and VR1-3 are all "L", the REC servo and capstan motor phase control are initiated.

- **DON (bit D2)**

This bit performs on/off drum motor control.

DON = "H": Drum motor control ON
"L": Drum motor control OFF

Also, when DON is "L", the output pins DPPWM, DIPWM, DOPWM, DTOUT, DIOUT, and DOOUT all become "L" too.

- **CON (bit D3)**

This bit performs on/off capstan motor control.

CON = "H" : Capstan motor control ON
"L" : Capstan motor control OFF

Also, when CON is "L", the output pins CPPWM, CIPWM, COOUT, CPOUT and CIOUT all become "L" too. However, if reel motor control is on (RON = "L") then CPPWM and CIPWM become reel motor control pulse outputs.

- **RON (bit D4)**

This bit performs on/off reel motor control.

RON = "H" : Reel motor control ON
"L" : Reel motor control OFF

Also, when RON is "L", the output pins CPPWM, RRAMP, CIPWM, RPOUT, and ROOUT all become "L" too. However, if capstan motor control is on (CON = "L") then CPPWM and CIPWM become capstan motor control pulse outputs.

Table 6 Mode Data Specifications

Data	Signal name	Mode
D1	ATF	H: ATF control ON
D2	DON	H: Drum motor ON
D3	CON	H: Cap. motor ON
D4	RON	H: Reel motor ON
D5	VR1	
D6	VR2	
D7	VR3	
D8	REV	H: Reverse
D9	TSD1	Reel servo tape speed data
D10	TSD2	Reel servo tape speed data

D5	D6	D7	Mode
0	0	0	x1
1	0	0	x2
0	1	0	x3
1	1	0	x5
0	0	1	x9
1	0	1	x16
0	1	1	FF/REW
1	1	1	Search

Mode Data Specifications (cont)

Data	Signal name	Mode	
D11	TSD3	Reel servo tape speed data	During playback - H: With drum offset servo L: Without drum offset servo
D12	TSPD	H: ×100 servo L: ×200 servo	Also functions as ATF pilot amp 2 gain switch H: 26 dB L: 20 dB
D13	TP	H: 1.5 TP tape (soft tape)	
D14	OFT	H: Offset on	
D15	PROT	H: Protect on	
D16	TEST	H: Use prohibited	L: Normal
D17	CFS1	Cap. FG select	
D18	CFS2	Cap. FG select	

D17	D18	CFG freq.
0	0	400 Hz
1	0	466.6 Hz
0	1	633.3 Hz
1	1	—

Data	Signal name	Mode	
D19	DFS	H: 800 Hz	L: 666.6 Hz
D20	RFS	H: 1 reel FG.	L: 2 reel FG.
D21	RTM1	Rise time	
D22	RTM2	Rise time	

D21	D22	Voltage ramp rate
0	0	2.8 V/sec
1	0	1.4 V/sec
0	1	0.7 V/sec
1	1	0.35 V/sec

Data	Signal name	Mode	
D23	GATE	H: ATF Gate on	Set gate to "H" during searching
D24	REAR	H: ATF 2 select (however, changes with each variable-speed mode)	

• **VR1, VR2, VR3 (bits D5, D6, D7)**

These bits perform both speed control of variable-speed playback and mode settings of reel motor control.

• **REV (bit D8)**

This bit sets the forward/reverse mode.

REV = "H": Reverse
"L": Forward

Further, when REV is "H", all speed/modes set by VR1, VR2 and VR3 will become reverse modes (ATF error voltage polarity will reverse, FF/REW mode will become REW, and high-speed search will become REW search).
Also, from the microprocessor change the capstan and reel motor rotation direction through the motor driver control pin.

• **TSD1, TSD2, TSD3 (bits D9, D10, D11)**

(a) FF/REW and search modes

These bits set the reel motor FG period for reel motor control. Table 8 shows the two-reel FG periods for TSD1, TSD2 and TSD3 (detection range values).

(b) Other than FF/REW and search modes
REC, PLAY

* TSD2 (bit D10)

This bit forces the ATFLK signal to "H", ignoring the SYNC detection status.

TSD2 = "H": Forces ATFLK to "H".
"L": Generates ATFLK as basis for SYNC detection status.

Set TSD2 to "H" only during special tape playback for adjustment; otherwise, set it to "L".

* TSD3 (bit D11)

This bit performs on/off drum phase offset control.

TSD3 = "H": Drum phase offset control ON
"L": Drum phase offset control OFF (becomes velocity offset control only)

• **TSPD (bit D12)**

This bit is the gain switch for ATF pilot amp 2, which controls tape travel velocity for reel motor FF/REW and search modes, and controls the capstan motor for PLAY mode.

Table 7 Variable-Speed Playback Speed Control and Reel Motor Control Mode Settings

Mode data				
VR1	VR2	VR3	Speed / mode	Control type
0	0	0	1x speed	Variable-speed playback
1	0	0	2x speed	Capstan motor control
0	1	0	3x speed	
1	1	0	5x speed	
0	0	1	9x speed	
1	0	1	16x speed	
0	1	1	FF/REW	Reel motor control
1	1	1	High-speed search	

• **TP (bit D13)**

This bit sets the 1.5 track pitch soft tape mode.

TP = "H": Soft tape
"L": NORMAL tape

• **OFT (bit D14)**

This bit performs on/off control of external offset during ATF tracking.

OFT = "H": Adds offset voltage of VOFT pin as ATF tracking offset.
"L": No offset during ATF tracking.

• **PROT (bit D15)**

This bit performs on/off control of the ATF SYNC misdetection protection circuit.

PROT= "H": Misdetection protection circuit ON
"L": Misdetection protection circuit OFF

The ATF SYNC misdetection protection circuit prevents the misdetection of SYNC signals left over from previous recordings on an overwritten tape, allowing correct SYNC signals to be detected. During normal operation this circuit is ON, but during special tape playback for adjustment only this circuit is taken OFF.

• **TEST (bit D16)**

This bit is for chip test purposes only, so it should be tied permanently to "L".

TEST = "H": Use prohibited (TEST mode)
"L": Normal operation

• **CFS1, CFS2 (bits D17, D18)**

These bits select the capstan motor FG frequency.

• **DFS (bit D19)**

This bit selects the drum motor FG frequency.

DFS = "H": FG is 800 Hz
"L": FG is 666.6 Hz

• **RFS (bit D20)**

This bit selects the reel motor FG moe.

RFS = "L": 2-reel FG mode
(Controls the dual-reel FG periods for the FG mechanism (8 pulses/rotation) set up on both reel shafts)
"H": 1-reel FG mode
(Controls the single-reel FG rotations for the FG mechanism (8 pulses/rotation) set up on one reel shaft only)

• **RTM1, RTM2 (bits D21, D22)**

These bits select the voltage ramp rate after reel rotation has started for high-speed searching. Before starting reel rotation, the ramp voltage is fixed at 5.6 V/sec. Reel rotation is considered to have begun when one reel pulse is then detected.

Table 8 Reel Period of Reel Motor Control (2-reel FG mode)

Mode data			200x-speed reel control	100x-speed reel control
TSD1	TSD2	TSD3	TSPD = "L"	TSPD = "H"
0	0	0	13.93 ms	27.86 ms
1	0	0	13.06 ms	26.12 ms
0	1	0	12.19 ms	24.38 ms
1	1	0	11.32 ms	22.64 ms
0	0	1	10.45 ms	20.90 ms

Reel Period of Reel Motor Control (2-reel FG mode) (cont)

Mode data			200x-speed reel control	100x-speed reel control
TSD1	TSD2	TSD3	TSPD = "L"	TSPD = "H"
1	0	1	9.58 ms	19.16 ms
0	1	1	8.71 ms	17.42 ms
1	1	1	7.84 ms	15.68 ms

Table 9 TSPD Mode Data Specification

Mode data		
TSPD	Reel motor control	Capstan motor control
0	200x speed	Pilot amp 2 gain 20 dB
1	100x speed	Pilot amp 2 gain 26 dB

Table 10 CFG Frequency Specifications

Mode data		
CFS1	CFS2	CFG frequency
0	0	400 Hz
1	0	466.6 Hz
0	1	633.3 Hz
1	1	Use prohibited

Table 11 Reel Motor Rising Voltage Ramp Rate Specifications

Mode data		
RTM1	RTM2	Voltage ramp rate
0	0	2.8 V/sec
1	0	1.4 V/sec
0	1	0.7 V/sec
1	1	0.35 V/sec

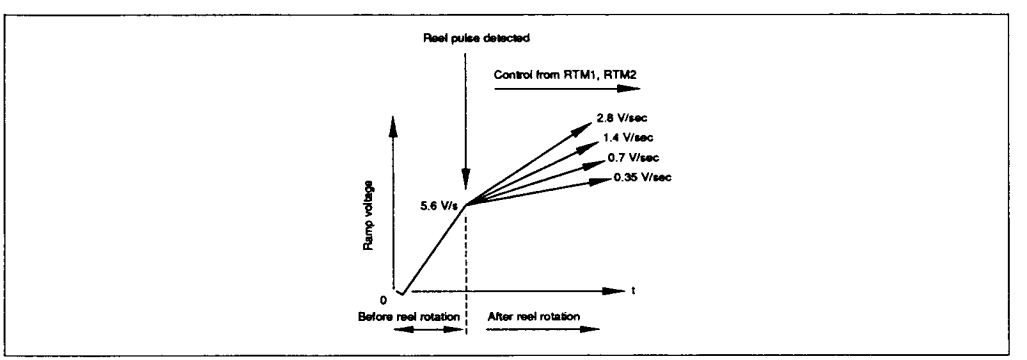


Figure 4 Reel Motor Ramp up Characteristics

• **GATE (bit D23)**

(a) Playback mode

This bit performs on/off control of the ATF gate. During ATF tracking, the ATF gate signal opens a window for the ATF area only, allowing ATF detection to be performed. This signal prevents erroneous detection when noise is generated outside the ATF area at harmonics of the ATF frequency.

GATE = "H" : ATF gate ON
"L" : ATF gate OFF

The ATF gate is normally used ON. It is OFF only during special tape playback for adjustment.

(b) Search mode

Selects drum offset control hold/reset during hunting.

GATE = "H" : Drum offset voltage hold
"L" : Drum offset voltage reset

During normal operation the drum offset voltage should be held with GATE="H".

• **REAR (bit D24)**

This bit allows selection of ATF area 1 or 2 for ATF tracking during variable-speed playback. Table 12 shows the ATF area contents selected by REAR. During normal operation REAR is "L".

Table 12 ATF Areas Selected by REAR

(a) Rear = "L"

SPEED	FORWARD AREA		REVERSE AREA	
x1	A1	A2	A1	—
	B1	B2	B1	—
x2	—	A2	—	A2
	(B1)	—	(B1)	—
x3	A1	—	A1	—
	B1	—	B1	—
x5	A1	—	A1	—
	B1	—	B1	—
x9	A1	—	A1	—
	B1	—	B1	—
x16	—	A2	—	A2
	(B1)	—	(B1)	—

(b) Rear = "H"

SPEED	FORWARD AREA		REVERSE AREA	
x1	—	A2	—	A2
	—	B2	—	B2
x2	A1	—	A1	—
	—	(B2)	—	(B2)
x3	—	A2	—	A2
	—	B2	—	B2
x5	—	A2	—	A2
	—	B2	—	B2
x9	—	A2	—	A2
	—	B2	—	B2
x16	A1	—	A1	—
	—	(B2)	—	(B2)

Notes: 1. A1 : A-track ATF 1
A2 : A-track ATF 2
B1 : B-track ATF 1
B2 : B-track ATF 2

2. Parentheses "( )" indicates selection when playback with one of the heads becomes impossible.

Drum Motor Control Block

Block Overview

This block performs three types of servo control for drum motors: velocity control, phase control, and offset control. Figure 5 shows a block diagram and Figure 6 shows a flowchart of drum motor control.

- **Velocity control**

A counter measures the DFG signal period generated by the drum motor. The DFG period is latched as 8-bit error data. By comparing this data to a reference data value, a PWM signal is generated. This PWM signal is fed back to the drum motor through an external low-pass filter and an on-chip amp, thereby regulating the drum motor to a fixed number of rotations.

- **Phase control**

Phases are compared between the DTP signal (33.3 Hz) generated by pulses from the drum motor rotation and the SREF signal (33.3 Hz) input from the HD49211 signal processing LSI. This phase difference is latched as 9-bit error data, which is used to generate a PWM signal. This PWM signal is fed back to the drum motor through an external low-pass filter and an on-chip amp, thereby regulating the drum motor to a fixed phase difference.

- **Offset control**

This type of control controls velocity offset and phase offset. For velocity offset, until the upper 6 bits of the velocity error data are locked to a detection range center value, they are integrated and fed back to the drum motor. For phase offset, the upper 7 bits of the phase error data are integrated and fed back to the drum motor. Phase offset control can be turned on and off by the microprocessor through mode data TSD3.

Block Function

Velocity control

- **DFG amp**

The DFG signal is input through the DFGIN pin and then amplified with the on-chip DFG amp. It is then passed through a comparator and converted to a logic signal. The gain of the DFG amp is typically 20 dB.

- **DFG monitor**

The waveshaped DFG signal can be monitored from the DFGOUT pin.

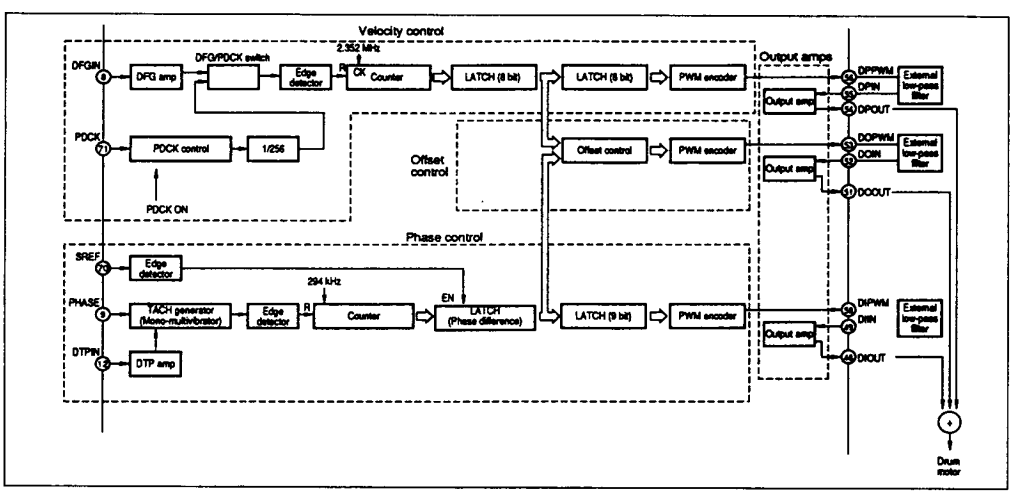


Figure 5 Drum Motor Control Block Diagram

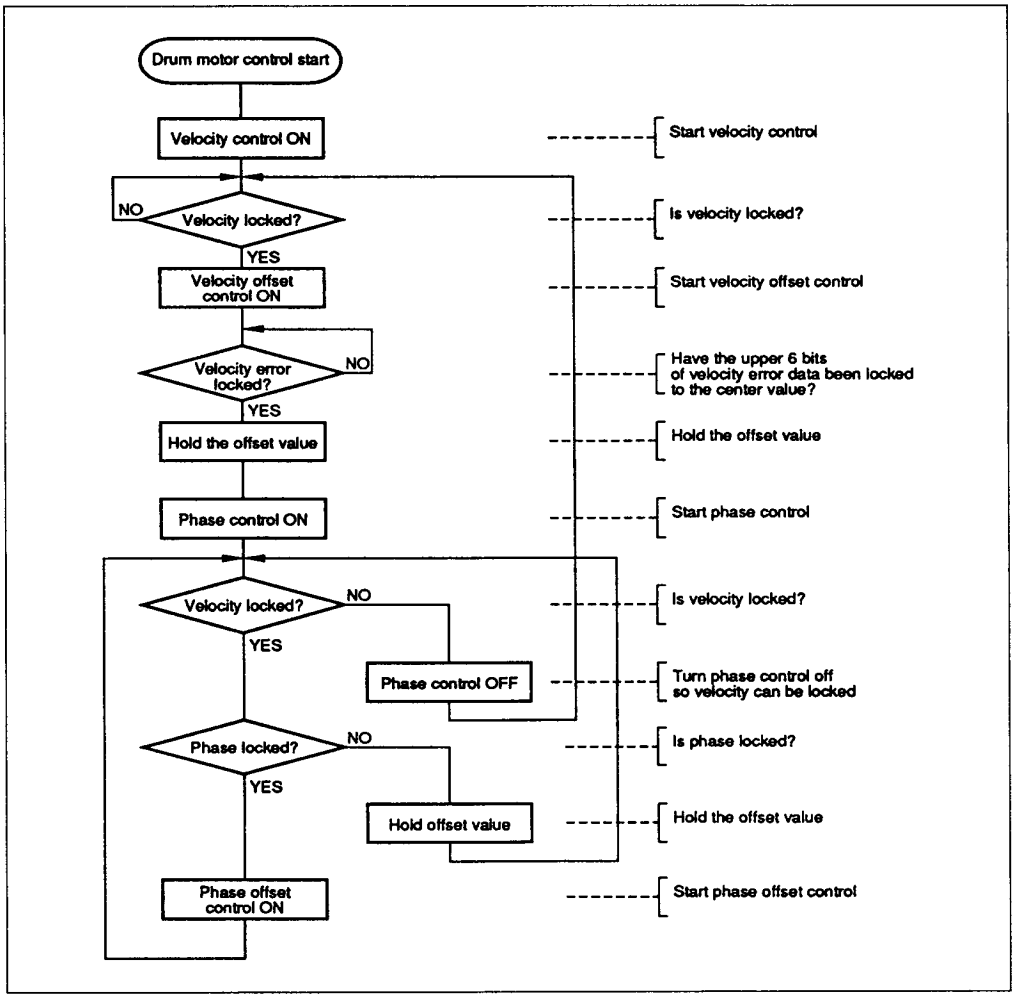


Figure 6 Drum Motor Control Flowchart

- **Detection range control, PWM signal generation**

DFG signal periods are counted with a 2.352 MHz clock. The upper 8 bits of the count are latched as error data. If that value is in the detection range, it is used to generate a PWM signal.

If the periods are shorter than the detection range, the PWM output will be fixed at a "L" level. If the periods are longer, the PWM output will fixed at an "H" level. (Refer to table 13.)

Phase control

- **DTP amp**

The DTP signal is input through the DTPIN pin and then amplified with the on-chip DTP amp 1 and DTP amp 2. It is then passed through a comparator and converted to a logic signal. The gain of DTP amp 1 is set in the range of 0 – 40 dB to match with the output level of the drum motor DTP sensor. DTP amp 2 is an inverting amplifier with a gain of 0 dB.

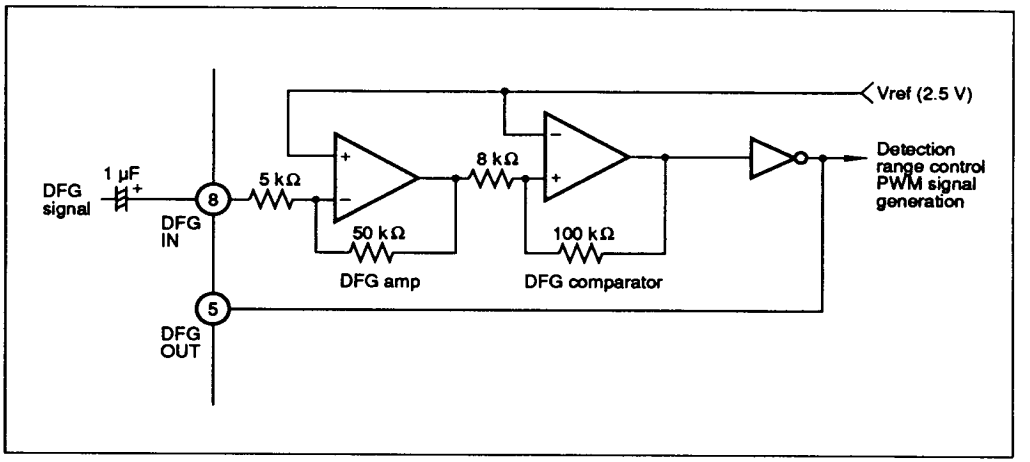


Figure 7 DFG Amplifier Circuit

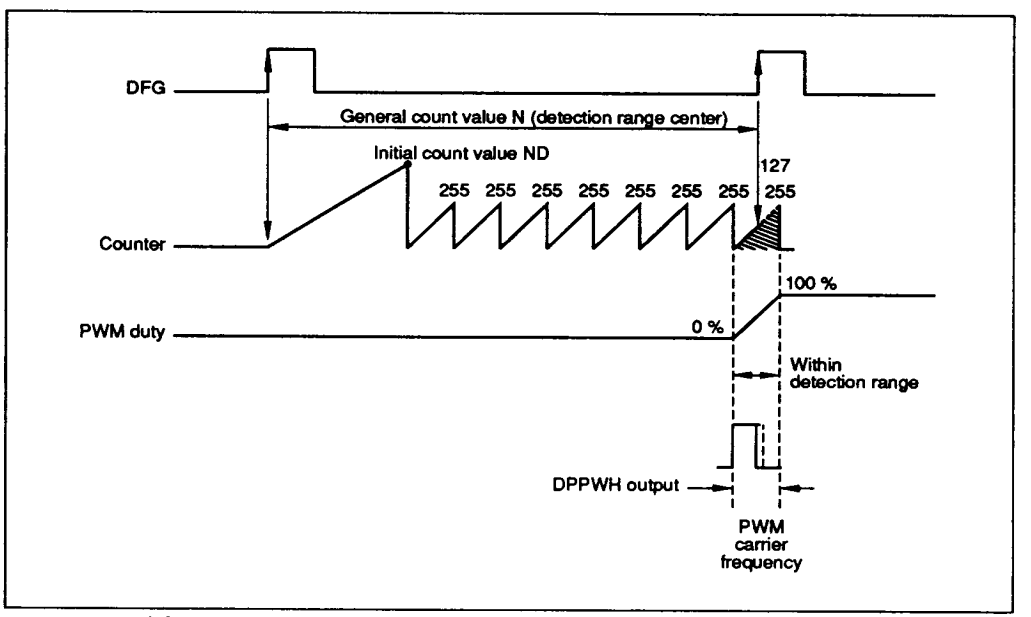


Figure 8 Detection Range for Drum Motor Velocity Control

- **TACH generation circuit**

The TACH generating mono-multivibrator is configured using the amplified DTP logic signal and the external RC time constant on the PHASE pin. Figure 10 shows a circuit diagram of the mono-multivibrator and figure 11 shows TACH generation timing.

When this circuit detects the DTP signal rising, it triggers the TACH generation circuit and turns CSW to OFF. Then the voltage on the PHASE pin gradually begins to rise according to the external RC time constant. When the Vref voltage (2.5 V typ) is exceeded, the TACH comparator inverts, CSW turns ON, and the previously charged C1 discharges.

In this manner, the TACH signal pulse width is determined by the external RC time constant. The TACH signal is output on the TACH pin. The falling of the TACH signal is the reference position during recording so by varying the RC time constant, the recording position can be adjusted.

The resistance R for determining the time constant should be at least 100 kΩ.

- **SWH signal generation**

(a) Normal mode

In normal mode, when drum motor rotation is 2000 rpm (record and playback modes), a normal SWH (Switch Head) signal is generated. The fallings of the SWH and TACH signals occur together. This becomes the recording signal output reference for the HD49211 signal processing LSI.

(b) FF/REW/Search mode

In these modes, when drum motor rotation is between 700 – 3300 rpm, a variable rotation SWH (Switch Head) signal is output. The falling of the SWH signal and the rising of the TACH signal occur together.

- **Detection range control, PWM signal generation**

For phase control, the phase difference between the TACH signal and the SREF signal (33.3 Hz) from the HD49211 signal processing LSI will be latched as 9-bit error data. If the phase difference is within the detection range shown below, a PWM signal will be generated using the error data. If it is outside of the detection range, then depending on the difference the PWM output will be fixed at "H" or "L".

Table 13 Detection Range Parameters for Drum Motor Velocity Control

	Mode	
Item	**I**	**II**
DFG frequency	667 Hz	800 Hz
Counter clock frequency	2.352 MHz	2.352 MHz
PWM carrier frequency	18.375 kHz	18.375 MHz
Detection range	±3.63 %	±4.35 %
Detection sensitivity	16.45 mV/rad/sec	11.42 mV/rad/sec
Initial count value ND	1608	1020
General count value N	3528	2940

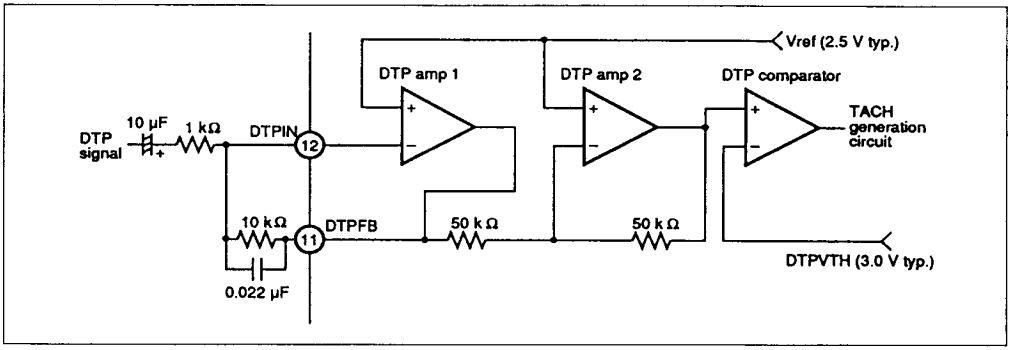


Figure 9 DTP Amplifier Circuit

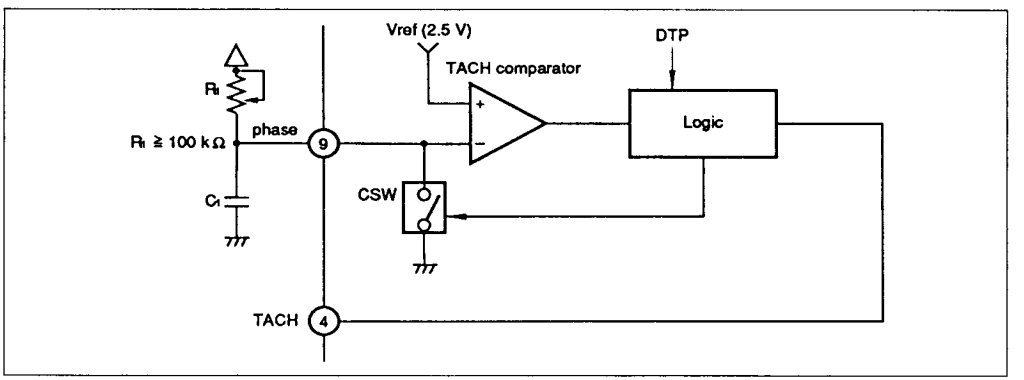


Figure 10 TACH Generation Circuit

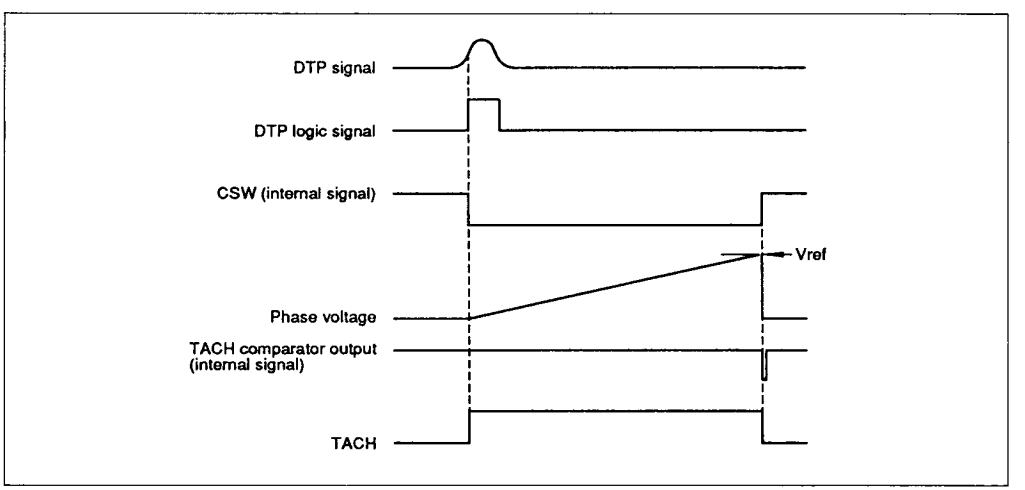


Figure 11 TACH Generation Timing

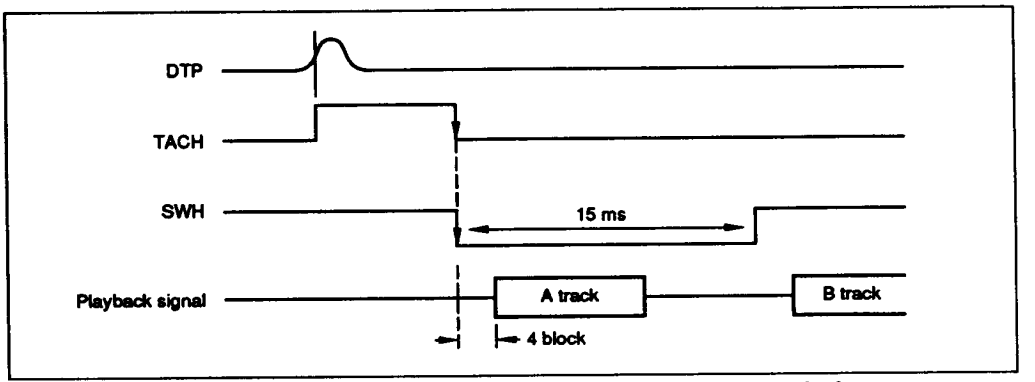


Figure 12 FF/REW/Search Mode SWH Generation Timing

Offset control

- **Velocity offset control**

Error data from drum motor velocity control is corrected such that it approaches a center vlaue.

The upper 6 bits of the 8-bit error data are detected, and when it matches the center value 20H or 1FH for 127 times, the error data is considered locked on the center value, and velocity offset control ends.(Refer to table 15.)

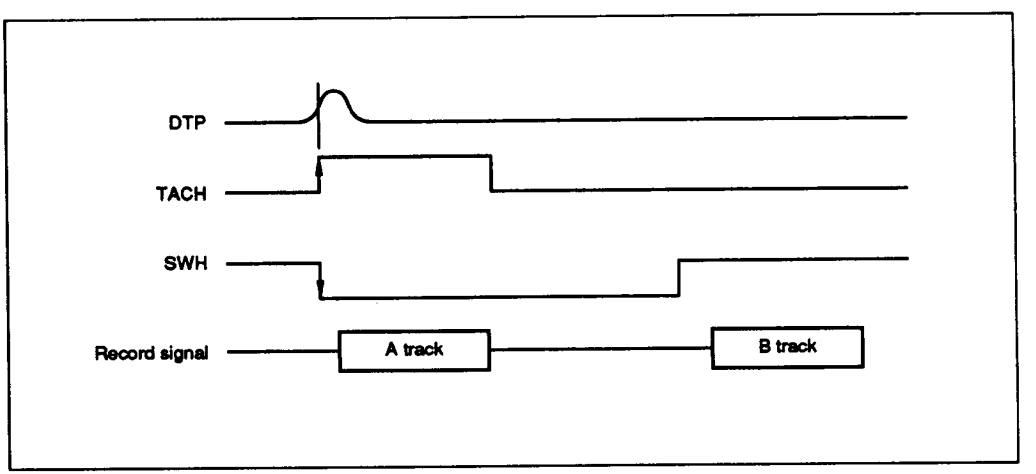


Figure 13 Normal Mode SWH Generation Timing

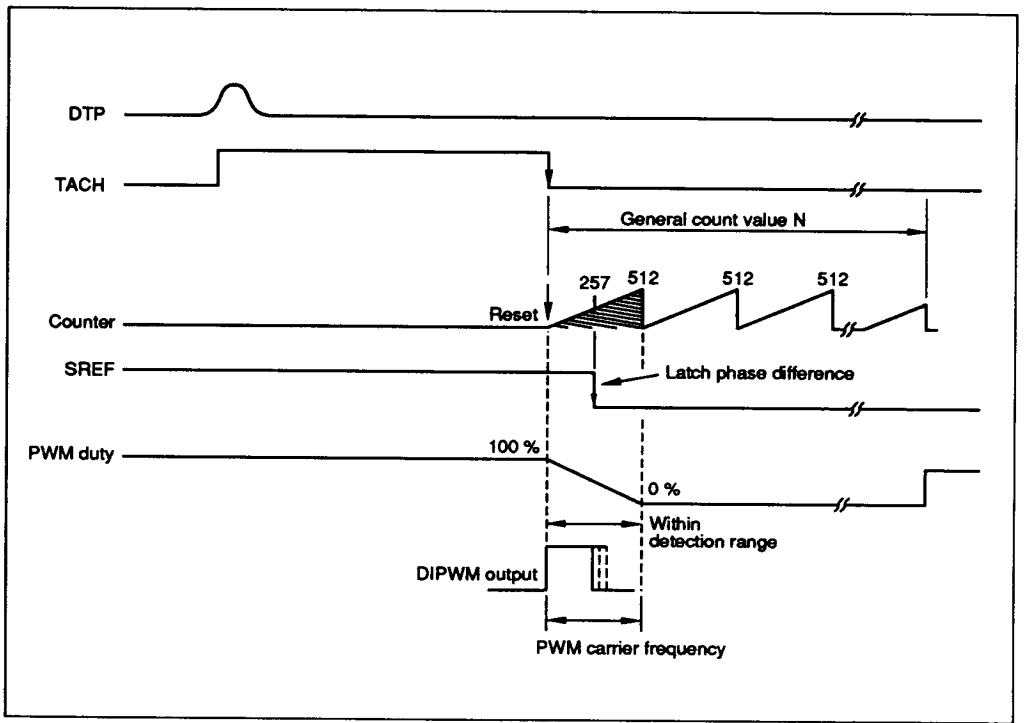


Figure 14 Detection Range for Drum Motor Phase Control

- **Phase offset control**

Drum motor steady-state phase error, which fluctuates depending on load and temperature, is corrected. The upper 7 bits of the 9-bit drum motor phase control error data are corrected such that they approach the center and are added to the offset.

Phase offset control can be turned on and off by the microprocessor mode data TSD3 (bit D11).(Refer to table 16.)

Output amplifier circuits

The HD49212 has output buffer amps on-chip for each control type: velocity control, and offset control. As shown in Figure 17, each of the PWM outputs is smoothed by a low-pass filter and then connected to an on-chip amp. The outputs of the on-chip amps can directly sent to a resistor adder.

Table 14 Detection Range Parameters for Drum Motor Phase Control

Item	Normal mode
Sampling frequency	33.3 Hz
Counter clock frequency	294 kHz
PWM carrier frequency	9.1875 kHz
Detection range	±2.9 %
Detection sensitivity	13.71 V/rad
General count value N	4410

Table 15 Offset Servo Bandwidths

FG frequency	Offset servo bandwidth
667 Hz	1.7 Hz
800 Hz	2.0 Hz

Note: Bandwidths for when the added gains of velocity error voltage and offset error voltage are equal.

Table 16 Offset Servo Bandwidth

Bandwidth	0.2 Hz

Note: Bandwidths for when the added gains of phase error voltage and offset error voltage are equal.

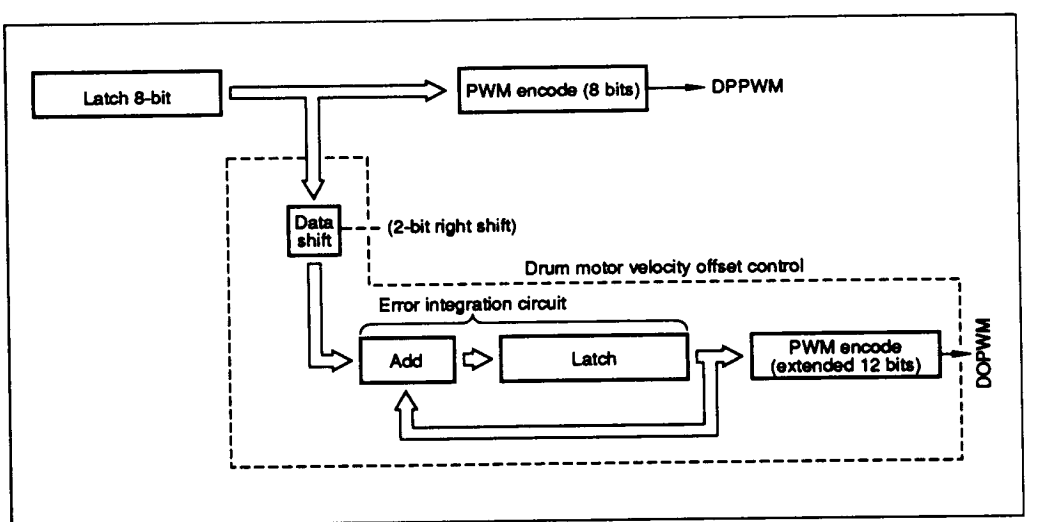


Figure 15 Drum Motor Velocity Offset Control Circuit

Drum motor lock signal

Drum motor control status can be monitored from the DLOCK pin. Table 17 shows DLOCK output conditions.

Table 17 DLOCK Output Conditions

Mode	Output conditions for DLOCK = "H" (CLOCK = "L" under all other conditions) (Notes)
REC, PLAY	DPLK • DILK • $\overline{\text{DOA}}$ • DON
FF/REW, Search	DPLK • $\overline{\text{DOA}}$ • DON

Notes: 1. DPLK (drum velocity lock signal):
Set to "H" if the drum velocity error data is within the detection range.
2. DILK (drum phase lock signal):
Set to "H" if drum phase error data is within the detection range.
3. DOA (drum offset value overflow signal):
Set to "H" if the offset value overflows.
4. DON (drum ON signal):
Mode data signal from microprocessor. Set to "H" when drum motor is ON.

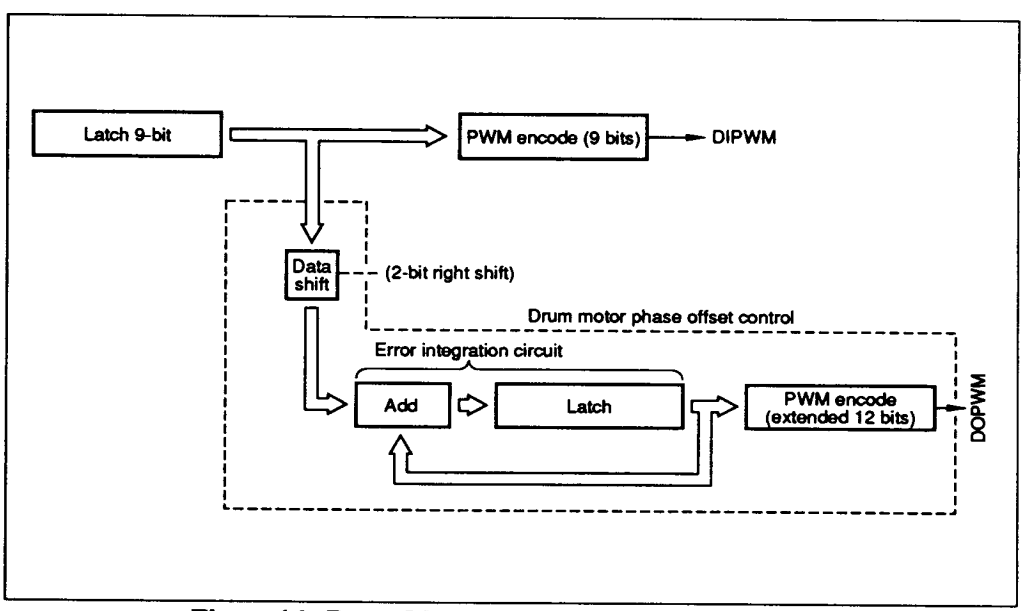


Figure 16 Drum Motor Phase Offset Control Circuit

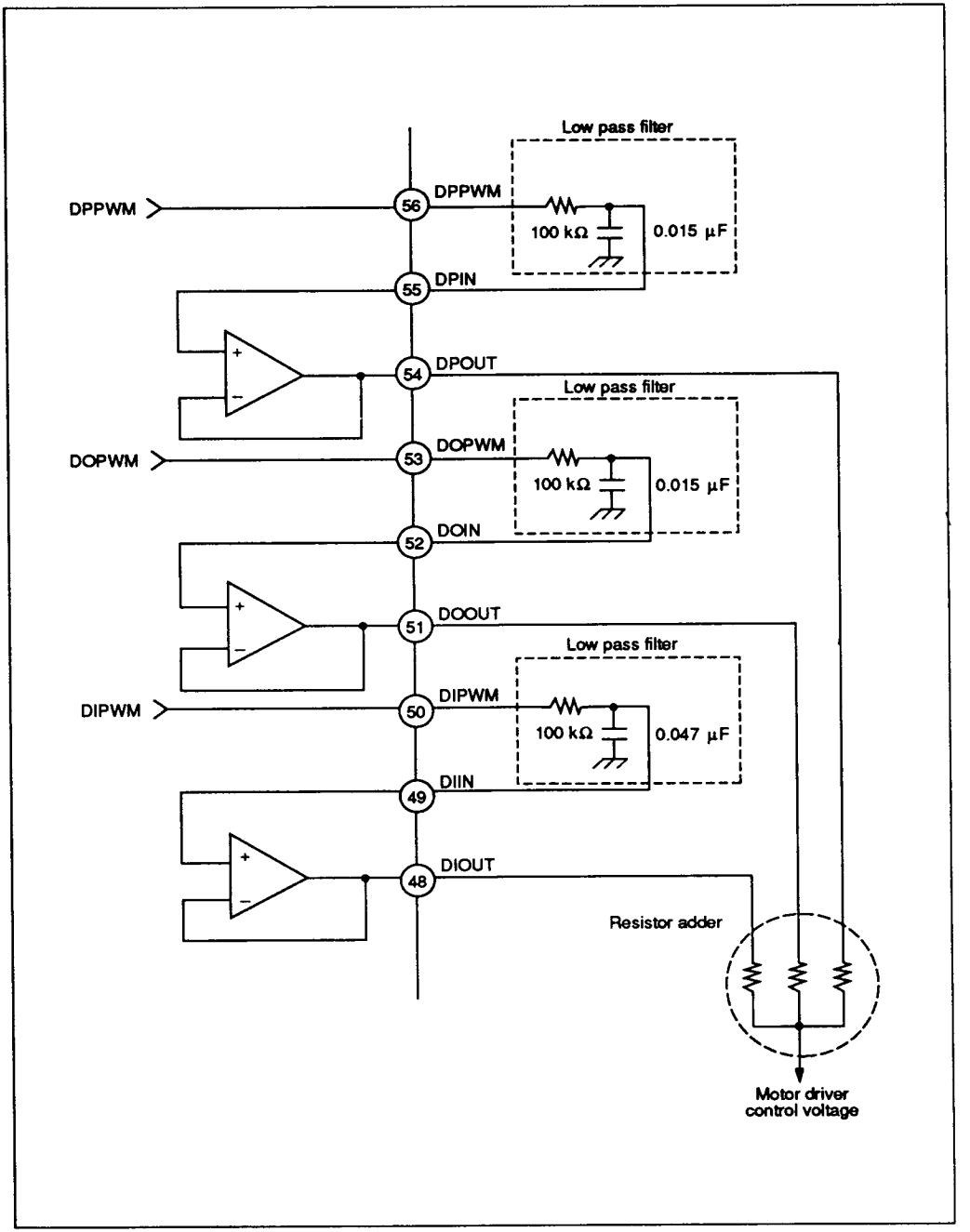


Figure 17 Drum Motor Control Output Amplifier Configuration

Capstan Motor Control Block

Block Overview

This block performs three types of servo control for capstan motors: Velocity control, phase control, and offset control. Figure 18 shows a block diagram and figure 19 shows a flowchart of drum motor control.

- **Velocity control**

A counter measures CFG signal period generated by the capstan motor. The CFG period is latched as 9-bit error data. By comparing this data to a reference data value, a PWM signal is generated. This PWM signal is fed back to the drum motor through an external low-pass filter and an on-chip amp, thereby regulating the drum motor to a fixed number of rotations.

- **Phase control**

Phase control for capstan motors operates only during recording; during playback a 50 % duty PWM signal is output from CIPWM. Phases are compared between the 33.3 Hz signal from frequency dividing the CFG signal and the SREF signal (33.3 Hz) input from the HD49211 signal processing LSI. This phase difference is latched as 9-bit error data, which is used to generate a PWM signal. This PWM signal is fed back to the drum motor through an external low-pass filter and an on-chip amp, thereby regulating the drum motor to a fixed phase difference.

- **Offset control**

This type of control controls velocity offset and phase offset. For velocity offset, until the upper 5 bits of the velocity error data are locked to a detection range center value, the error signal output on the CPOUT pin is integrated by a linear offset circuit and output on the COOUT pin. For phase offset, the error signal output on the CIOUT pin is integrated by a linear offset circuit and fed back to the capstan motor.

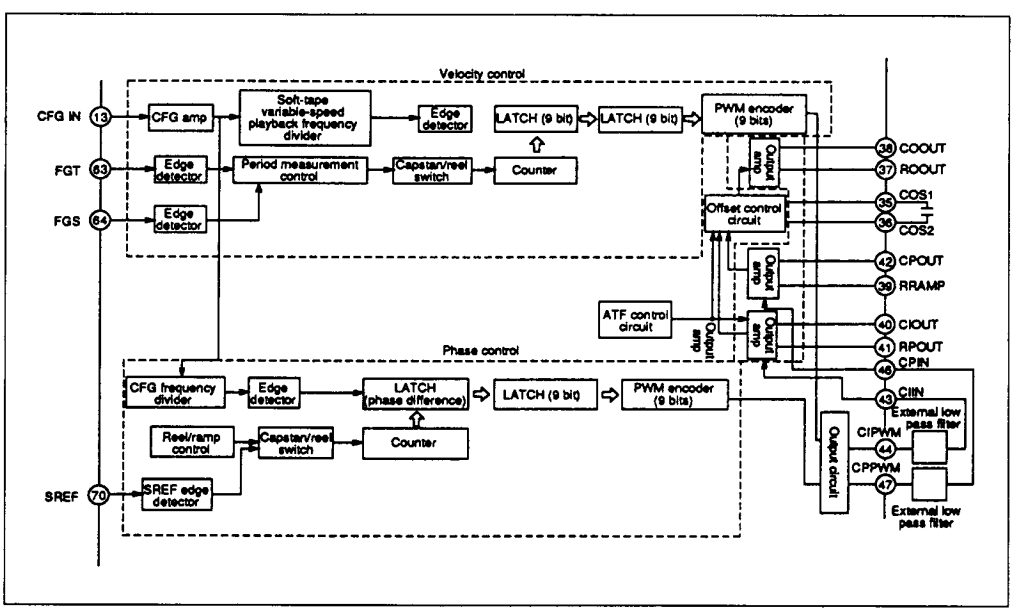


Figure 18 Capstan Motor/Reel Motor Control Block Diagram

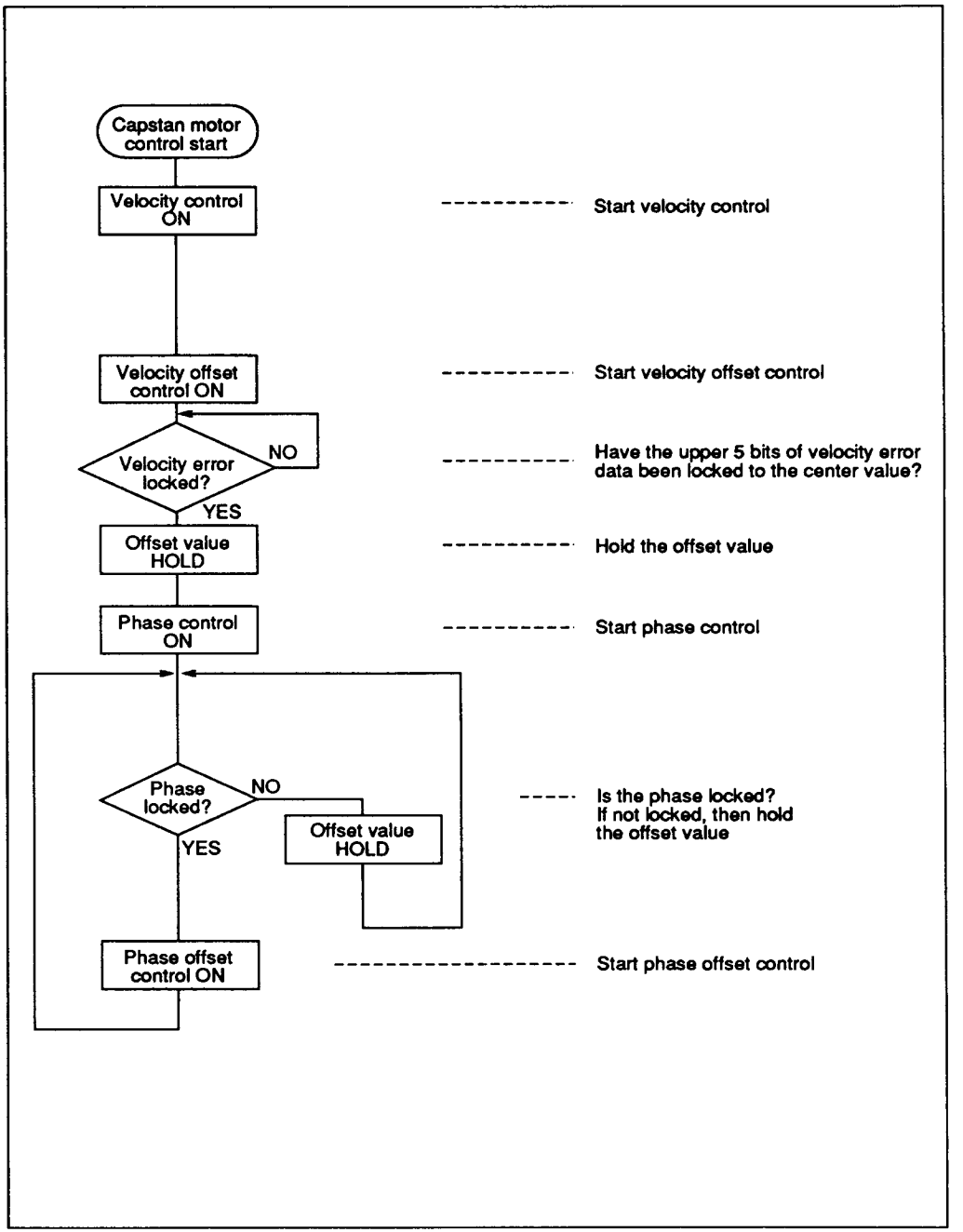


Figure 19 Capstan Motor Control Flowchart

Block Function

Velocity control

- **CFG amp**

The CFG signal is input from the CFGIN pin and amplified by the on-chip CFG amp. It is then passed through a comparator and converted to a logic signal. Gain of the CFG amp is typically 20 dB.

- **CFG monitor**

The wave-shaped CFG signal can be monitored from the CFGOUT pin.

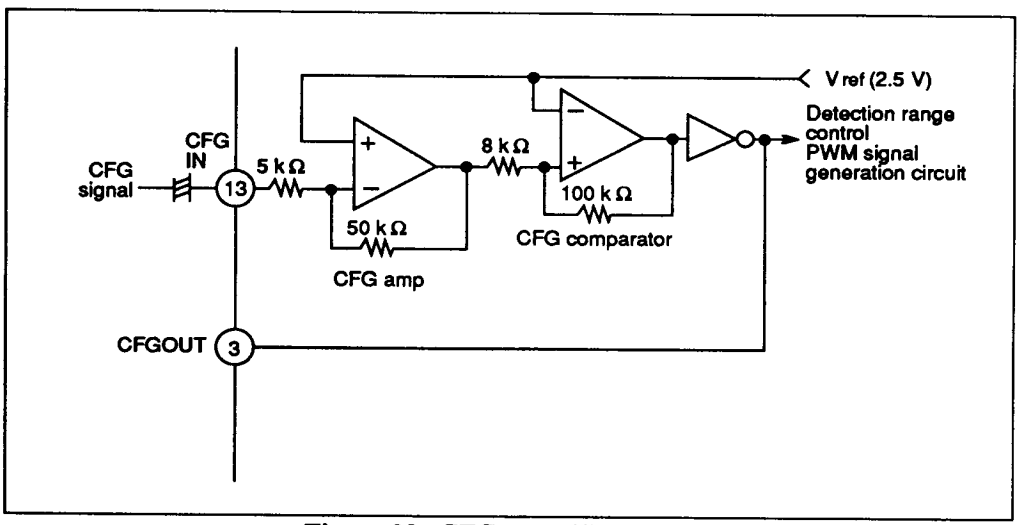


Figure 20 CFG Amplifier Circuit

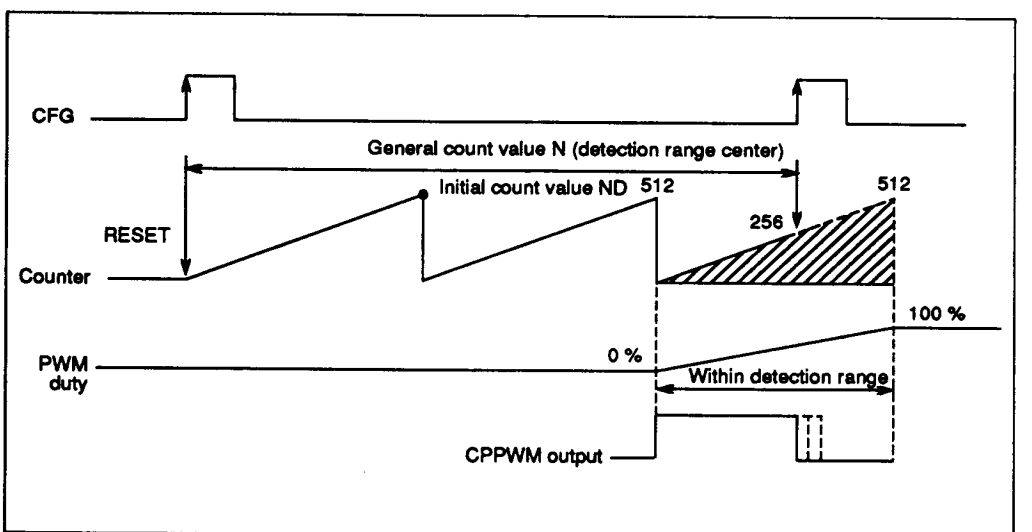


Figure 21 Detection Range for Capstan Motor Velocity Control

- **Detection range control, PWM signal generation**

CFG signal periods are counted with a 588 kHz clock. The upper 9 bits of the count are latched as error data. If that value is in the detection range, it is used to generate a PWM signal.

If the periods are shorter than the detection range, the PWM output will be fixed at a "L" level. If the periods are longer, the PWM output will fixed at an "H" level.

Phase control

- **Detection range control, PWM signal generation**

For phase control, the CFG signal waveshaped for velocity control is divided to 33.3 Hz. The phase difference between this and the SREF signal (33.3 Hz) from the HD49211 signal processing LSI will then be latched as 9-bit error data. If the phase difference is within the detection range shown below, a PWM signal will be generated using the error data. If it is outside of the detection range, then depending on the difference the PWM output will be fixed at "H" or "L".

Offset control

Figure 23 shows the capstan motor/reel motor offset control circuit. The error voltages from capstan motor velocity, phase, and ATF are all integrated by the offset integrater and then inverted by the offset amp. This signal is then output as the capstan motor/reel motor offset voltage.

CISEL and COSEL select the error voltage for the offset servo. HOLD is a switch that halts operation of the offset integrater, holding the output voltage.

Table 18 Detection Range Parameters for Capstan Motor Velocity Control

Item	Mode I	II	III
CFG frequency	400 Hz	466.67 Hz	633.3 Hz
Counter clock frequency	588 kHz	588 kHz	588 kHz
PWM carrier frequency	9.188 kHz	9.188 kHz	9.188 kHz
Detection range	±17.41 %	±20.32 %	±27.59 %
Detection sensitivity	5.71 mV/rad/sec	4.20 mV/rad/sec	2.28 mV/rad/sec
Initial count value ND	702	492	160
General count value N	1470	1260	928

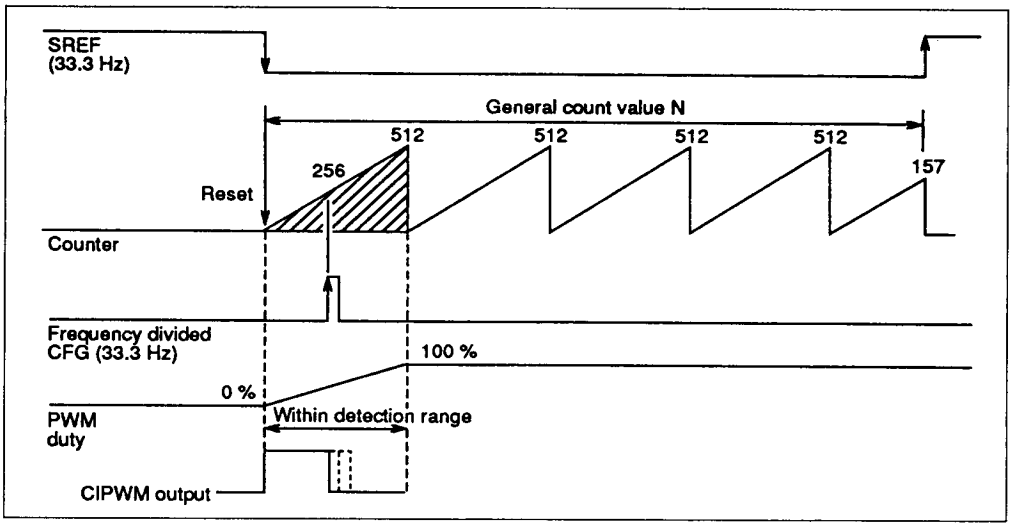


Figure 22 Detection Range for Capstan Motor Phase Control

Table 19 Detection Range Parameters for Capstan Motor Phase Control

Item	Normal mode
Sampling frequency	33.3 Hz
Counter clock frequency	147 kHz
PWM carrier frequency	9.1875 kHz
Detection range	±5.8%
Detection sensitivity	6.86 V/rad
General count value N	2205

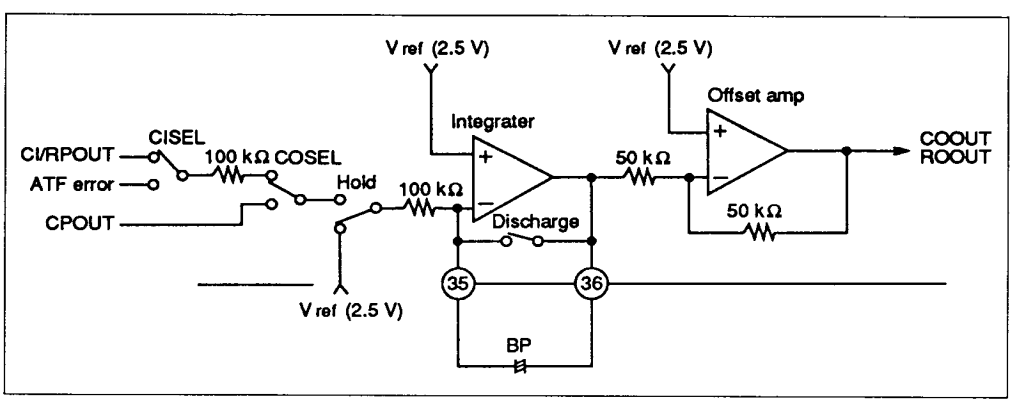


Figure 23 Capstan Motor/Reel Motor Offset Control Circuit

Output amplifier circuits

The HD49212 has output buffer amps on-chip for each control type: velocity control, phase control, and offset control. As shown in figure 24, each of the PWM outputs is smoothed by a low-pass filter and then connected to an on-chip amp. The outputs of the on-chip amps can directly sent to a resistor adder and the sum fed back to the motor velocity system.

For independent operation of a capstan motor and reel motor, send CPOUT, CIOUT and COOUT to the resistor adder and the sum to the capstan motor driver. Send RPOUT, RRAMP and ROOUT to the resistor adder and the sum to the reel motor driver.

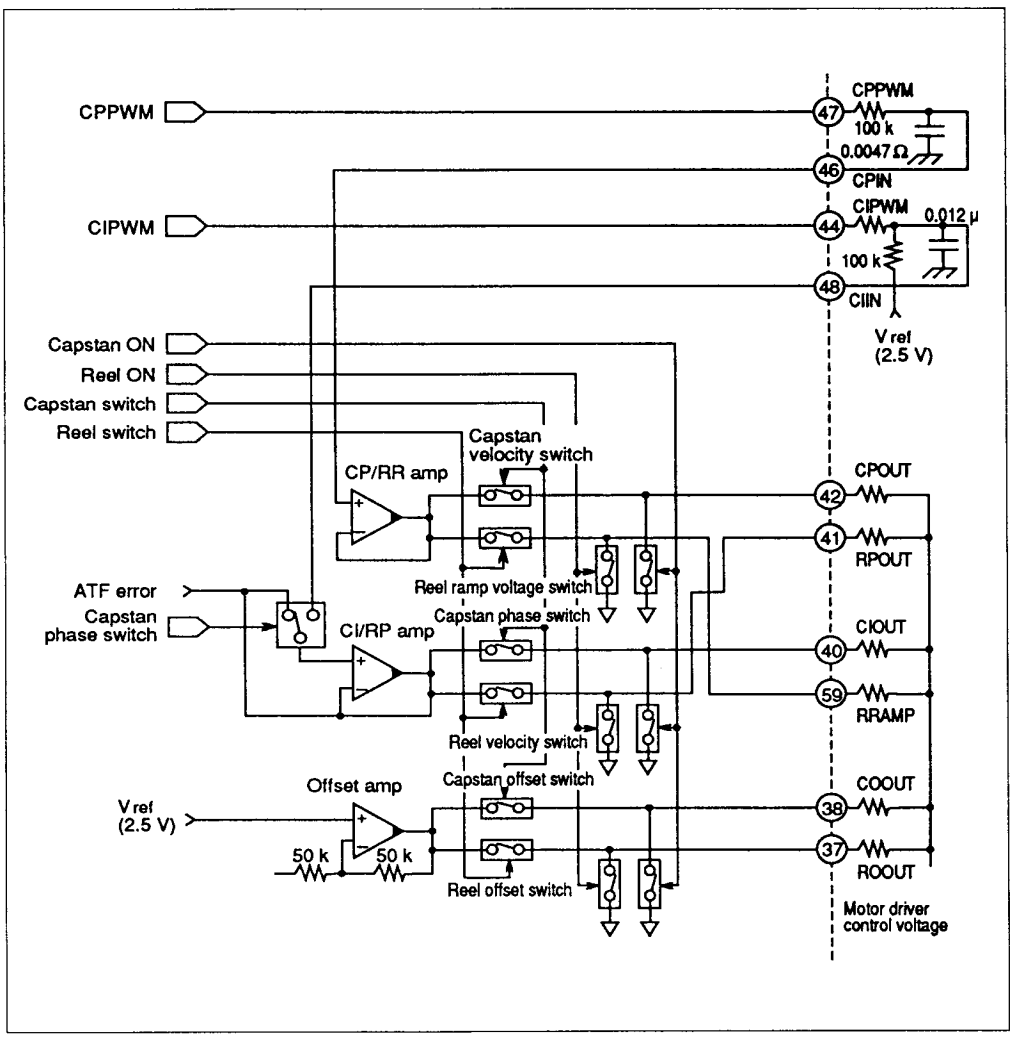


Figure 24 Capstan Control Output Amplifier Configuration

Capstan motor/reel motor lock signal

Capstan motor/reel motor control status can be monitored from the CRLOCK pin. table 20 shows CRLOCK output conditions.

Table 20 CRLOCK Output Conditions

Mode	Output conditions for CRLOCK = "H" (CRLOCK = "L" under all other conditions) (Notes)
REC	CPLK • CON • CION
ATF playback	CPLK • ATFLK • CON • CION
Playback when ATF OFF	CPLK • CON
FF/REW/Search	CPLK • RSVLK • RON

Notes:
1. CPLK (capstan velocity lock signal):
   Set to "H" if the capstan velocity error data is within the detection range.
2. CON (capstan motor ON signal):
   Mode data signal from microprocessor. Set to "H" when capstan motor is ON.
3. ATFLK (ATF lock signal):
   Set to "H" when SYNC is detected by ATF control (after which ATF tracking proceeds correctly).
4. RSVLK (reel motor velocity control ON signal):
   Set to "H" when reel motor velocity control starts.
5. RON (reel motor ON signal):
   Mode data signal from microprocessor. Set to "H" when reel motor is ON.
6. CION (capstan velocity lock-detection signal):
   Set to "H" when the upper 5 bits of velocity error data are locked in the center.

ATF Block

Block Overview

This block first detects the ATF SYNC signal from the RF signal and generates sampling pulses for ATF error voltage generation. From these sampling pulses, a pilot signal is amplified and detected and then sampled and held. This block then generates the ATF error voltage and performs ATF tracking during playback.

Block Function

Sampling pulse generation

- **SYNC amplifier**

A SYNC signal is detected from the RF signal using a band-pass filter. It is amplified by the SYNC amp and then passed through a comparator to convert it to a logic signal. Use a group delay equalizer for the SYNC band-pass filter if necessary gain of the SYNC amp is typically 18 dB.

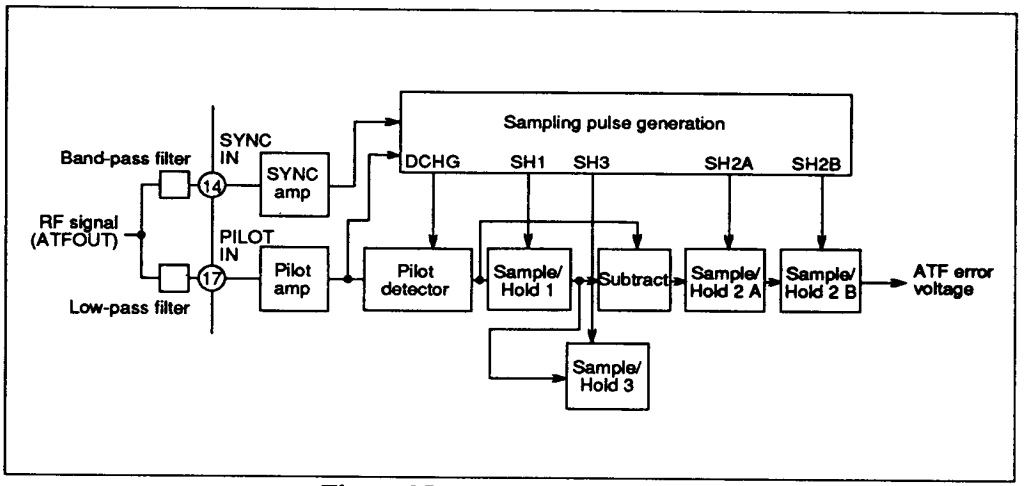


Figure 25 ATF Block Diagram

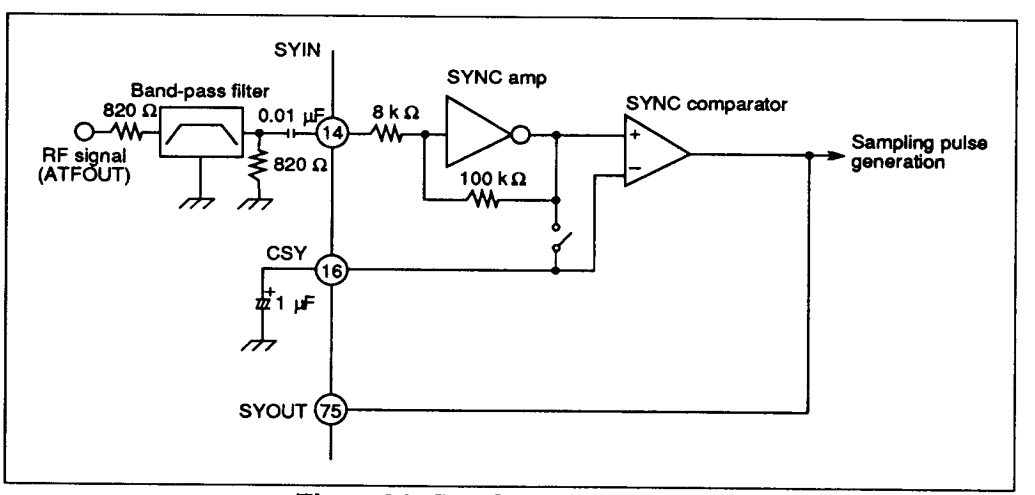


Figure 26 SYNC Amplifier Circuit

• **SYNC monitor**

The waveshaped SYNC signal can be monitored from the SYOUT pin (PLAY mode).

• **SYNC misdetection prevention**

New signals are recorded on DAT without an erase head but by overwriting. Because previous SYNC signal sometimes is not erased in the pilot area, misdetection of SYNC signals can occur during playback. To counter this, the HD49212 prevents SYNC misdetection using the on-track pilot signal, and so detects only correct SYNC signals. This is shown in Figure 27.

After detection of the A-track ATF1 and B-track ATF2 on-track pilot signal, then each time a SYNC appears to be detected, SYNC signal frequency and length are checked. Only correct SYNC signals are then taken.

Misdetection prevention for A-track ATF2 and B-track ATF1 is not performed. Only SYNC signal frequency and length are checked. SYNC signal misdetection prevention can be controlled from microprocessor mode data (PROT bit). For details, refer to the "Microprocessor Interface Block" section.

• **Sampling pulse generation**

Sampling pulses are used to generate the ATF error. Figure 28 shows sampling pulse generation timing.

(a) DCHG signal

Discharges all detector peak-hold capacitors, making possible sample/hold of the pilot signal.

(b) SH1 signal

Sample/holds the pilot signal putout by the adjacent track.

(c) SH2A, SH2B signals

Sample/holds the level difference of pilot signals from two adjacent tracks.

(d) SH3 signal

Generates the reference voltage of the pilot comparator.

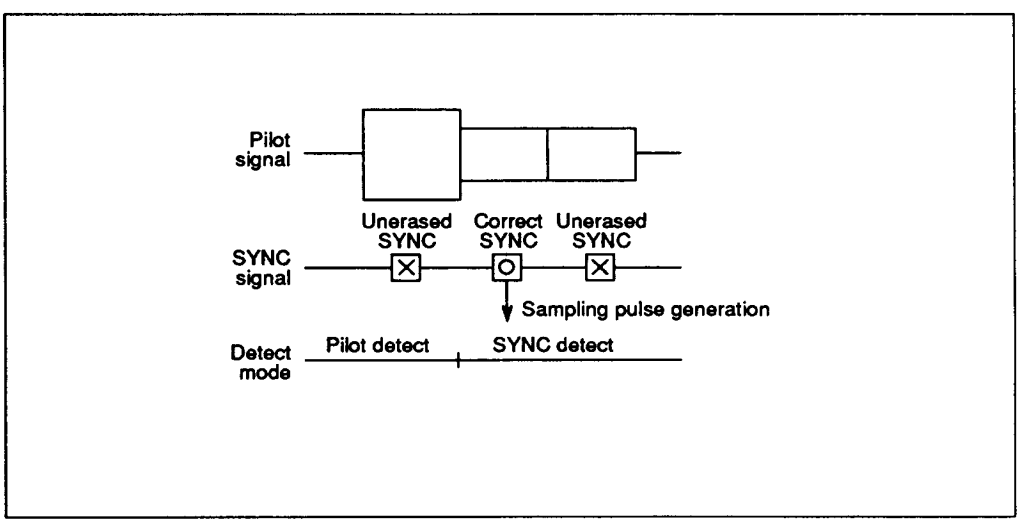


Figure 27 SYNC Signal Detection (A-track ATF1, B-track ATF2)

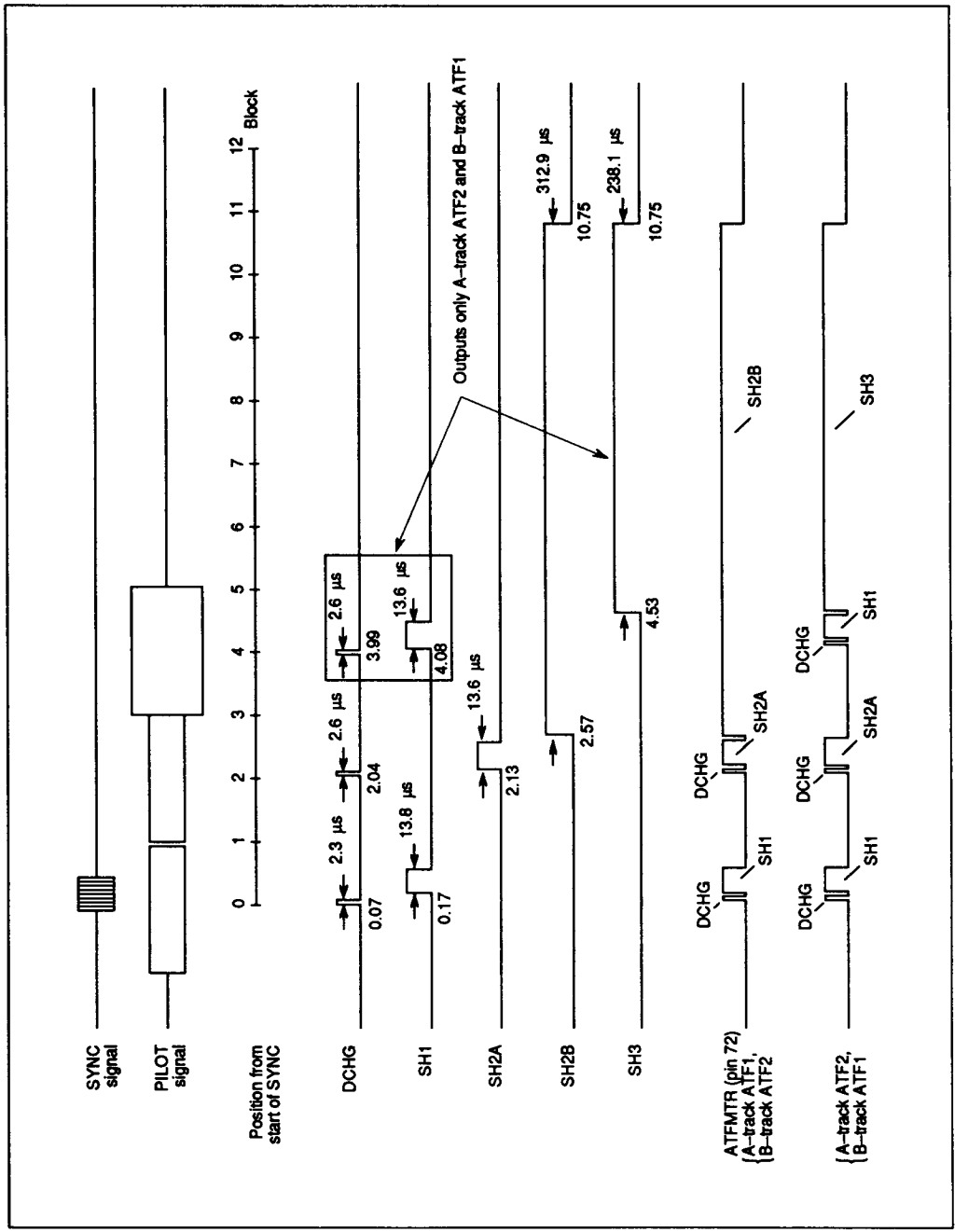


Figure 28 Sample Pulse Timing (1TP mode, both PROT ON/OFF)

- **Sampling pulse monitor**

Sampling pulses can be monitored from the ATFMTR pin (ATF control only). Refer to Figure 28 for timing. In FF/REW and high-speed search modes, the hunting monitor signal will be output.

- **ATF gate signal generation**

The ATF gate is set during ATF control in order to perform ATF-area detection. When noise of the same magnitude as the PCM signal area SYNC, misdetection can occur. By use of the ATF gate, misdetection can be prevented. The ATF gate can be turned on and off by the microprocessor mode data GATE.

- **ATF gate, SYNC pulse, pilot pulse monitor**

The ATF gate signal, SYNC detected pulses, and pilot detected pulses can be monitored from the ATFDET pin, as shown in figure 29. In FF/REW and search modes, the hold monitor signal is output.

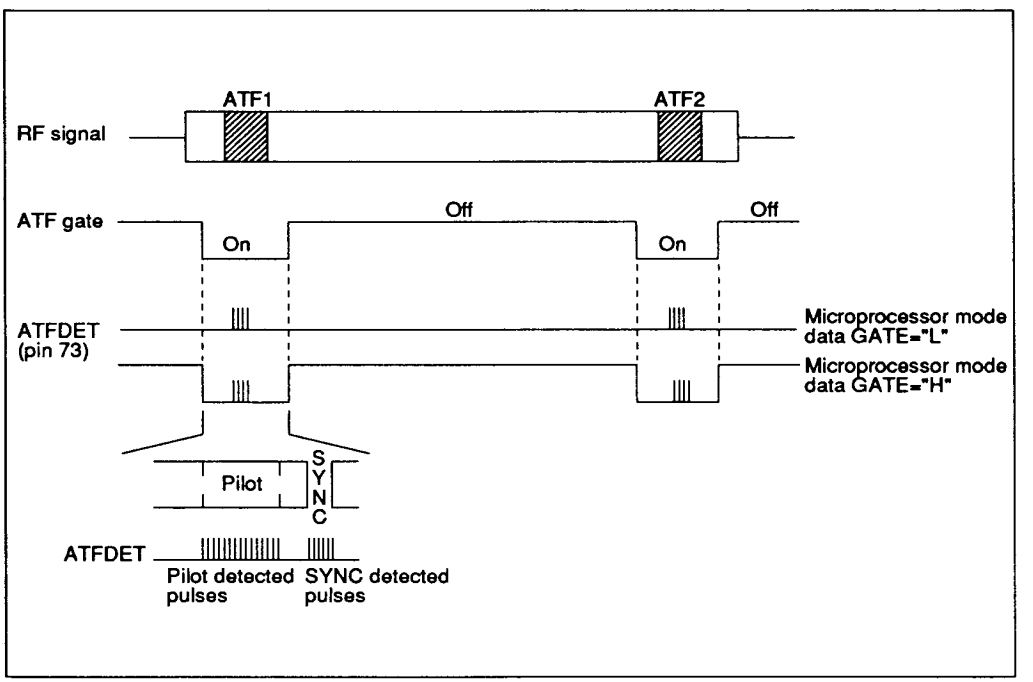


Figure 29 ATFDET Monitor Signal

ATF error generation

- **Pilot amplifier**

From the RF signal through the external pilot low-pass filter, the pilot signal is amplified by amp 1 and amp 2, and then sent to the pilot detector. Also, the output of amp 2 is passed through a comparator and converted to a logic signal, which is then sent to the sampling pulse generation circuit.
The gain of amp 1 can be adjusted independently for the A-head and B-head. However, if the sensitivity dispersion of the A-head and B-head is small, then short AGAIN and BGAIN as shown in figure 30.
The gain of amp 1 can be varied within the range 14 – 29 dB (130 kHz). The gain of amp 2 can be selected as either 20 dB or 26 dB. The selected gain can be monitored from the microprocessor with mode data TSPD.

- **Pilot monitor**

While in PLAY mode, the wave-shaped pilot signal can be monitored from the PLTOUT pin.

- **Pilot detector**

The pilot detector puts the pilot signal through a full-wave rectifier and a peak-hold circuit, and then sends it to the sample-hold circuit.
In order to prevent coupling between the full-wave rectifier reference voltage and the pilot amp 2 offset voltage, the pilot amp 2 output voltage is generated passing through a low-pass filter. This low-pass filter consists of an on-chip 50 kΩ resistor and a capacitor connected to CPLT.
The rectified signal is put in a peak-hold circuit. A capacitor between the PLTENV and VREF pins holds the peak value. DCHG provides the signal for discharging the peak-hold capacitor.

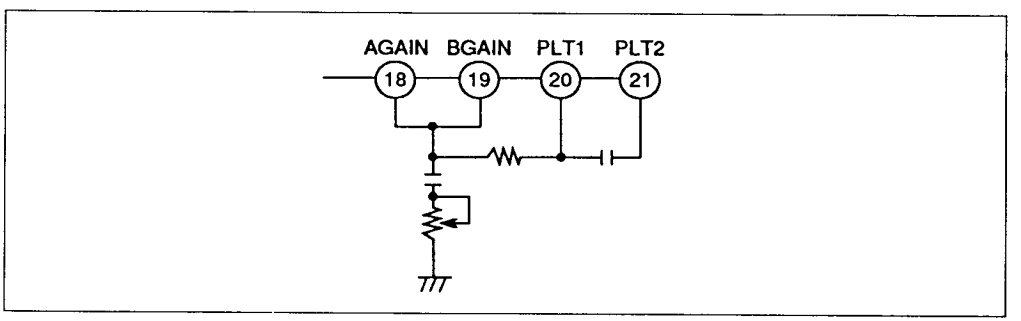


Figure 30 Example of Amplifier 1 Gain Adjustment

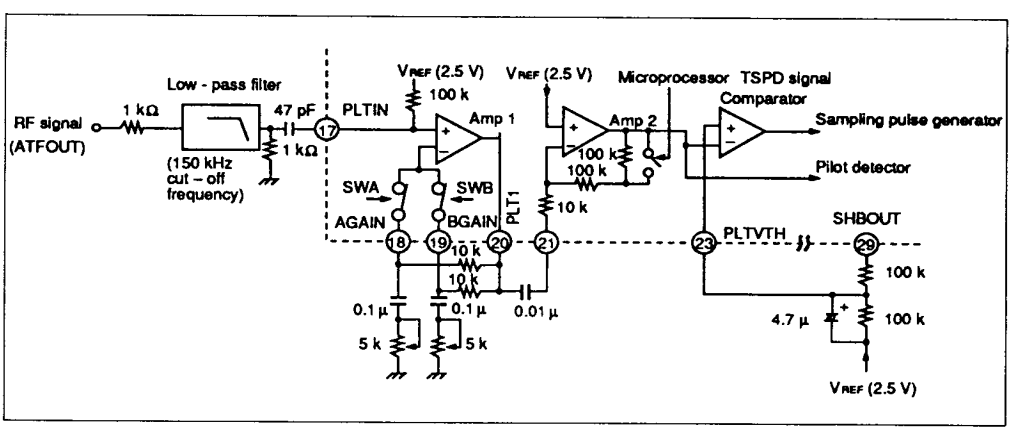


Figure 31 Pilot Amplifier Circuit

• **Sample-hold circuit**

The sample-hold circuit consists of 3 sample-hold sections and a subtracter. Each sample-hold section is controlled by the SH1, SH2A, SH2B and SH3 signals generated in the sampling pulse section.

As shown in figure 33, the pilot signal of the adjacent track is sampled on the SH1 pulse and held in capacitor CSH1. Next, the sampled voltage is subtracted from the next occurring pilot signal by the subtracter.

Then, that subtracted value is sampled on the SH2A pulse and held in capacitor CSH2A. This held voltage will become the ATF error voltage, but to prevent leakage and other negative influences, this voltage is sampled and held again on the SH2B pulse.

Finally, the signal is amplified by the ATF error amp and output as the ATF error voltage from pin CIOUT.

An external offset voltage from the VOFT pin can be added to the ATF error voltage. The applied offset voltage from the VOFT pin can be turned on and off with the microprocessor mode data OFT signal.

SH3 samples and holds the pilot signal level when on-track. This held voltage is passed through a low-pass filter and sent to the pilot amp comparator. It is then used as the pilot signal detector reference potential when on-track.

In order to keep the on-track pilot signal from being held in the CSH3 capacitor after ATF playback has begun, CSH3 is charged to 3.0 V typically while the capstan motor is halted.

ATF detection sensitivity can be adjusted by varying the gain of the ATF error amp. Adjust the ATF error amp gain with an external resistor after taking into account the ATF loop gain and capstan phase error voltage added gain. The ATF error amp can be used from a gain of 0 dB (voltage follow).

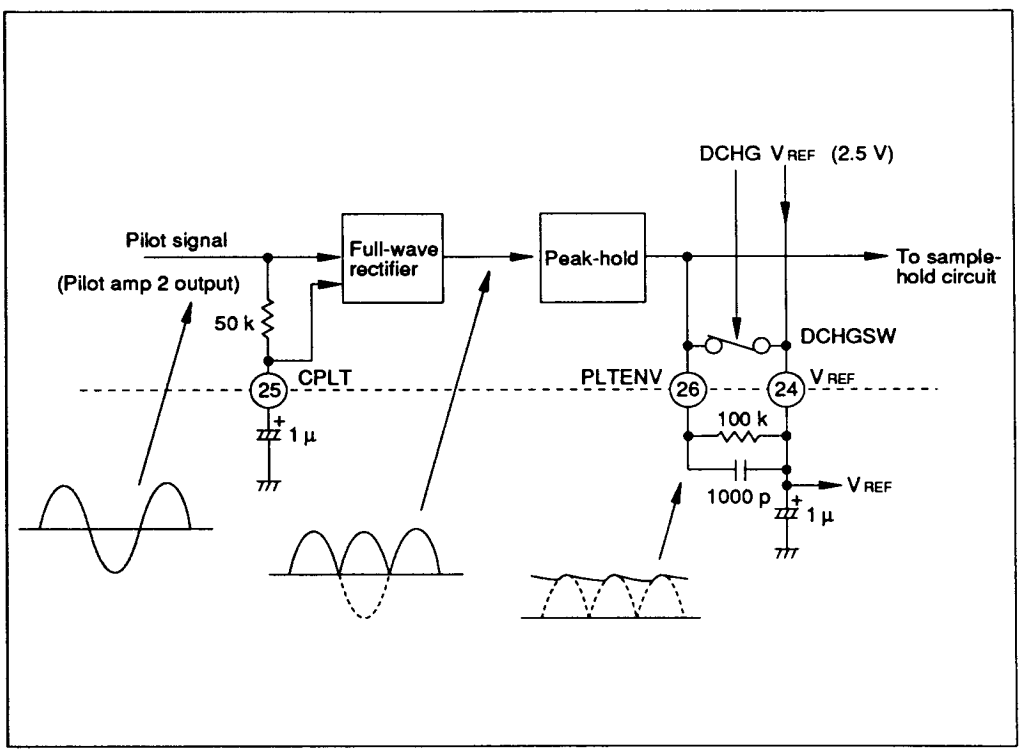


Figure 32 Pilot Detector Circuit

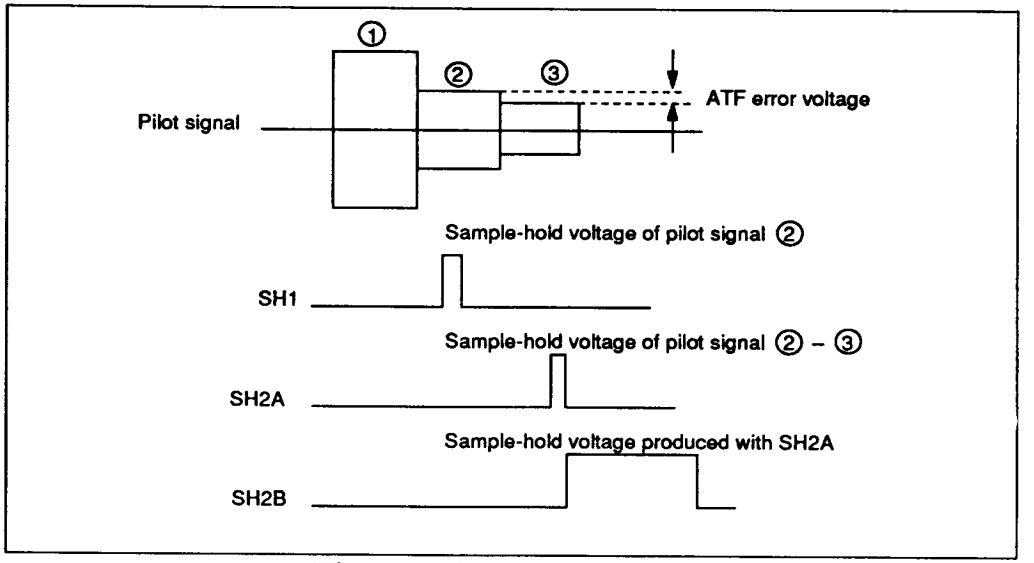


Figure 33 Sample-Hold Timing

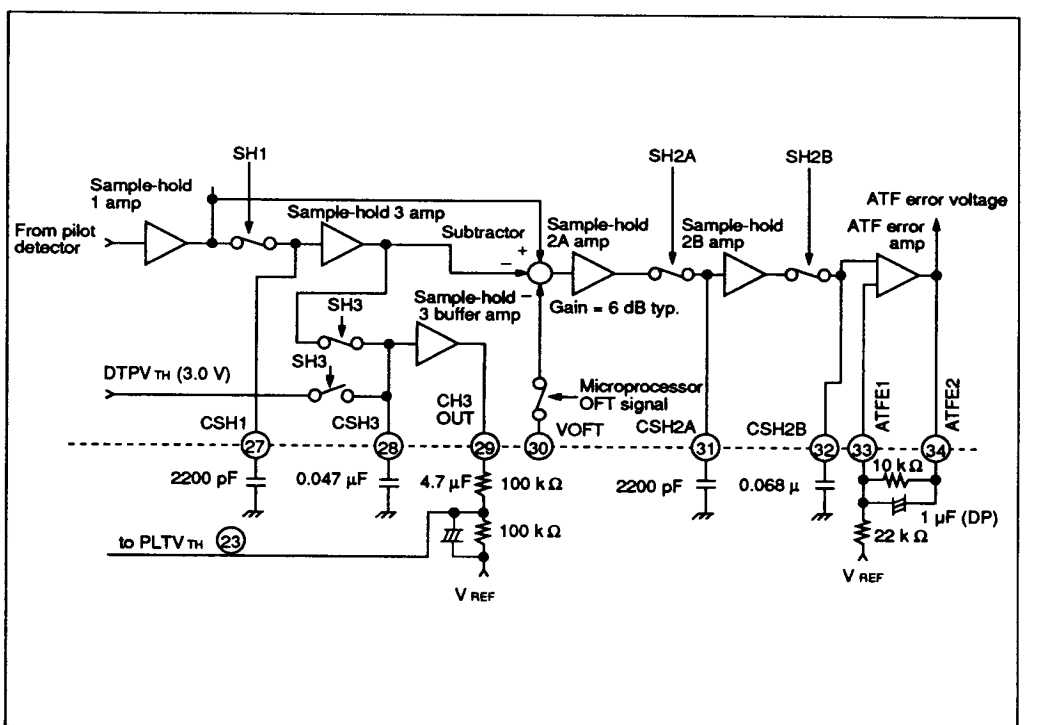


Figure 34 Sample-Hold Circuit

• **Reference voltage generation**

This section generates VREF for use as the linear section's reference voltage as well as DTPVTH for use as the DTP comparator's reference voltage.
The power supply voltages (AVDD, AVss) are put through a resistor divider to make VREF (2.5 V typ.) and DTP VTH (3.0 V typ.). Also, a division of the power supply voltage charges the CSH3 capacitor in the sample-hold circuit when the capstan motor is halted (microprocessor data CON = "L").

ATF offset control

Refer to the section covering the capstan motor offset control circuit.

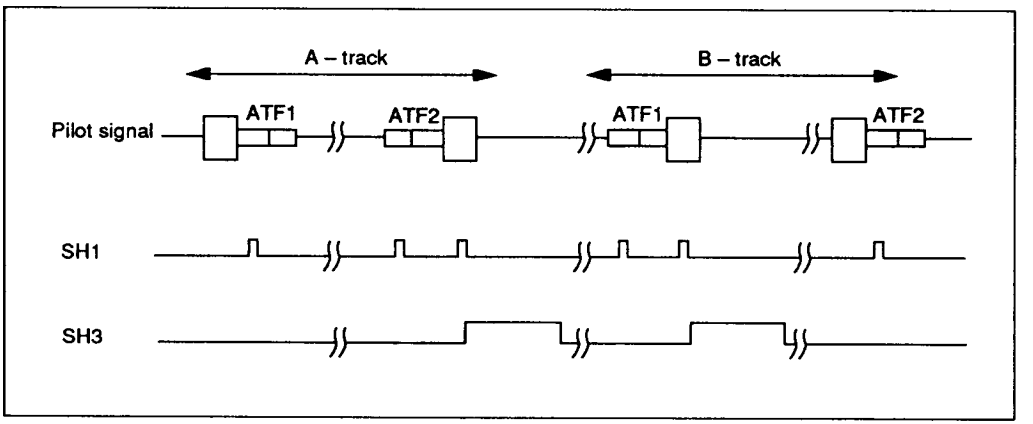


Figure 35 Sample-Hold 3 Timing

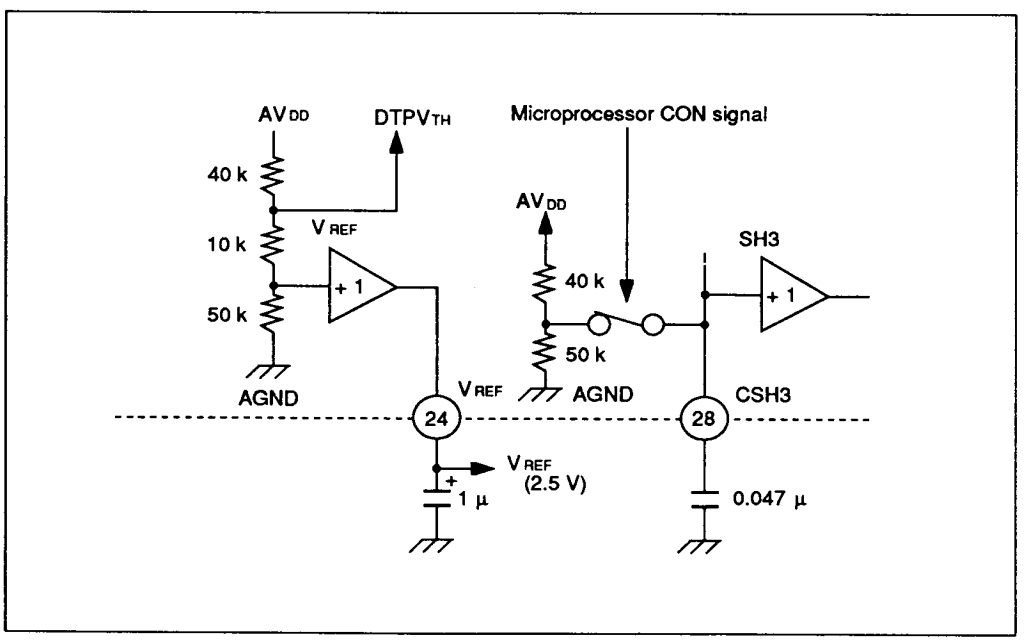


Figure 36 Reference Voltage Generation Circuit

Reel Motor Control Block

Block Overview

This block performs three types of servo control for reel motors: ramp voltage generation, velocity control, and offset control. Refer to Figure 18 "Capstan Motor/Reel Motor Control Block Diagram" for the configuration of the reel motor control block. Figure 37 shows the reel motor control flowchart.

- **Ramp voltage generation**

During high-speed searching, reel motor control must keep the tape winding and travelling speed fixed relative to the drum motor velocity. Therefore the speed needs to ramp up smoothly from a stopped condition at a fixed rate. The HD49212 reel motor rising ramp voltage is generated along with the capstan motor phase control.

- **Velocity control**

Velocity control uses the FG signals which are generated from the reel axis (8 pulses/rotation). The system performs fixed-rotation count velocity control for a reel generating a single-axis FG signal only. It performs fixed frequency velocity control for a reel generating a dual-axis FG signal.

- **Offset control**

Reel motor offset control is common with capstan motor offset control. It outputs the error voltage from reel motor velocity control.

Block Function

Ramp voltage generation

Table 5-1 shows the ramp voltage rates. During high-speed searches, the ramp voltage steeply rises at 5.6 V/sec until the reel starts rotating. After rotation has begun, the ramp rate switches to that selected by the microprocessor mode data RTM1 and RTM2, such that reel rotation smoothly increases.

In order to perform searching while in FF/REW mode, the ramp voltage continues to rise steeply at 5.6 V/sec even after reel rotation has begun.

Also, the ramp voltage for high-speed searches is not generated until after the drum motor is rotating at 2000 rpm.

Ramp voltage is held when the velocity control error exceeds the center value.

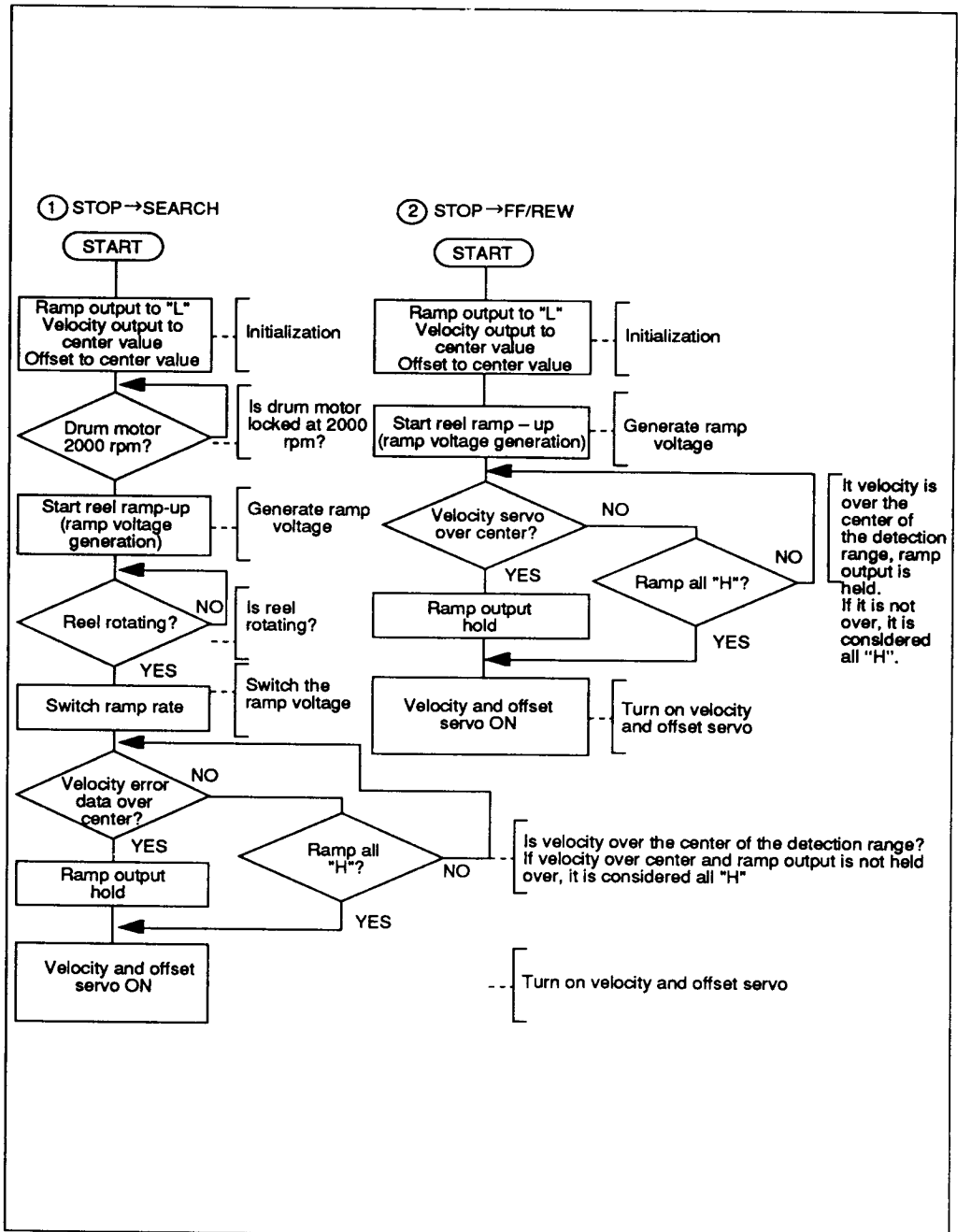


Figure 37 Reel Motor Control Flowchart

Velocity control

The reel FG signals (FGT, FGS) are edge-detected for velocity control. For 1-reel FG mode, the FGS edge pulse is used, while for 2-reel FG mode, both the FGT and FGS edge pulses are used. The cumulative FG periods are measured with a 9-bit counter.

The counter values are output as PWM error data. Figure 38 shows the cumulative period measurement timing for 2-reel FG mode.

Velocity control controls the servo such that the periods of figure 38 are in the center of the detection range. The detection range changes depending on the microprocessor mode data TSD1, TSD2 and TSD3, as shown in table 22. However, the detection range will depend on the mode data TSPD when operation is switched to 100x or 200x search.

Figures 39 – 42 shows actual ramp speeds for TSPD and TSD1-3.

Table 21 Reel Motor Ramp Voltage Rates

Item	Mode		Ramp voltage rate	
			High-speed search	FF/REW
Before reel rotation starts			5.6 V/sec	
After reel rotation starts	Microprocessor mode data			
	RTM1	RTM2		
	0	0	2.8 V/sec	5.6 V/sec
	1	0	1.4 V/sec	
	0	1	0.7 V/sec	
	1	1	0.35 V/sec	

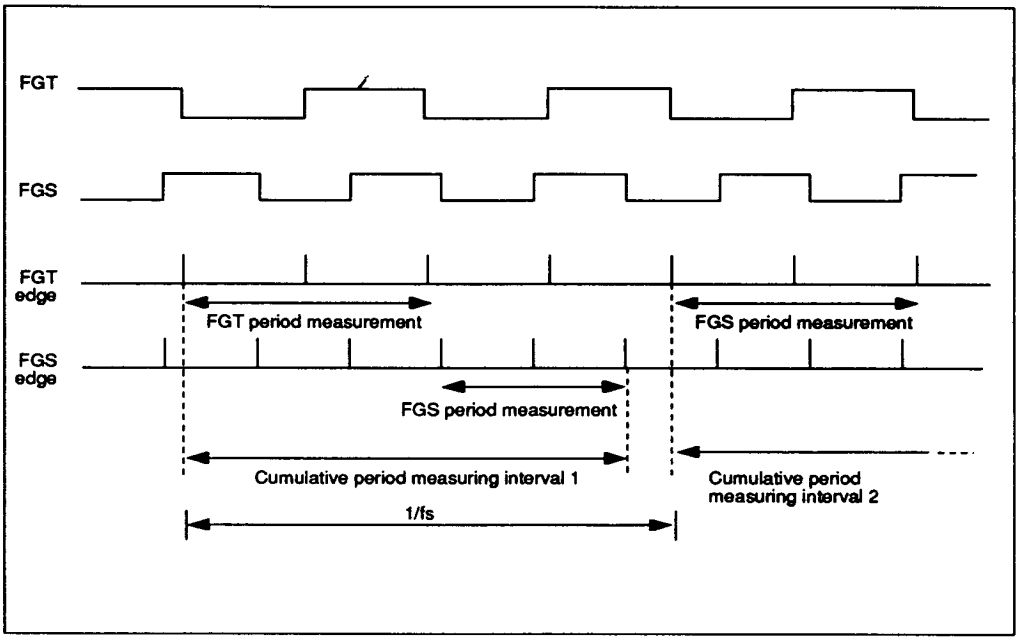


Figure 38 Reel FG Cumulative Period Measurement Timing

Table 22 Reel Velocity Control Measured Periods

			x200 (TSPD: L)			x100 (TSPD: H)			(Units: ms)
TSD1	TSD2	TSD3	Min	Detection range center	Max	Min	Detection range center	Max	
0	0	0	6.97	13.93	20.09	—	27.86	55.72	
1	0	0	6.09	13.06	20.03	—	26.12	53.98	
0	1	0	5.22	12.19	19.16	—	24.38	52.24	
1	1	0	4.35	11.32	18.28	—	22.64	50.50	
0	0	1	3.48	10.45	17.41	—	20.90	48.76	
1	0	1	2.61	9.58	16.54	—	19.16	47.02	
0	1	1	1.74	8.71	15.67	—	17.42	45.28	
1	1	1	0.87	7.84	14.80	—	15.68	43.54	

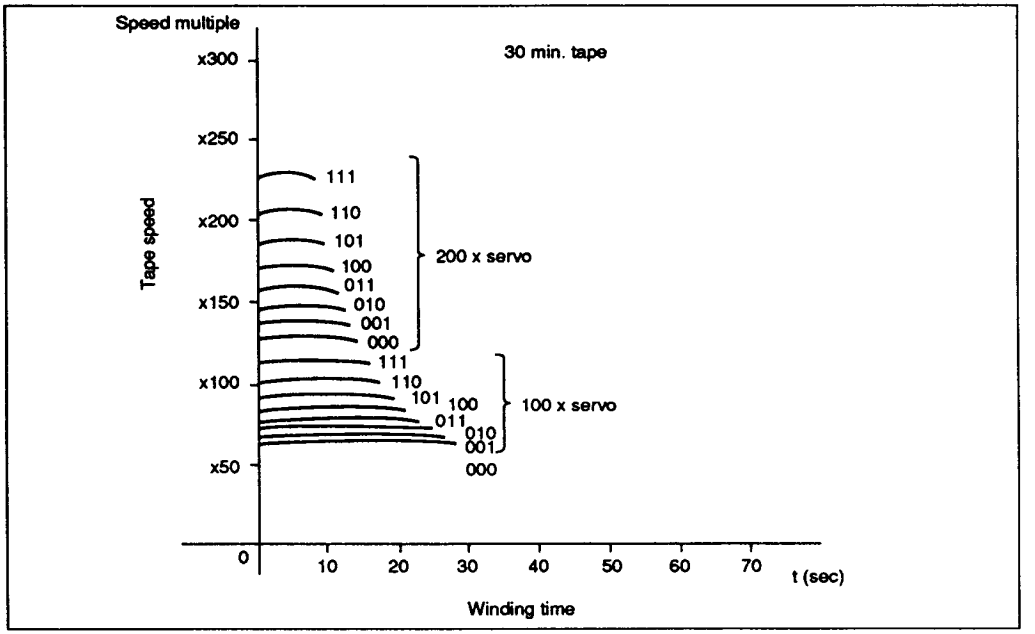


Figure 39 Reel Servo: Tape Speed Variation for Mode Data TSPD and TSD1-3

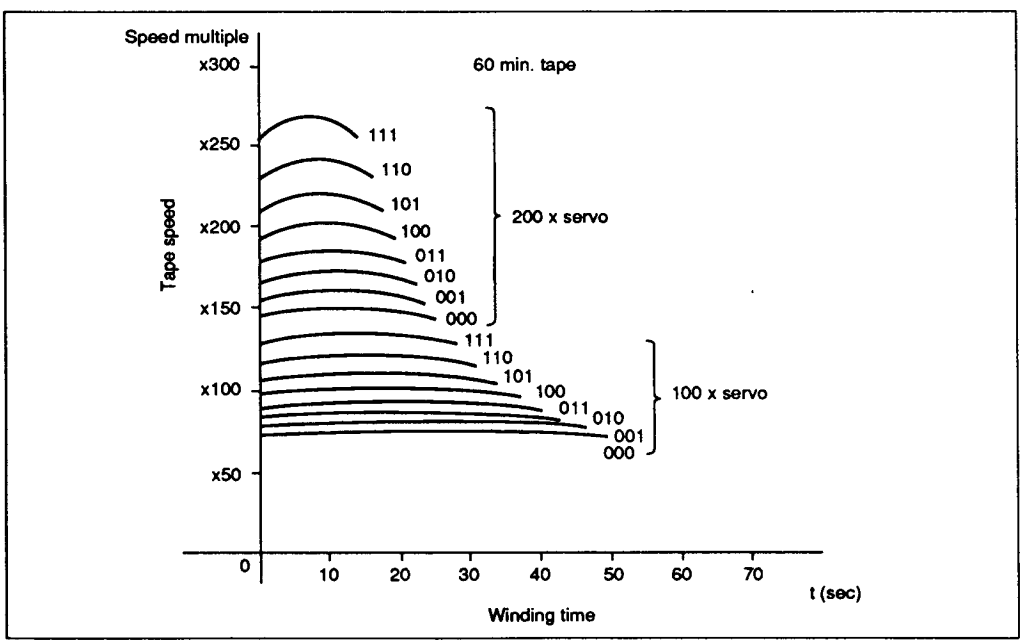


Figure 40 Reel Servo: Tape Speed Variation for Mode Data TSPD and TSD1-3

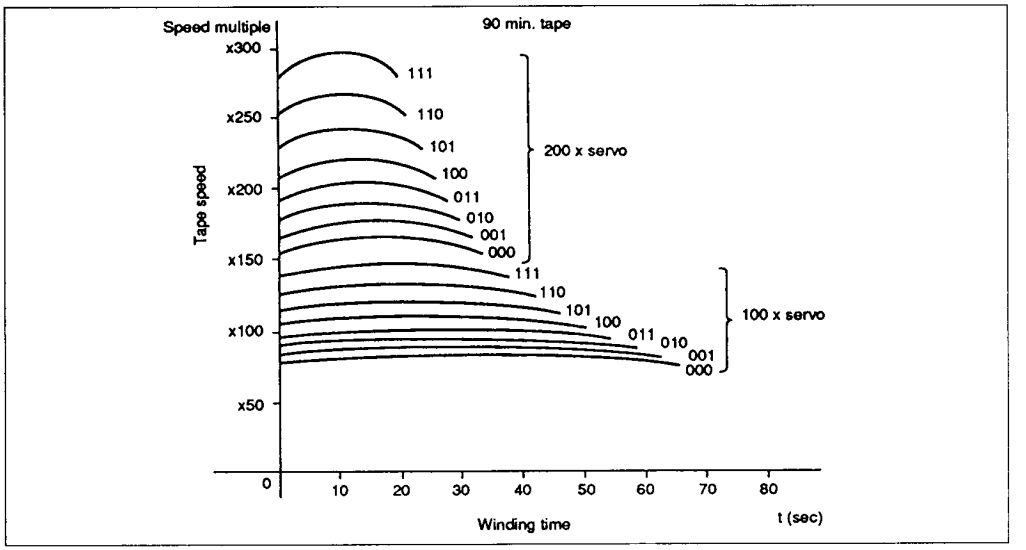


Figure 41 Reel Servo: Tape Speed Variation for Mode Data TSPD and TSD1-3

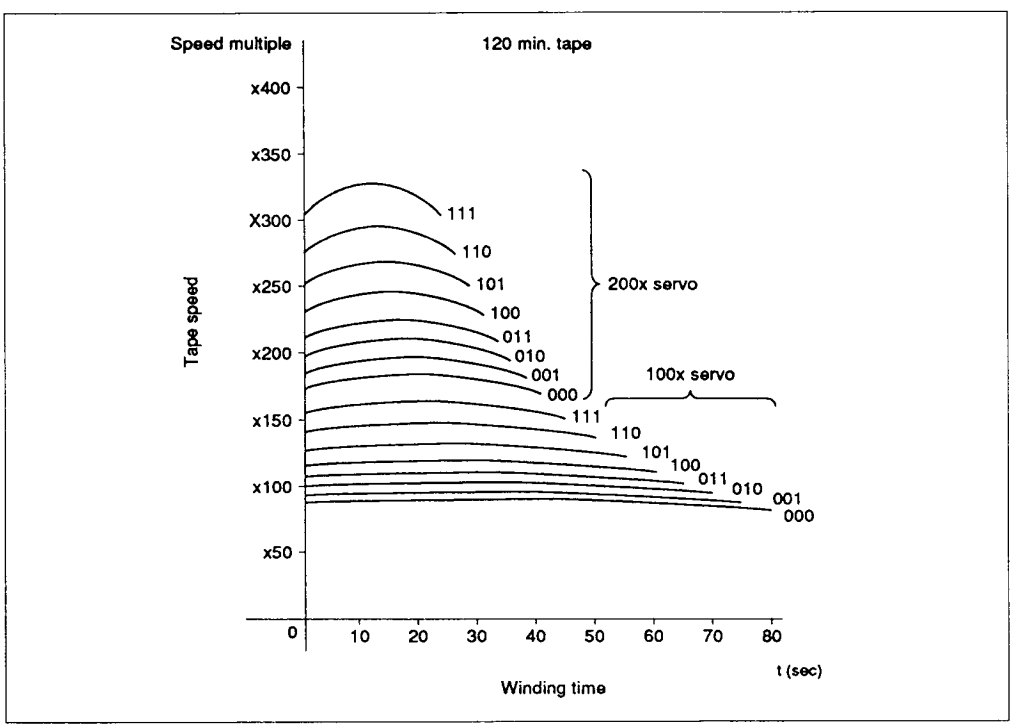


Figure 42 Reel Servo: Tape Speed Variation for Mode Data TSPD and TSD1-3

High-speed Search Control

Block Overview

This block plays back the sub-code signal on the tape while making it travel at 100x or 200x speed. It performs such functions as positioning the tape to the start of song selections.

In particular, this block controls tape speed by performing PDCK control, which fixes the drum motor effective relative velocity. When a search misses, it sweeps above and below the drum motor rotation rate. It performs hunting control in conjunction with tape relative velocity, and hold control when no RF signal is present on the tape.

Figure 43 shows the high-speed search control block diagram. Figure 44 shows the flowchart for control during high-speed searches.

When entering search mode from STOP, first drum motor rotation is brought to 2000 rpm. After this speed has been checked, real motor control is ON, and RF PLL LOCK is detected, then PDCK control begins.

However, if there is no RF signal when the reel motor starts, a 2000 rpm FG servo is maintained for the drum motor.

During FF searches, once the reel motor ramp-up has ended, the drum motor is switched to a 3300 rpm FG servo. In this case, while raising the drum motor rotation rate, the drum motor is held when its relative speed is fast enough, in order to easily detect the RF signal when it appears.

During REW searches, the drum motor is held at 2000 rpm.

If the PLL is not locked when the reel motor starts, hunting control begins. Normally for hunting control, drum motor speed begins to be reduced. However, if the reel motor were ramping up for a FF search, the drum motor rotation could not follow along. In this situation only does hunting start with the drum motor speed increasing.

When entering search mode from FF/REW, search mode proceeds during FF with a drum motor 3300 rpm FG servo, and during REW with a drum motor 2000 rpm FG servo.

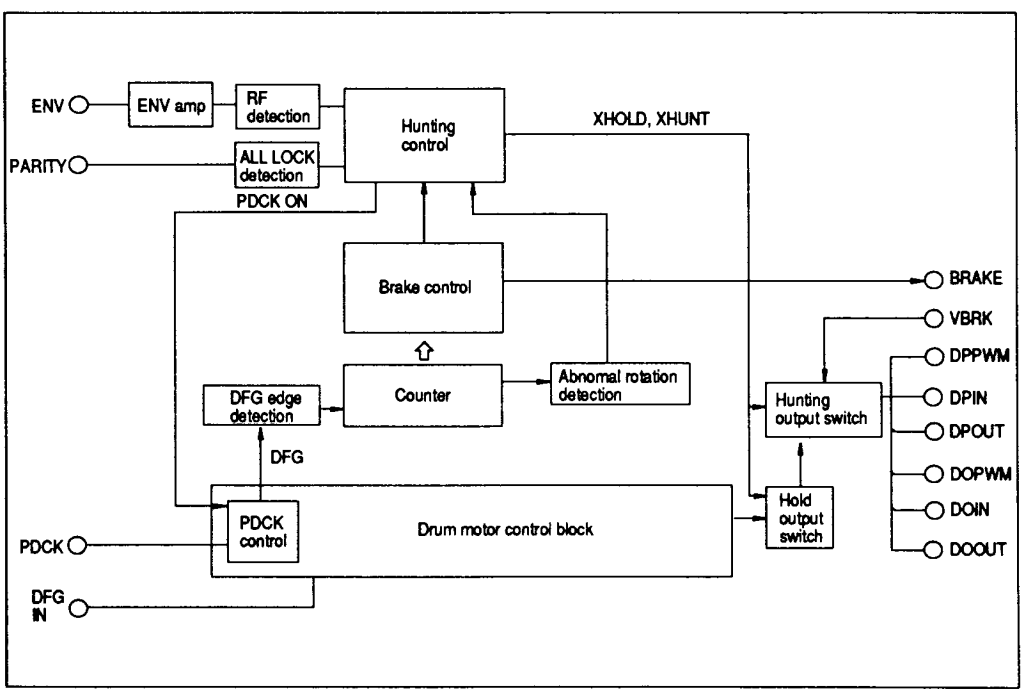


Figure 43 High-speed Search Block

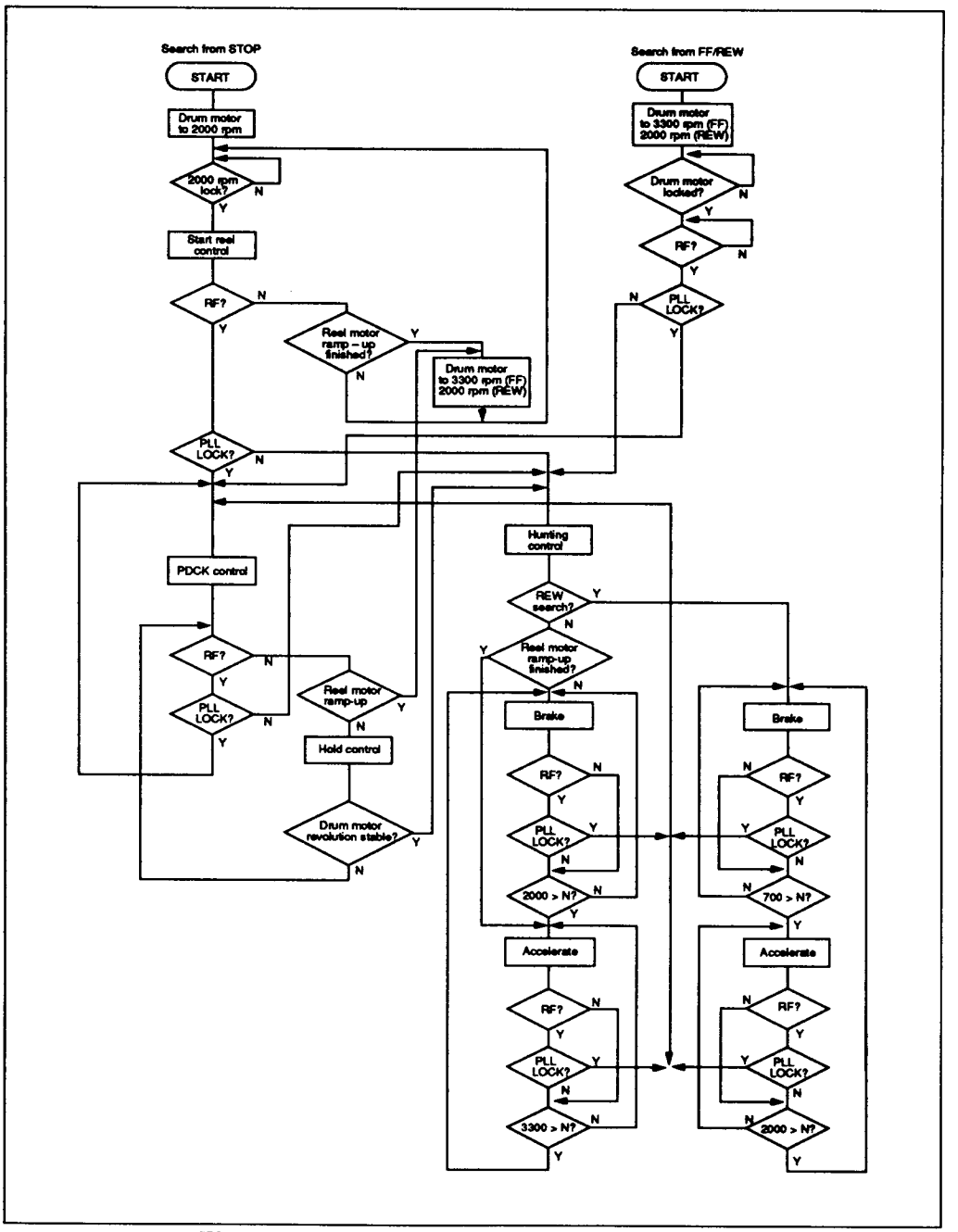


Figure 44 High-speed Search Control Flowchart

Block Function

PDCK Control

This section controls drum motor rotation so that tape travelling speed and head effective relative velocity are fixed.
The PDCK signal (9.408 MHz) is output after the head → pre-amp → data strobe sequence. When relative velocity is detected to be off its fixed value, drum motor rotation is measured dividing PDCK by 256. Drum motor rotation is then controlled so that the measured frequency becomes 9.408 MHz again.

- **PDCK ON signal generation**

PDCK is generated from the playback signal on the tape. In order for PDCK control to detected that relative velocity is off the data strobe playback clock frequency, PDCK must be PLL locked. Therefore, as conditions for entering PDCK control (PDCK ON), both detection of the RF signal and detection of the parity signal from the HD49211 signal processing LSI must be checked.

- **PDCK velocity control**

The PDCK signal is divided by 256, and its period is counted with a 4.7 MHz clock. This measured data is latched as 6-bit error data, and if it is in the detection range, a PWM signal corresponding to its value is generated.

If the PDCK periods are shorter than the detection range, the PWM output will be fixed at a "L" level. If the periods are longer, the PWM output will fixed at an "H" level.

The PWM signal is output from the DPPWM pin. Exactly as for drum motor control, this is sent through an external low-pass filter, input to DPIN, and then from DPOUT fed back to motor velocity control to fix the rotation rate.

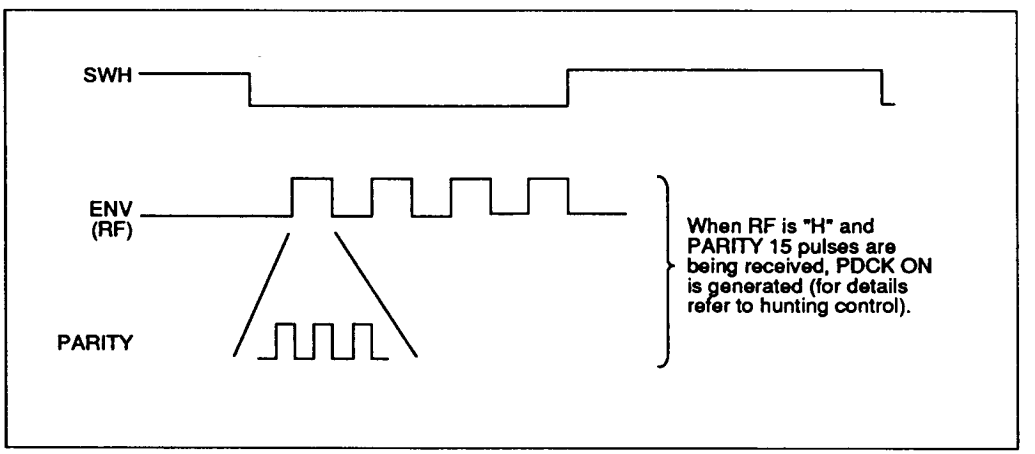


Figure 45 PDCK ON Timing

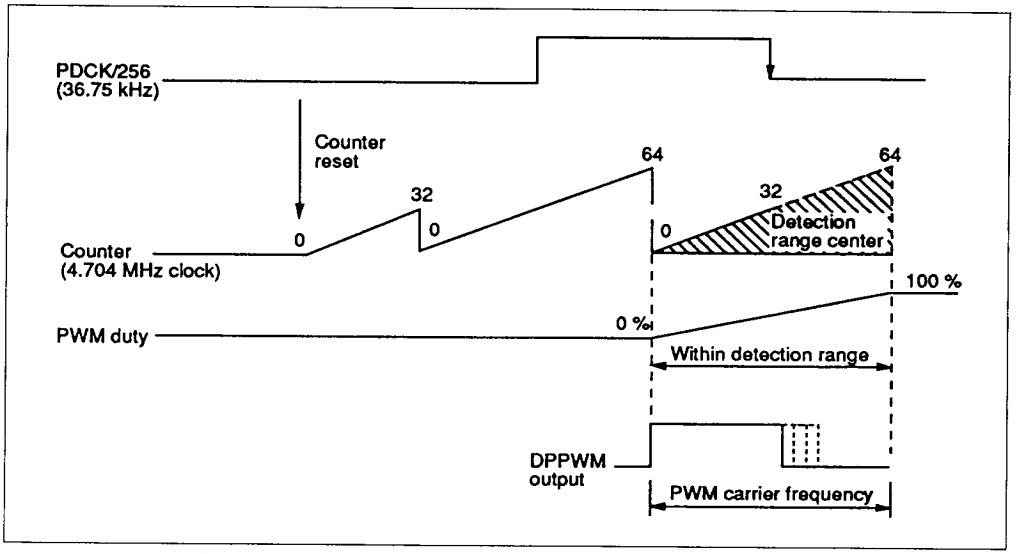


Figure 46 Detection Range for PDCK Velocity Control

- **PDCK offset control**

PDCK offset control corrects velocity errors so that its error data approaches a center vlaue. Since drum motor rotation rates are different for FF searches and REW searches, offset control data is taken as written below. The offset control output is the same as that of the drum motor control block.

Table 23 Detection Range Parameters for PDCK

Item	High-speed search
PDCK frequency (divided by 256)	36.75 kHz
Counter clock frequency	4.704 MHz
PWM carrier frequency	73.5 kHz
Detection range	25%
Detection sensitivity	13.7 mV/rad
General count value N	128 (detection range center)

Table 24 PDCK Offset Control Bandwidth

Mode	Bandwidth
FF search	1.0 Hz
REW search	0.64 Hz

Note: When the voltage for the velocity error and the voltage for the offset error are equal.

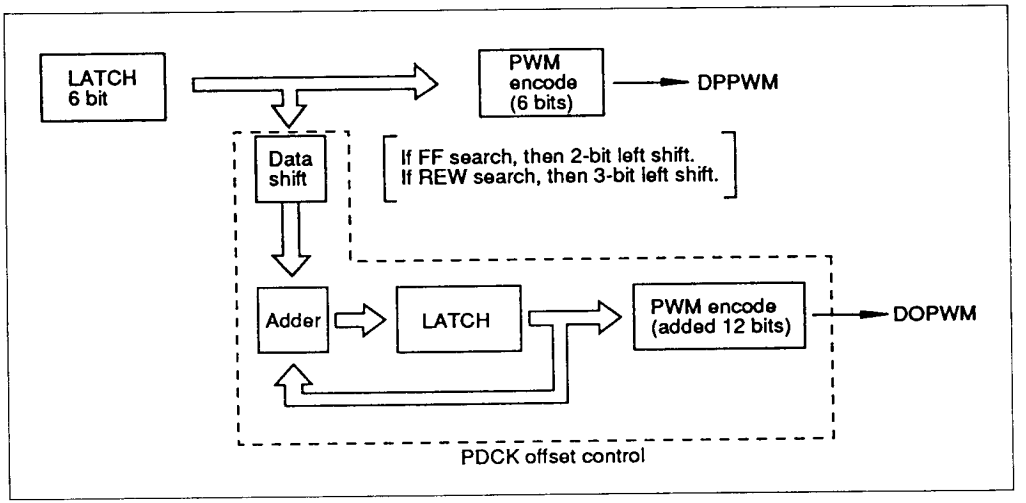


Figure 47 PDCK Offset Control Block Diagram

Hunting control

- **RF detection**

The RF detector's output envelope amp amplifies the input from ENVIN. After amplification, it is passed through a comparator and converted to a logic signal. After logic conversion, the envelope is passed through an inverter and sent to the ENVOUT pin, from which it can be monitored. Envelope amp gain is typically 21 dB.

Based on the logic converted envelope, the RF detector detects whether or not the envelope signal of a drum motor revolution exists. If there is an envelope signal for at least 40.8 µs, the RF detector considers the signal to exist. It then outputs an "H" on the monitor pin RF and also sends this result to the hunting control section.

- **PLL lock detector**

The PLL lock detector counts the drum motor rotation parity pulses as input from the HD49211 signal processing LSI. The PLL is considered to be locked when the parity pulse count reaches 15. The PLL lock detector then outputs an "H" on the monitor pin PLL LOCK and also sends this result to the hunting control section.

- **Hunting control**

Normally high-speed searches perform PDCK control following the PDCK signal input from the HD49211 signal processing LSI. However, if the PDCK ON signal becomes OFF for some reason, hunting control or hold control will be performed. Hunting control is performed during high-speed searches when for some reason tape speed and drum motor relative velocity no longer correspond (PLL unlocked). In order to match up the relative velocity, hunting control changes the drum motor rotation rate. During FF searches, the rotation rate sweeps from 2000 to 3300 rpm; during REW searches, it sweeps from 700 to 2000 rpm.

Figure 49 shows drum motor rotational velocity during hunting. As shown in figure 50, the DPOUT pin is connected to the VBRK pin. After the motor driver control voltage is fixed, the motor's direction of rotation is switched by the brake signal from the BRAKE pin. Drum motor velocity is thereby increased or reduced.
Connect the BRAKE pin should to the rotational direction reverse pin of the drum motor driver.

Table 25 Conditions for Control Modes During High-Speed Searches

Monitor signal		
RF	**PLL LOCK**	**Control mode**
"H"	"H"	PDCK control
"H"	"L"	Hunting control
"L"	"L"	Hold control
"L"	"H"	

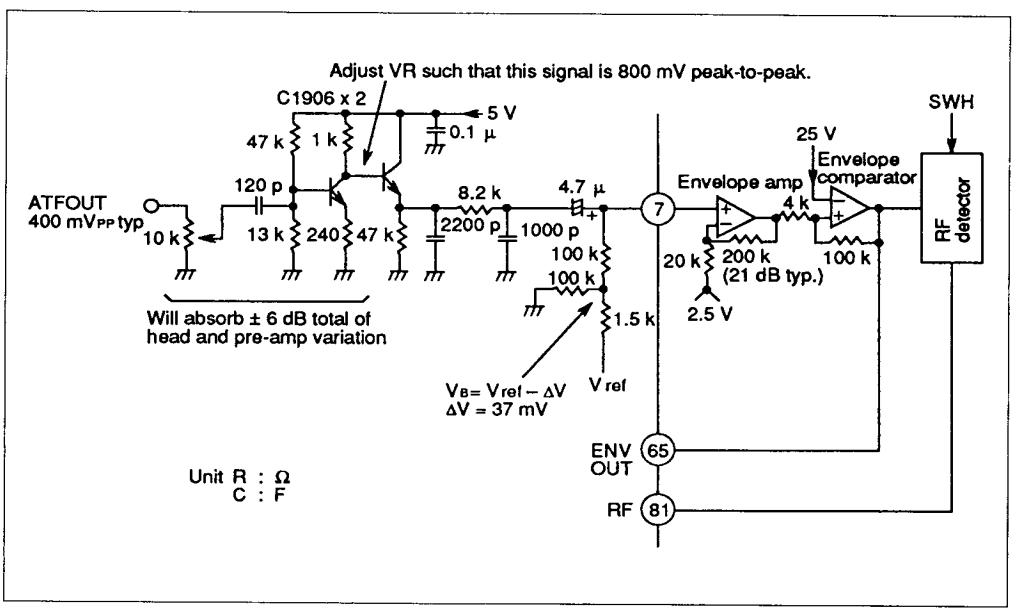


Figure 48 RF Detector Circuit

- **Drum motor rotation rate detection**

In order to detect whether the brake signal is on or off in hunting mode, the DFG period of the drum motor is measured with a 7-bit counter. Table 26 shows the drum motor rotation rate when the brake signal is on and off.

- **Hunting control monitor**

During high-speed searches, the ATF control monitor pin ATF MTR (pin 72) becomes the hunting monitor pin.

Table 26 Drum Motor Rotation Rate for Hunting Control

Mode	DFG	Counter CK	Rotation rate – brake on	Rotation rate – brake off
FF search	666.6 Hz	73.5 kHz	3270 rpm	2016 rpm
	800 Hz	73.5 kHz	3270 rpm	2008 rpm
REW search	666.6 Hz	18.375 kHz	2080 rpm	703 rpm
	800 Hz	18.375 kHz	2042 rpm	701 rpm

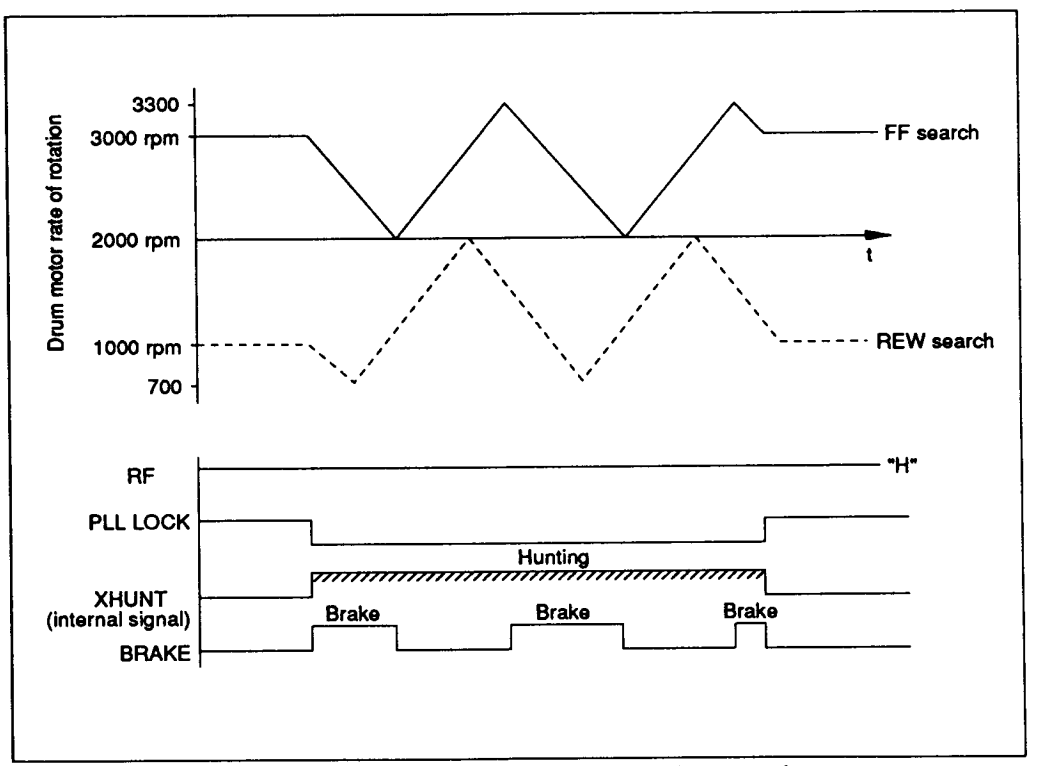


Figure 49 Drum Motor Rotation During Hunting

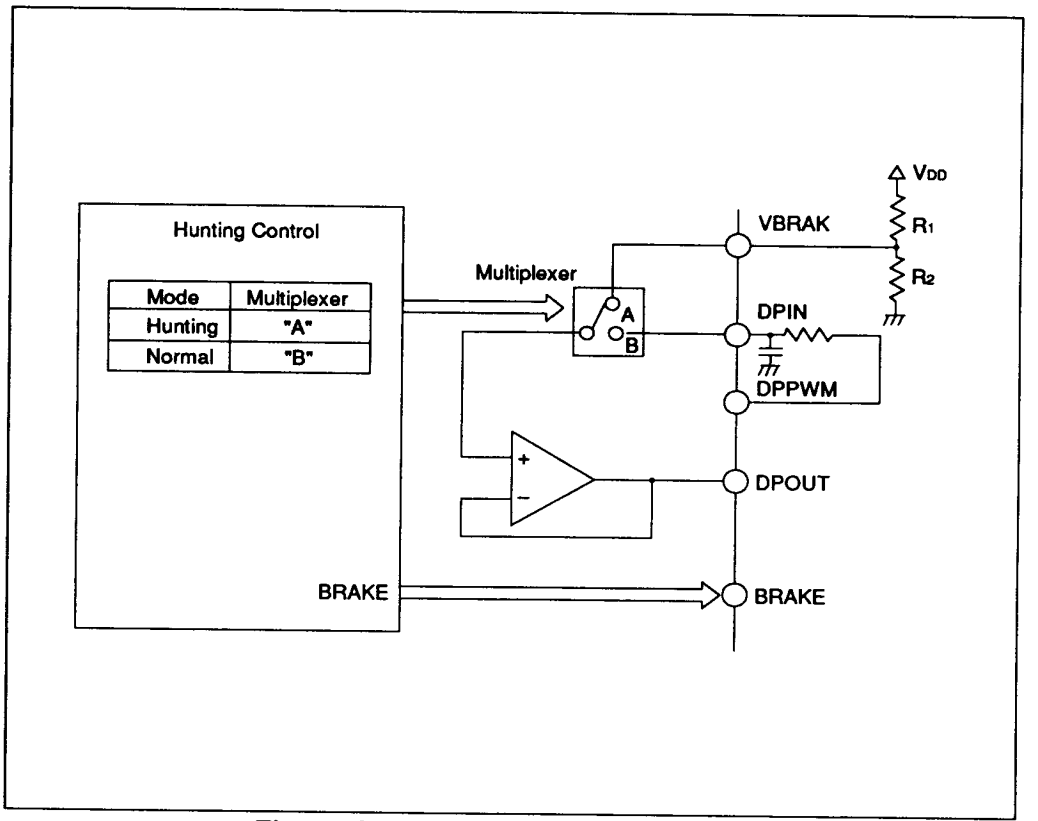


Figure 50 Output Switch During Hunting

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Hold control

- **Hold control**

When the RF signal disappears during high-speed searches, depending on PDCK control and hunting control, it may be impossible to match up tape speed and drum motor rotational velocity. In such cases, the HD49212 responds with its hold control function.

Hold control outputs a 50% duty cycle pulse from the DPPWM pin, and it maintains the data output on the DOPWM pin previous to losing the RF signal. Figure 51 shows the drum motor rotation rate during hold control.

In hold control, if RF and PLL lock are detected, then PDCK control is entered.

Further, the hold function normally detects the drum motor rotation rate. If an abnormal rotation rate begins as shown in table 27, control is forced to shift to the hunting function. Figure 52 shows the drum motor rotation rate when an abnormal rate is detected.

- **Hold control monitor**

During high-speed searches, the ATF control monitor pin ATF DET (pin 73) becomes the hold monitor pin.

ATF DET = "H" : Hold control
= "L" : Other control
(during high-speed searches only)

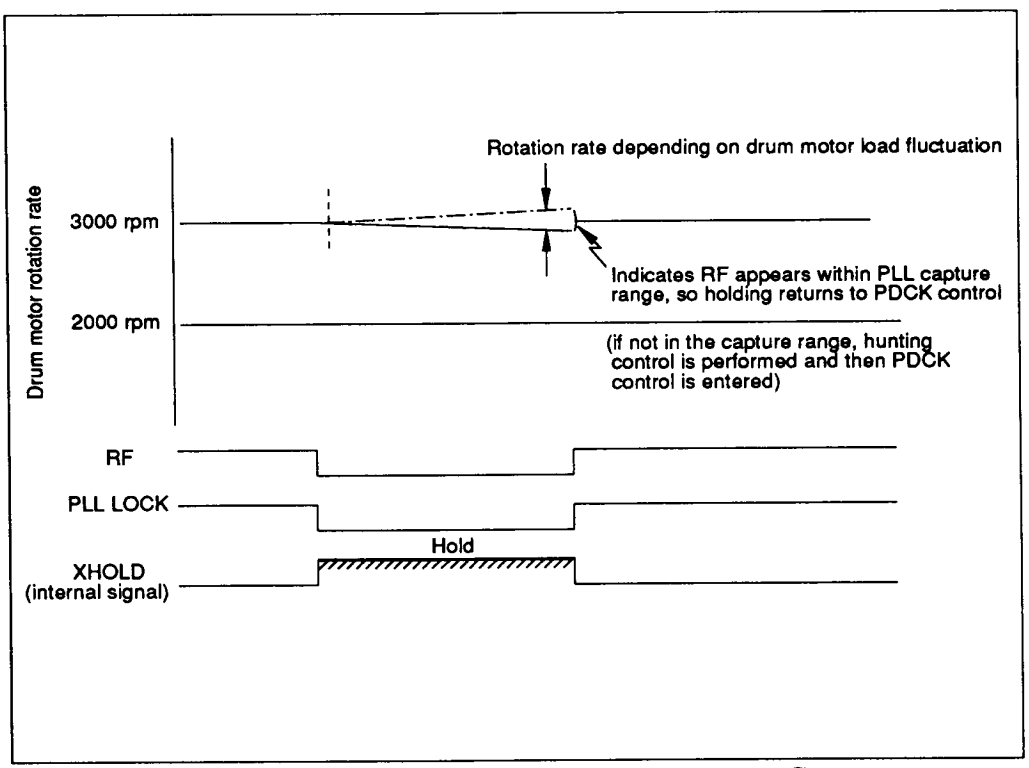

Figure 51 Drum Motor Rotation Rate During Hold Control

Table 27 Drum Motor Abnormal Rotation Rate Detection Values

FG	FF search / REW search	Unit
666.6 Hz	1734	rpm
	435	
800 Hz	1445	rpm
	363	

Note: During hold control mode.

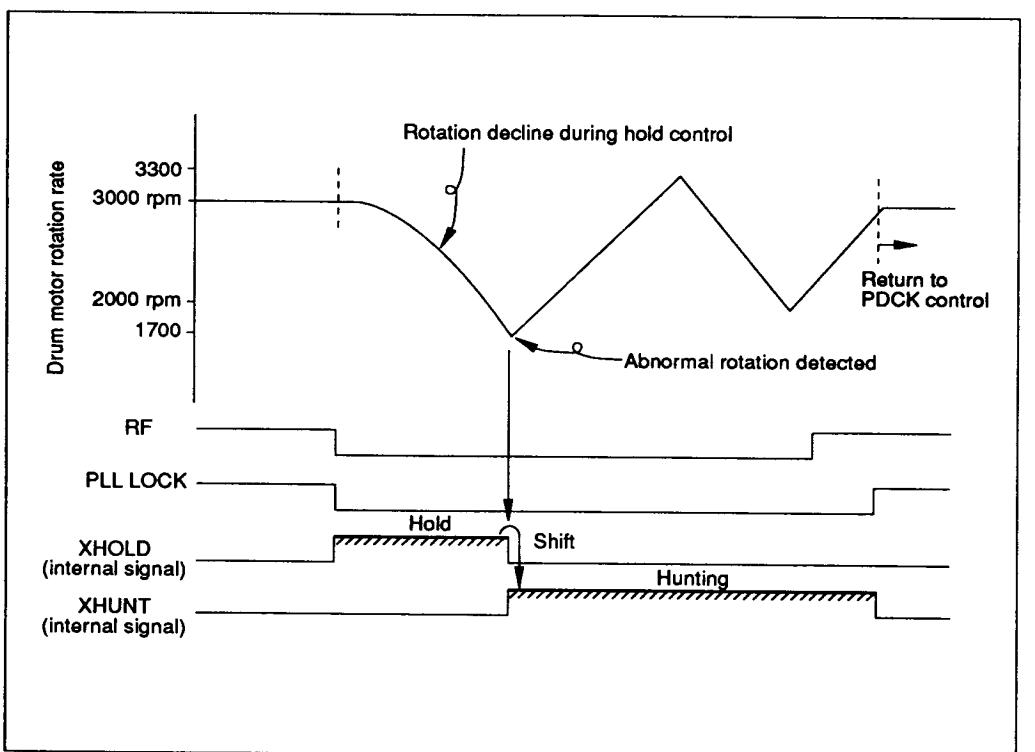

Figure 52 Drum Motor Rotation Rate when Abnormal Rotation Detected

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Table 28 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Pin voltage	V_T	–0.3 to V_{DD} +0.3	V
Maximum allowable loss	P_T	400	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Table 29 Electrical Characteristics (Ta = 25 °C, V_{DD} = 5 V)

Item		Symbol	Applied pins	Min	Typ	Max	Unit	Conditions
Power supply voltage		V_{DD}	AV_{DD}, DV_{DD}	4.5	5.0	5.5	V	
Input voltage	"H" level	V_{IH}	Digital	0.7 V_{DD}	—	—	V	
	"L" level	V_{IL}		—	—	0.3 V_{DD}	V	
Input leak current		I_{LI}		—	—	1	µA	$0 \le V_i \le V_{DD}$
Input pin pull-up resistance		Rpu	Pull-up	10	20	40	kΩ	
Output voltage	"H" level	V_{OH}	Digital	V_{DD}–0.5	—	—	V	$-I_{OH}$ = 0.4 mA
	"L" level	V_{OL}		—	—	0.4	V	I_{OL} = 0.4 mA
Power supply operating current		I_{DD}		—	+8	—	mA	