HD49315AF

CMOS 10-Bit A/D Converter

HITACHI

ADE-207-160 (Z)
Preliminary, 1st Edition
Jan. 1995

Description

The HD49315AF is a high-speed, low-power monolithic CMOS 10-bit Analog-to-Digital (A/D) converter LSI.

Application

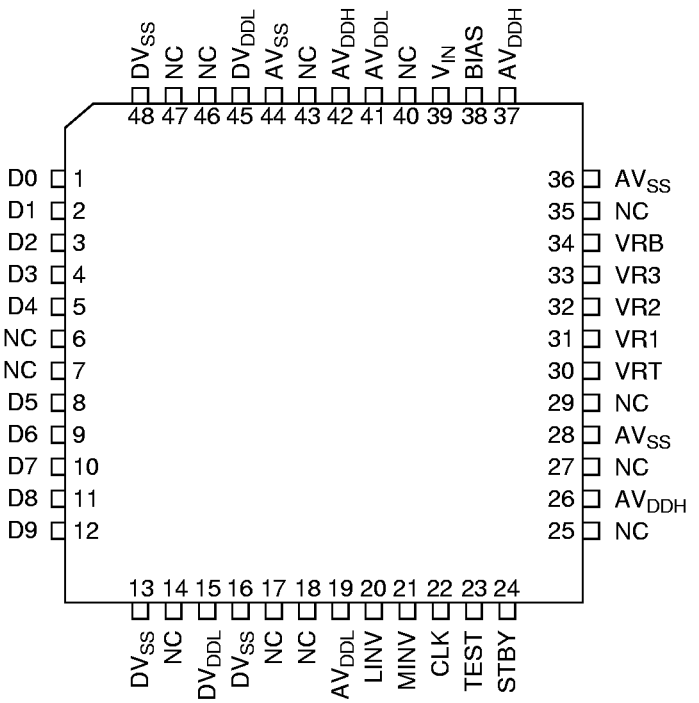
- Digital video processing including digital VCR and digital TV.

Features

- Resolution: 10 bits
- Maximum conversion rate: 15 Msps (Min)
- Power dissipation: 115 mW (Typ)
- Standby mode provided (low-power waiting mode)
- Operating supply voltage: +4.75 V, +3.3 V (Split supply)

Pin Arrangement

FP- 48



(Top View)

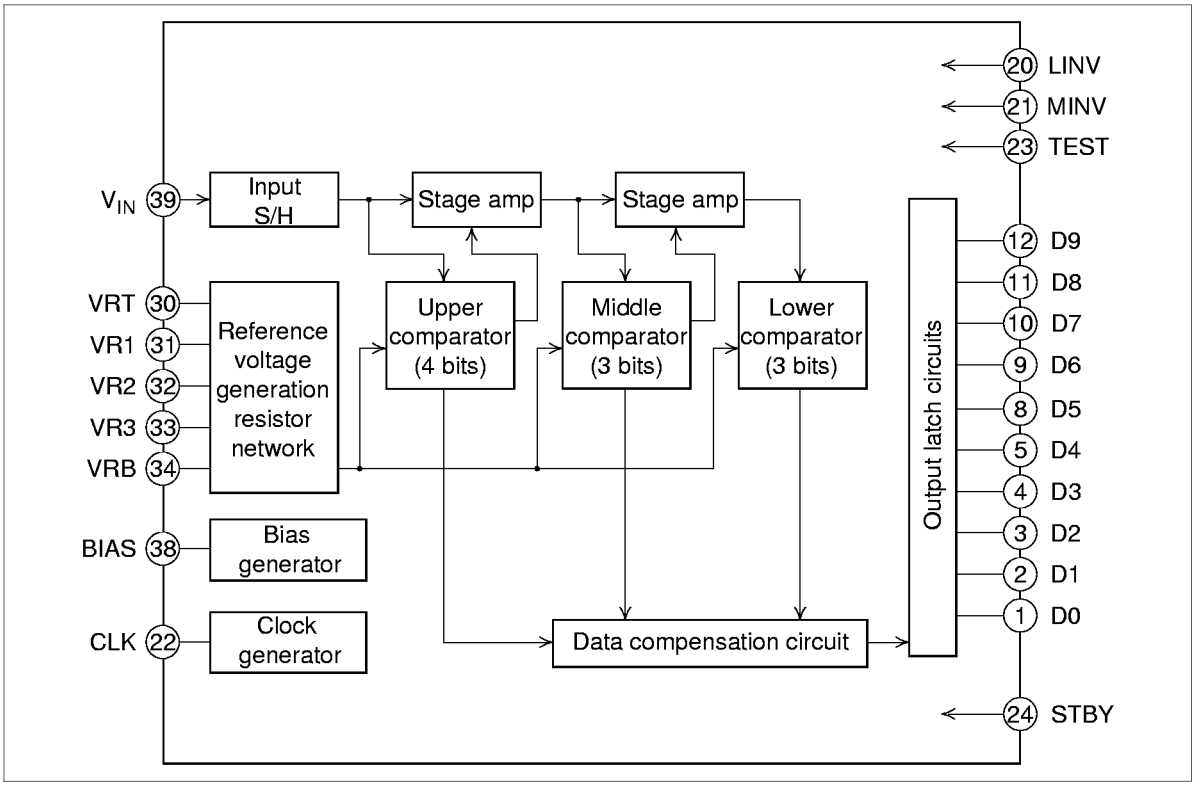
Pin Description

Pin No.	Symbol	Function	Description	I/O
1	D0	Digital output (LSB)		O
2 to 5	D1 to D4	Digital output		O
6, 7	NC	Unused		—
8 to 11	D5 to D8	Digital output		O
12	D9	Digital output (MSB)		O
13	DV_{SS}	Digital ground (0 V)	Connect this pin in common with AV_{SS} external to the IC	—
14	NC	Unused		—
15	DV_{DDL}	Digital power supply (3.3 V)	Connect this pin in common with AV_{DDL} external to the IC	—
16	DV_{SS}	Digital ground (0 V)	Connect this pin in common with AV_{SS} external to the IC	—
17, 18	NC	Unused		—
19	AV_{DDL}	Analog power supply (3.3 V)		—
20	LINV	H: D0 to D8 invert L: Normal operation (0 to DV_{DDL})	Pull-up internal to DV_{DDL}	I
21	MINV	H: D9 invert L: Normal operation (0 to DV_{DDL})	Pull-up internal to DV_{DDL}	I
22	CLK	Conversion clock input (0 to DV_{DDL})		I
23	TEST	H: Test mode L: Normal operation (0 to DV_{DDL})	Pull-up internal to DV_{DDL}	I
24	STBY	H: Standby mode L: Normal operation (0 to DV_{DDL})	Pull-up internal to DV_{DDL}	I
25	NC	Unused		—
26	AV_{DDH}	Analog power supply (4.75 V)		—
27	NC	Unused		—
28	AV_{SS}	Analog ground (0 V)		—
29	NC	Unused		—
30	VRT	Reference voltage input (high side: 4.0 V)	Insert a 0.1 µF ceramic capacitor between this pin and AV_{SS}	I
31 to 33	VR1 to VR3	Center tap for reference voltage	Insert a 0.1 µF ceramic capacitor between this pin and AV_{SS}	—
34	VRB	Reference voltage input (low side: 2.0 V)	Insert a 0.1 µF ceramic capacitor between this pin and AV_{SS}	I

Pin Description (cont)

Pin No.	Symbol	Function	Description	I/O
35	NC	Unused		—
36	AV_{SS}	Analog ground (0 V)		—
37	AV_{DDH}	Analog power supply (4.75 V)		—
38	BIAS	Internal bias pin	Insert a 39 kΩ resistor between this pin and AV_{DDH}, and insert a 0.1 µF ceramic capacitor between this pin and AV_{SS}	—
39	V_{IN}	Analog signal input (2 to 4 V)		—
40	NC	Unused		—
41	AV_{DDL}	Analog power supply (3.3 V)		—
42	AV_{DDH}	Analog power supply (4.75 V)		—
43	NC	Unused		—
44	AV_{SS}	Analog ground (0 V)		—
45	DV_{DDL}	Digital power supply (3.3 V)	Connect this pin in common with AV_{DDL} external to the IC	—
46	NC	Unused		—
47	NC	Unused		—
48	DV_{SS}	Digital ground (0 V)	Connect this pin in common with AV_{SS} external to the IC	—

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Units
Power supply voltage	$V_{DD(max)}$	6.0	V
Analog input pin voltage	$V_{IN(max)}$	–0.3 to AV_{DDH} + 0.3	V
Reference pin voltage	$V_{REF(max)}$	–0.3 to AV_{DDH} + 0.3	V
Digital input voltage	$V_{I(max)}$	–0.3 to DV_{DDL} + 0.3	V
Reference pin voltage difference	$V_{RT} – V_{RB}$	2.5	V
Power dissipation	$P_{D(max)}$	400	mW
Operating temperature	Topr	–10 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Notes: 1. V_{DD} refers to AV_{DDH}, AV_{DDL}, and DV_{DDL}.
2. Connect AV_{DDL} and DV_{DDL} to a common point outside the IC. If AV_{DDL} and DV_{DDL} are separated by a noise filter, make sure that their voltages differ by less than 0.3 V on power up, and by less than 0.1 V during operation.
3. Connect AV_{SS} and DV_{SS} to a common point outside the IC.

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, AV_{DDH} = 4.75 V, AV_{DDL} = 3.3 V, DV_{DDL} = 3.3 V, V_{RT} = 4.0 V, V_{RB} = 2.0 V, R_{EXT} = 39 kΩ)

Item	Symbol	Min	Typ	Max	Units	Test conditions
Resolution	RES	10	10	10	bit	
Power supply voltage range	V_{DDH}	4.50	4.75	5.25	V	V_{DDL} = 3.3 V, f_{CLK} = 15 MHz (duty 50%), f_{IN} = 3.751 MHz sine wave
	V_{DDL}	2.7	3.3	V_{DDH}	V	V_{DDH} = 4.75 V
Supply current	I_{DDH}*1	—	16.0	20.0	mA	f_{IN} = 1 kHz sine wave,
	I_{DDL}*2	—	11.8	15.0	mA	f_{CLK} = 15 MHz (duty 50%) V_{IN} = 2 Vp-p
Standby current	I_{STBYH}*1	—	—	100	µA	CLK: 0 V fixed
	I_{STBYL}*2	—	—	100	µA	Other digital I/O pins open
Reference resistance	R_{REF}	400	620	—	Ω	Resistance between V_{RT} and V_{RB}
Input range	V_{INp-p}*3	1.95	—	2.08	V	
Offset voltage	E_{OB}*4	–50	—	+50	mV	Bottom side
Analog input current	I_{IN}*5	–8	—	+8	µA	f_{CLK} = 15 MHz V_{IN} = 2 to 4 V: DC voltage
Analog input capacitance	C_{IN}*6	—	(10)	—	pF	

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, AV_{DDH} = 4.75 V, AV_{DDL} = 3.3 V, DV_{DDL} = 3.3 V, V_{RT} = 4.0 V, V_{RB} = 2.0 V, R_{EXT} = 39 kΩ) (cont)

Item	Symbol	Min	Typ	Max	Units	Test conditions
Analog input bandwidth	BW	–1	—	—	dB	f_{IN} = 10 MHz
Digital input current	I_{IH}	—	—	50	µA	$V_{IH} = V_{DDL}$
	I_{IL} (CLK)	–50	—	—	µA	V_{IL} = 0 V
	I_{IL}	–200	—	—	µA	V_{IL} = 0 V
Digital input voltage	V_{IH}	2.0 × DV_{DDL} / 3.3	—	DV_{DDL}	V	
	V_{IL}	0	—	0.8 × DV_{DDL} / 3.3	V	
Conversion frequently	f_{CLK}	2	—	15	MHz	
Clock pulse width	t_{WH}*7	31	—	300	ns	V_{DDL} = 4.75 V, f_{CLK} = 15 MHz f_{IN} = 3.751 MHz, sine wave
		27	—	300	ns	V_{DDL} = 3.30 V, f_{CLK} = 15 MHz f_{IN} = 3.751 MHz, sine wave
		27	—	300	ns	V_{DDL} = 2.70 V, f_{CLK} = 15 MHz f_{IN} = 3.751 MHz, sine wave
	t_{WL}*7	27	—	300	ns	V_{DDL} = 4.75 V, f_{CLK} = 15 MHz f_{IN} = 3.751 MHz, sine wave
		27	—	300	ns	V_{DDL} = 3.30 V, f_{CLK} = 15 MHz f_{IN} = 3.751 MHz, sine wave
		31	—	300	ns	V_{DDL} = 2.70 V, f_{CLK} = 15 MHz f_{IN} = 3.751 MHz, sine wave
Digital output delay	t_{PD}	—	—	47	ns	V_{DDL} = 3.3 V, C_L = 10 pF
time		—	—	52	ns	V_{DDL} = 2.7 V, C_L = 10 pF
Digital output hold	t_{HOLD}	15	—	—	ns	V_{DDL} = 3.3 V, C_L = 10 pF
time		20	—	—	ns	V_{DDL} = 2.7 V, C_L = 10 pF
Digital output enable	t_{ZH}	—	—	500	ns	R_L = 2 kΩ, C_L = 10 pF
time	t_{ZL}	—	—	500	ns	R_L = 2 kΩ, C_L = 10 pF
Digital output	t_{HZ}	—	—	500	ns	R_L = 2 kΩ, C_L = 10 pF
disable time	t_{LZ}	—	—	500	ns	R_L = 2 kΩ, C_L = 10 pF
Analog signal read-in time	t_{AP}	–5	—	10	ns	
Integration linearity	INL +	—	+1.0	+2.0	LSB	f_{CLK} = 15 MHz
error	INL –	–2.0	–1.0	—	LSB	

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, AV_{DDH} = 4.75 V, AV_{DDL} = 3.3 V, DV_{DDL} = 3.3 V, V_{RT} = 4.0 V, V_{RB} = 2.0 V, R_{EXT} = 39 kΩ) (cont)

Item	Symbol	Min	Typ	Max	Units	Test conditions
Differentiation	DNL +*8	0	+0.5	+0.8	LSB	f_{CLK} = 15 MHz
linearity error	DNL –*8	–0.8	–0.5	—	LSB	
Digital output	I_{OZH}	—	—	50	µA	$V_{STBY} = V_{DDL}$, $V_{OUT} = V_{DDL}$
current	I_{OZL}	–50	—	—	µA	$V_{STBY} = V_{DDL}$, V_{OUT} = 0 V
Digital output	V_{OH}	DV_{DDL} – 0.5	—	—	V	I_{OH} = –2 mA
voltage	V_{OL}	—	—	0.5	V	I_{OL} = 2 mA

Notes: 1. I_{DDH}, I_{STBYH} is Quiescent of AV_{DDH}

2. I_{DDL}, I_{STBYL} is Quiescent of A_{VDDL} + DV_{DDL}

3. $V_{INp-p} = V_{IN(1022\rightarrow1023)} - V_{IN(0\rightarrow1)}$

   $V_{IN(1022\rightarrow1023)}$: Input voltage when the output code of A/D converter change from 1022 to 1023.

   $V_{IN(0\rightarrow1)}$: Input voltage when the output code of A/D converter change from 0 to 1.

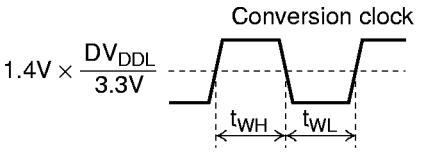
4. The offset voltage (E_{OB}) is the difference between V_{RB} and the input voltage at which the output code changes from 0 to 1 ($V_{IN(0\rightarrow1)}$). The offset is positive if $V_{IN(0\rightarrow1)}$ is higher than V_{RB}, and negative if $V_{IN(0\rightarrow1)}$ is lower than V_{RB}.

   $E_{OB} = V_{IN(0\rightarrow1)} - V_{RB}$

   The offset voltage (E_{OB}) has V_{DDL} (AV_{DDL}, DV_{DDL}) dependence. (+50 mV/V)

5. I_{IN} is not transition current, but static current.

6. Reference value

7. 

8. DNL calculate the difference of linearity error between next two codes.

Function Table

				Digital output										
STBY	**TEST**	**LINV**	**MINV**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Operation mode**
H	X	X	X	High-Z										Lower power standby
L	L	L	L	Code table as follows										Normal operation
		L	H	In the code table below, D9 is inverted										
		H	L	In the code table below, D8 to D0 are inverted										
		H	H	In the code table below, D9 to D0 is inverted										
	H	L	L	L	H	L	H	L	H	L	H	L	H	Test mode
		L	H	H	H	L	H	L	H	L	H	L	H	
		H	L	L	L	H	L	H	L	H	L	H	L	
		H	H	H	L	H	L	H	L	H	L	H	L	

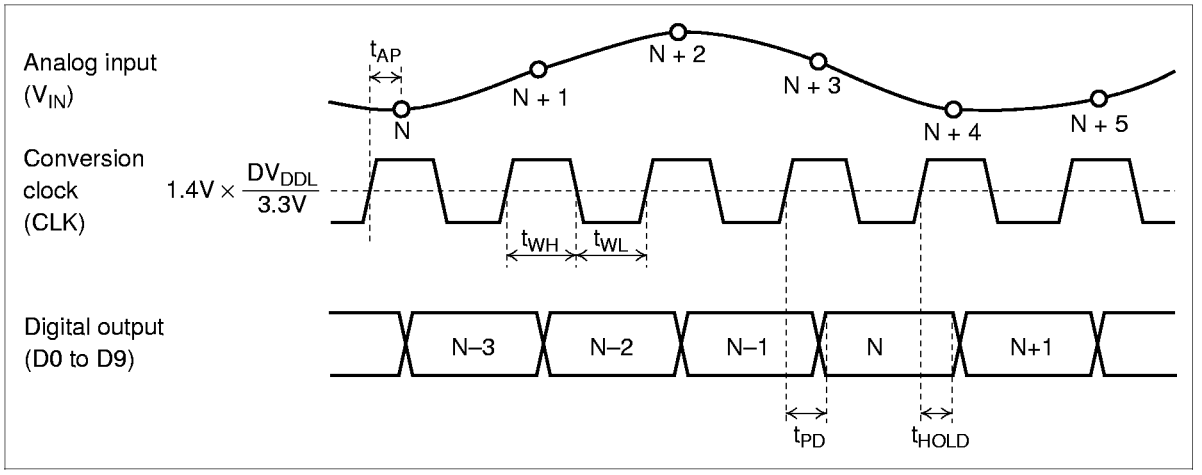
Note: L: Low level, H: High level, X: High or Low level.
STBY, TEST, LINV and MINV are pulled up internal to DV_{DDL}.

Output Code Table

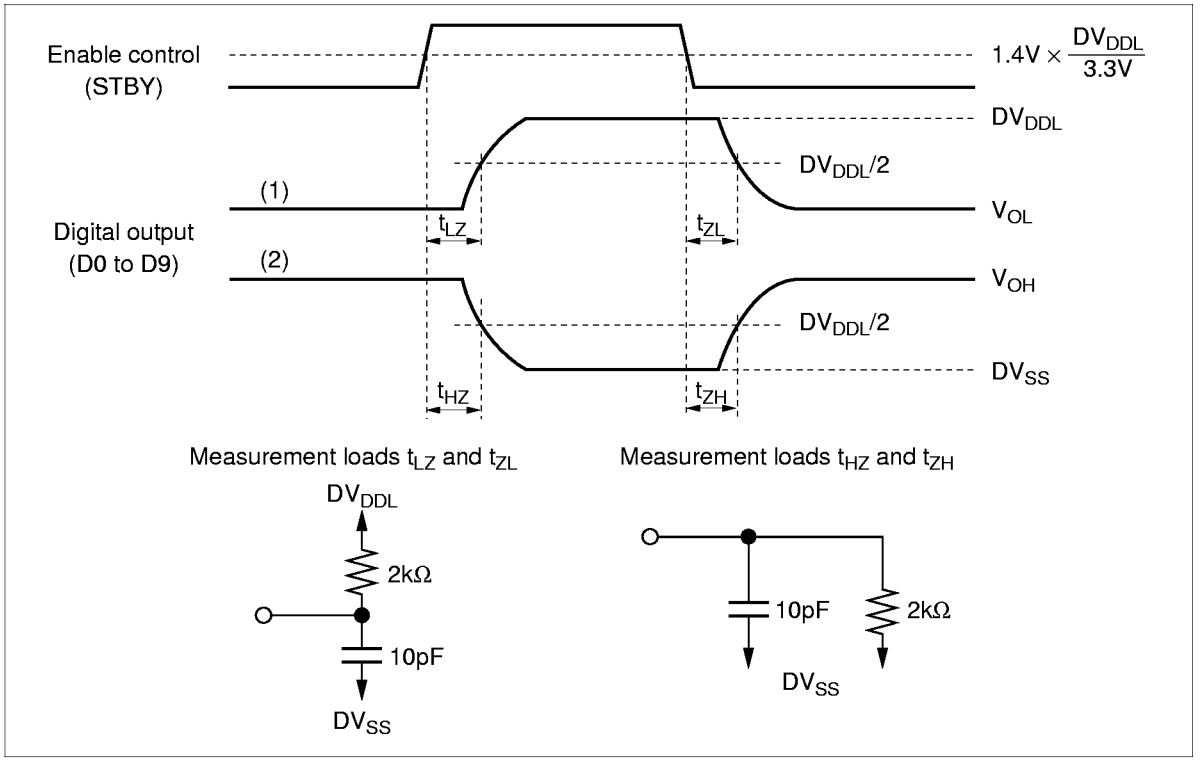
Output code			**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Step	(VRB)	0	L	L	L	L	L	L	L	L	L	L
		1	L	L	L	L	L	L	L	L	L	H
		2	L	L	L	L	L	L	L	L	H	L
		3	L	L	L	L	L	L	L	L	H	H
		511	L	H	H	H	H	H	H	H	H	H
		512	H	L	L	L	L	L	L	L	L	L
		1020	H	H	H	H	H	H	H	H	L	L
		1021	H	H	H	H	H	H	H	H	L	H
		1022	H	H	H	H	H	H	H	H	H	L
	(VRT)	1023	H	H	H	H	H	H	H	H	H	H

Note: L: Low level, H: High level.

Timing Chart

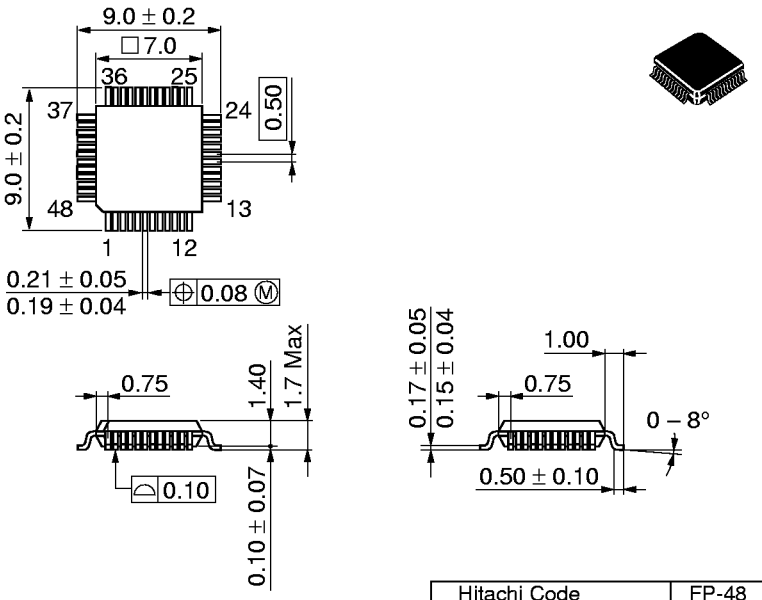


3-State Control



Package Dimension

Unit: mm



Hitachi Code	FP-48
JEDEC Code	—
EIAJ Code	ED-7404A
Weight	0.17 g

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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071