HD49409FS

P-in-P Controller (with Built-in A/D, D/A Converters)

Description

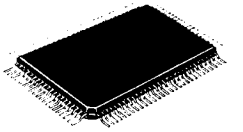
The HD49409FS is a memory controller for P-in-P (picture-in-picture) systems and incorporates a 1-channel 6-bit A/D converter, a 2-channel 8-bit D/A converter, a 3-channel multiplexer, a 4 f_{sc} PLL circuit, and oscillators for memory read/write operations.
By combining this IC with four additional ICs (the HA118088, HA11532, HA11525, and HM53461), it is possible to construct a five-chip P-in-P system.

Functions

- P-in-P system memory controller
- 3-channel multiplexer with clamping function
- 1-channel, 6-bit 2.4 Msps A/D converter
- 2-channel, 8-bit 14 Msps D/A converter
- 4 f_{sc} (14 MHz) PLL
- Memory read oscillator, memory write oscillator

Features

- A P-in-P system can be constructed by combining this IC with four other ICs (HA118088, HA11532, HA11525, and HM53461).
- The size of the sub picture can be set to 1/3 or 1/4 the size of the main picture.
- The sub picture can be displayed even when no main picture is input.
- The sub picture can be frozen (Still mode).
- The IC can process S signals (Y/C 2-signal processing).

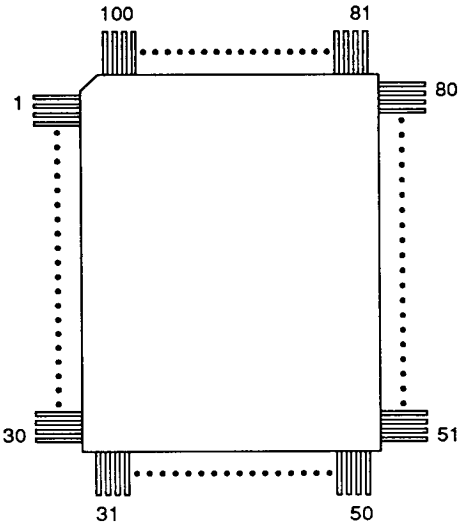


FP-100A

Ordering Information

Type No.	Package
HD49409FS	FP-100A

Pin Arrangement



(Top View)

Pin Functions

Table 1 Pin Function Table

Pin No.	Symbol	Function	I/O system (I/O level)	I/O or impedance	Active level
1	PIP	P-in-P mode input	Schmitt	I	Hi
2	CY	Y signal clamping filter	Analog	(15 k)	
3	CRY	R-Y signal clamping filter	Analog	(2 k)	
4	CBY	B-Y signal clamping filter	Analog	(2 k)	
5	MPXO	Test-use pin			Note: Leave this pin open.
6	REFADJ	ADC reference voltage adjustment	Analog		
7	ADGND	Analog system ground			
8	VRT	ADC reference voltage Hi level input	Analog		

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O system (I/O level)	I/O or Impedance	Active level
9	VB	ADC comparator bias voltage	Analog	Open drain	
10	CSW	Main picture on/off signal input	Schmitt	I	Lo: Main picture off.
11	ADVDD	Analog system V_{DD}			
12	Y	Y signal input	Analog	I: Gate input	
13	BS	Test-use pin	CMOS	I	Note: Fix to Hi.
14	RY	R-Y signal input	Analog	I: Gate input	
15	TN	Test-use pin	CMOS	I	Note: Fix to Hi.
16	BY	B-Y signal input	Analog	I: Gate input	
17	ALLR	Test-use pin	CMOS	I	Note: Fix to Lo.
18	VRM	ADC reference voltage intermediate tap	Analog		
19	VRB	ADC reference voltage Lo level input	Analog		
20	DGND	Digital system ground			
21	DGND	Digital system ground			
22	SIFTC	Sub picture position shift	Schmitt	I	Shifts in a clockwise rotation each time a Lo/Hi pulse is input.
23	M1	DASW control signal	CMOS	I	Hi
24	DGND	Digital system ground			
25	VODD	Oscillator V_{DD}			
26	RCI	Read clock feedback signal	CMOS	O	Hi/Lo
27	RC	Read clock signal input	Schmitt	I	Hi/Lo
28	DATEST	DAC test pin	CMOS	I	Hi: $\overline{\text{PINP}}$ mode Lo: $\overline{\text{PINP}}$
29	MCP	Pedestal clamp timing signal	CMOS	O	Hi
30	OUTC	Sub picture output timing signal	CMOS	O	Hi: Sub picture display period

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O system (I/O level)	I/O or impedance	Active level
31	CLIP	Sub picture noise clip timing signal	CMOS	O	Hi: Clipping period
32	WAKU	Sub picture frame output timing signal	CMOS	O	Hi: Frame output period
33	DACK1	Y-DAC clock	CMOS	I	Hi/Lo
34	DA11	Digital signal input (1)	CMOS	I	Hi/Lo
35	DA12				
36	DA13				
37	DA14				
38	DA15				
39	DA16				
40	REXY	DAC external resistor connection (1)	Analog		7.2 kΩ external resistor connected to V_{DD}
41	CBLY	DAC bypass capacitor connection (1)	Analog		
42	VREFY	DAC reference voltage input (1)	Analog	I: Gate input	
43	YO	Y signal output	Analog	O	150 Ω external resistor connected to V_{DD}
44	DAVDD	DAC V_{DD}			
45	REXC	DAC external resistor connection (2)	Analog		7.2 kΩ external resistor connected to V_{DD}
46	VREFC	DAC reference voltage input (2)	Analog	I: Gate input	
47	CBLC	DAC bypass capacitor connection (2)	Analog		
48	CO	C signal output	Analog	O	150 Ω external resistor connected to V_{DD}
49	DAGND	GND			
50	DACK2	C-DAC clock	CMOS	I	Hi/Lo

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O system (I/O level)	I/O or impedance	Active level
51	DA21	Digital signal input (2)	CMOS	I	Hi/Lo
52	DA22				
53	DA23				
54	DA24				
55	DA25				
56	DA26				
57	DA27				
58	DA28				
59	DACONT	Test-use pin	CMOS	I	Note: Fix to Hi.
60	SUB VDD	Substrate V_{DD}			
61	CP	PLL phase comparator filter	Analog	(80 k)	
62	PLLGND	PLL ground			
63	FSCI	Main picture burst lock f_{SC} input	Analog	I	
64	PLLVDD	PLL V_{DD}			
65	DVDD	Digital system V_{DD}			
66	SO2	Memory read data input	TTL	I	Hi/Lo
67	SO3				
68	SO1				
69	SO4				
70	SC	Serial read clock output	CMOS	O	Hi/Lo

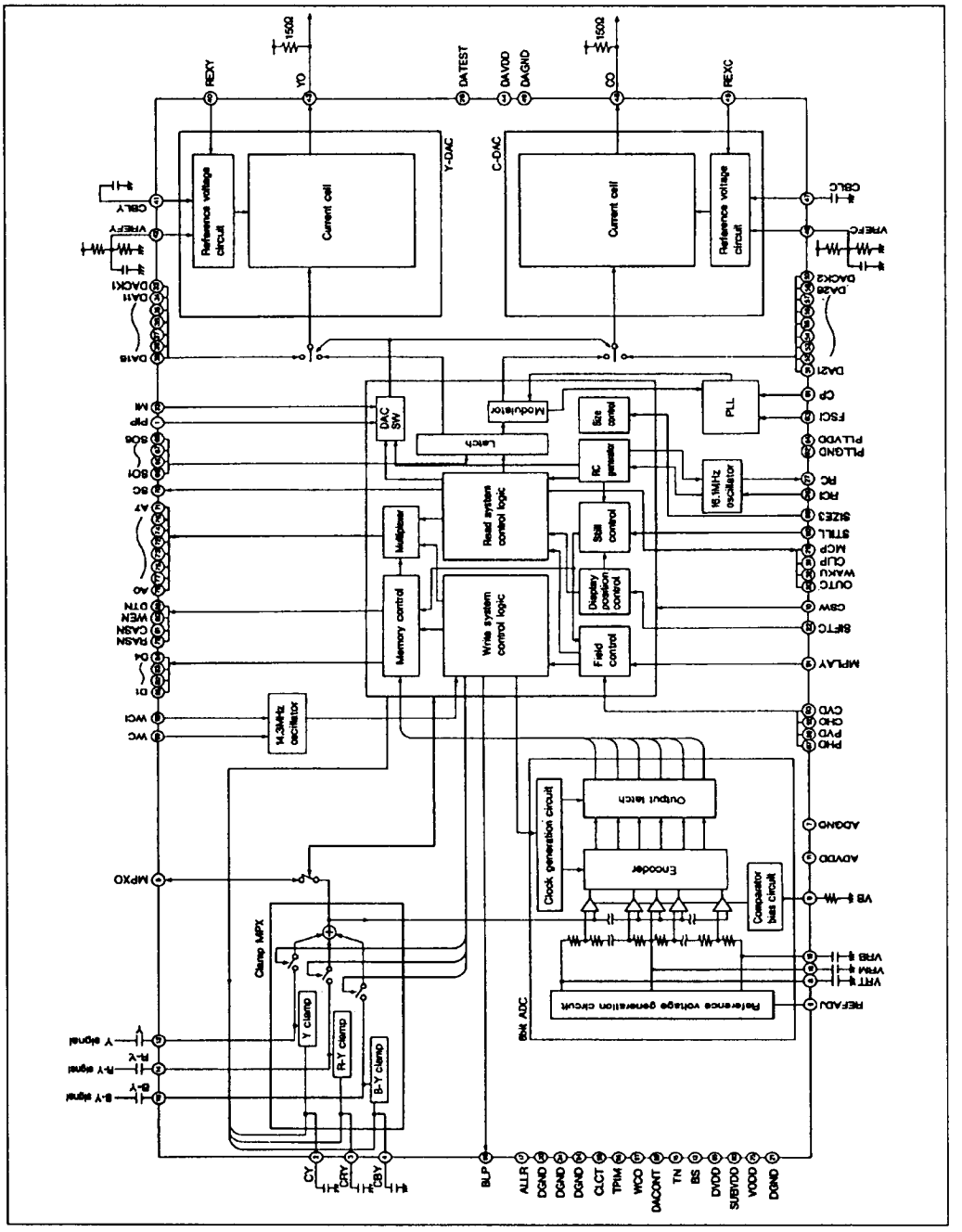
Pin Function Table (cont)

Pin No.	Symbol	Function	I/O system (I/O level)	I/O or impedance	Active level
71	A7 (MSB)	Memory address data output	CMOS	O	Hi/Lo
72	A4				
73	A3				
74	A5				
75	A2				
76	A6				
77	A1				
78	RASN	Memory row address assigned output	CMOS	O	When Hi changes to Lo
79	A0 (LSB)	Memory address data output	CMOS	O	Hi/Lo
80	WEN	Sub picture data write control output	CMOS	O	Hi: Write inhibited
81	CASN	Memory column address assigned output	CMOS	O	When Hi changes to Lo
82	D2	Memory write data output	CMOS	O	Hi/Lo
83	D3				
84	D4				
85	D1				
86	DTN	Memory data transmission mode/ read mode control output	CMOS	O	Lo: Data transmission mode Hi: Read mode
87	PHD	Main picture horizontal sync signal input	Schmitt	I	Hi
88	PVD	Main picture vertical sync signal input	Schmitt	I	Hi
89	SIZE3	Sub picture size control	CMOS	I	Hi: 1/3 mode Lo: 1/4 mode
90	STILL	Sub picture still mode control	CMOS	I	Hi
91	MPLAY	Control signal for special playback	CMOS	I	Hi

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O system (I/O level)	I/O or impedance	Active level
92	CHD	Sub picture horizontal sync signal input	Schmitt	I	Hi
93	CVD	Sub picture vertical sync signal input	Schmitt	I	Hi
94	DGND	Digital system ground			
95	CLCT	Test-use pin	CMOS	I	Note: Fix to Hi.
96	TRIM	Test-use pin	CMOS	I	Note: Fix to Lo.
97	WCO	Test-use pin	CMOS	I/O	Note: Fix to Lo.
98	BLP	Blanking pulse output	CMOS	O	Hi
99	WC	Write clock signal input	Schmitt	I	Hi/Lo
100	WCI	Write clock feedback signal	CMOS	O	Hi/Lo

Block Diagram



P-in-P System Block Diagram