HD614P180/HD40P4281/ HD40P42161

Description

The HD614P180/HD40P4281/HD40P42161 are 4-bit single-chip microcomputers which can be mounted by a standard EPROM 27128/27256 for program memory.

The HD614P180 is pin-compatible with the mask ROM HMCS412C, but has some differences. By modifying the program in the EPROM, it can be used for the evaluation of the HMCS412C or for small-scale production.

Features

- Applicable for 4- or 8-Kword × 10-bit EPROM
  - — 8192-word × 10-bit: HN27128A
  - — 16384-word × 10-bit: HN27C256
- 576-digit × 4-bit RAM (HD614P180)
- 1 timer/counter (HD614P180)
  2 timer/counters (HD40P4281/HD40P42161)
- 3 interrupt sources (HD614P180)
  5 interrupt sources (HD40P4281/HD40P42161)
- Subroutine stack up to 16 levels, including interrupts
- Minimum instruction execution time
  - — 1.33 µs (HD614P180)
  - — 0.89 µs (HD40P4281/HD40P42161)
- 2 low power modes
  - — Standby mode
  - — Stop mode
- On-chip oscillator
  - — Crystal resonator or ceramic filter resonator (also externally drivable)
- Power voltage range: 5 V ±10%
- I/O pin circuit types:
  - — All standard pins are without pull-up MOS
  - — All high voltage pins are without pull-down MOS
- 42-pin EPROM on-package

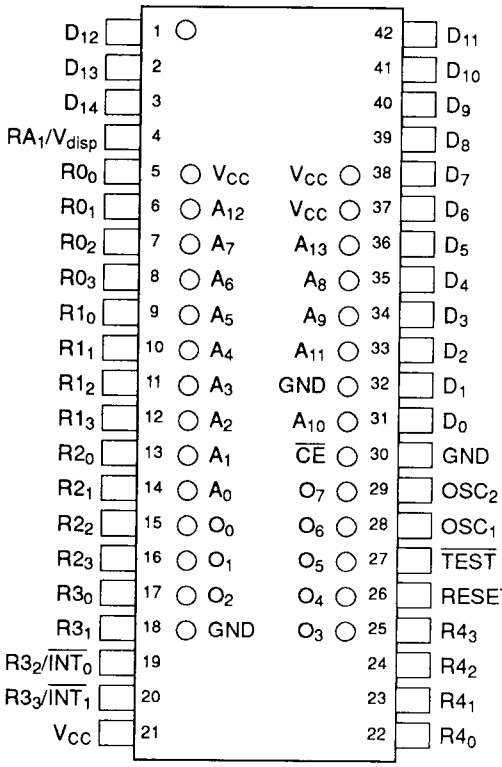
Recommended EPROMs

Type	Program Memory Capacity	f_{OSC} (MHz)	EPROM Type No.
HD614P180 HD40P4281*	8192 words	8	HN27128A series
HD40P42161*	16384 words	4	HN27256 series HN27C256 series HN27C256A series HN27C256H series
		8	

* Under development

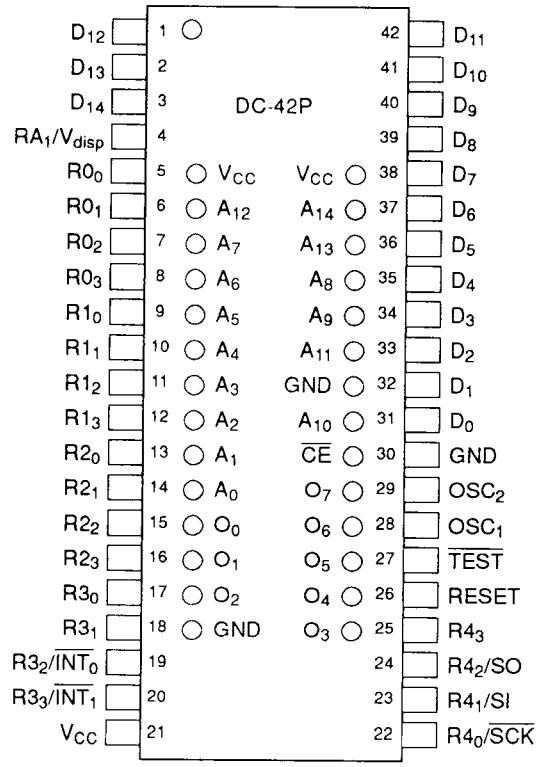
Pin Arrangement

HD614P180
HD40P4281



(Top view)

HD40P42161



(Top view)

Pin Functions

Power Supply

V_{CC}: Connect the V_{CC} power supply voltage to this pin.

GND: Connect to ground.

V_{disp}: The RA_1/V_{disp} pin is used as RA_1 for all high voltage pins which are without pull-down MOS (PMOS open drain).

$\overline{TEST}$: Non-user application pin. Connect it to V_{CC}.

RESET: MCU reset pin. For details, see the Reset section.

Oscillators

OSC_1, OSC_2: Internal clock generator circuit input pins. These can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuit. Refer to the Internal Oscillator Circuit section for details.

Ports

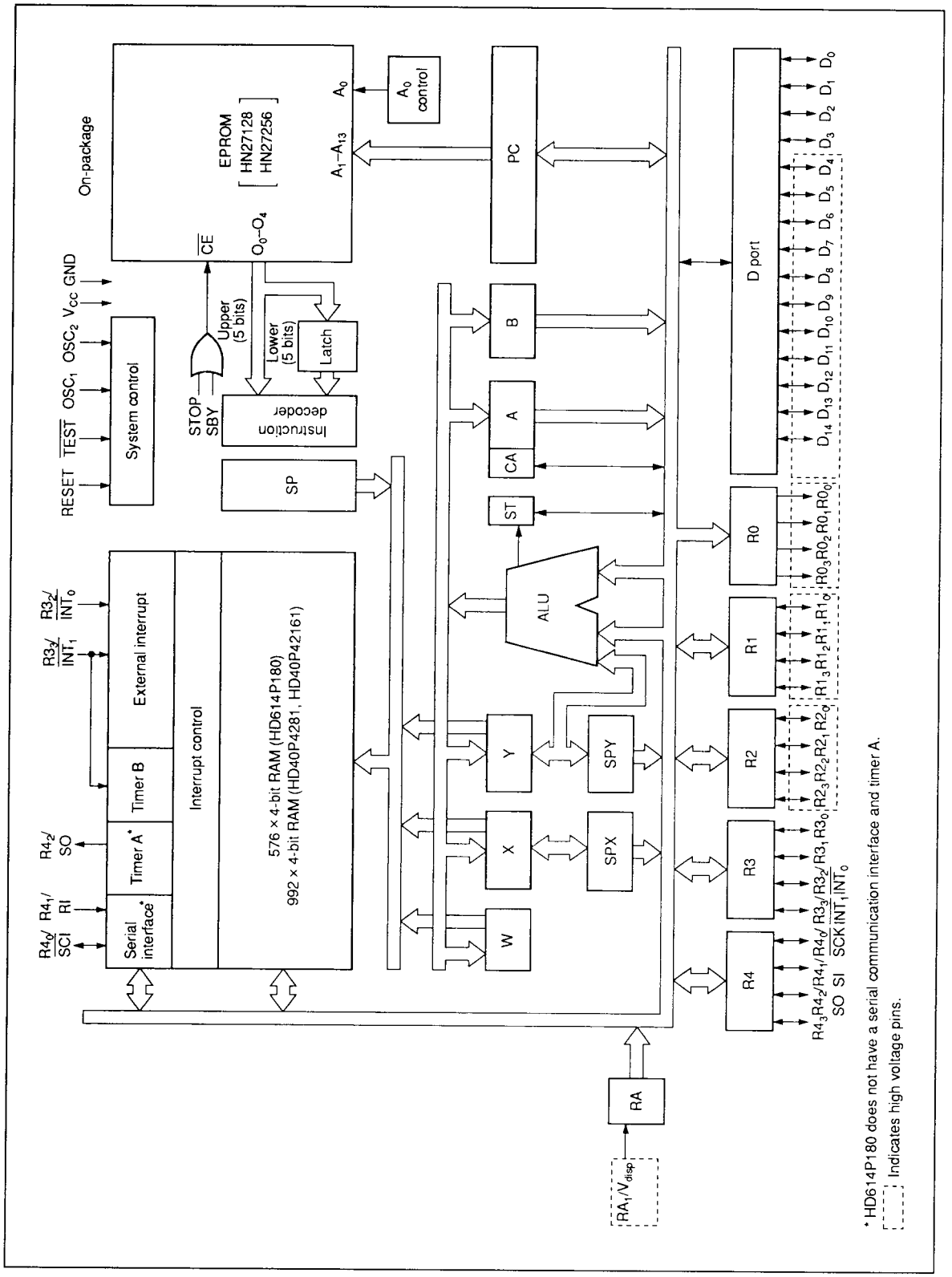
D_0 to D_{14} (D Port): 1-bit common I/O port. D_0 to D_3 are standard types and D_4 to D_{14} are for high voltage. For details, see the Input/Output section.

R0 to R4, RA (R Ports): 4-bit I/O ports. Only RA is a 2-bit port. R0 is an output port, RA is an input port, and R1 to R4 are common I/O ports. R0 to R2 and RA are the high voltage ports, and R3 to R4 are the standard ports. $R3_2$ and $R3_3$ are also available as $\overline{INT_0}$ and $\overline{INT_1}$, respectively. Refer to the Input/Output section for details.

Interrupts

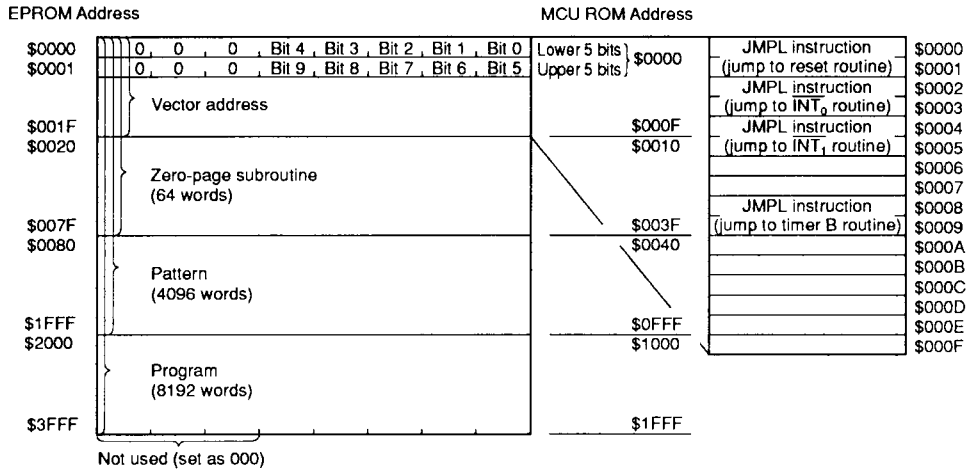
$\overline{INT_0}$, $\overline{INT_1}$: External interrupt input pins. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are also available as $R3_2$ and $R3_3$, respectively. Refer to the Interrupt section for details.

Block Diagram

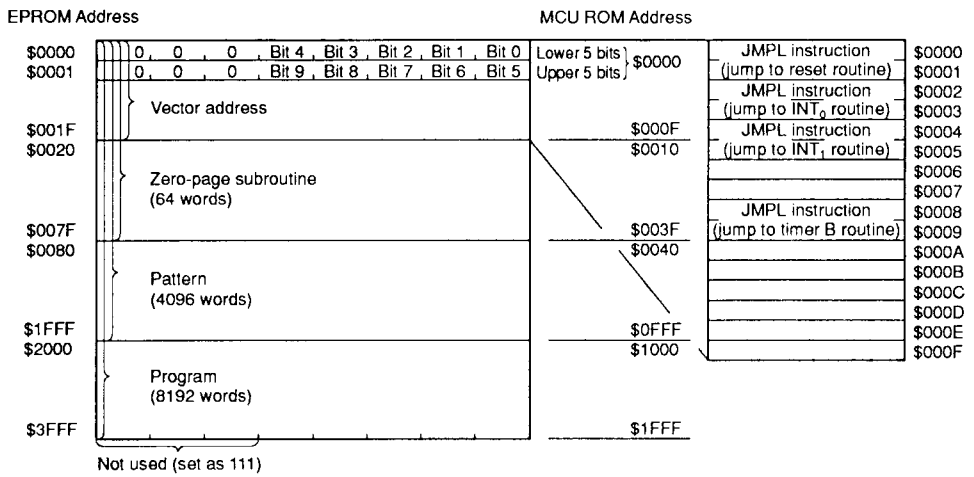


Memory Map

ROM Memory Map



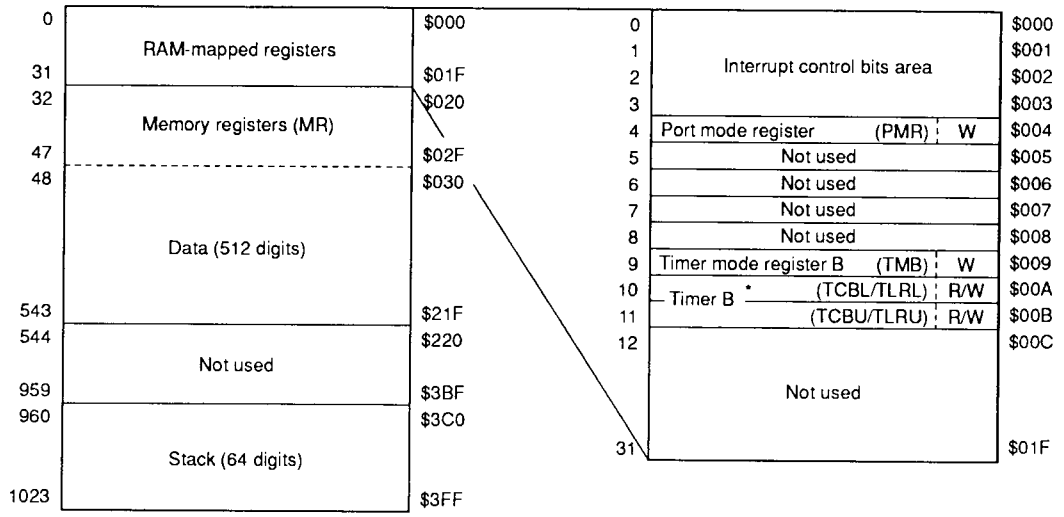
HD614P180, HD40P4281



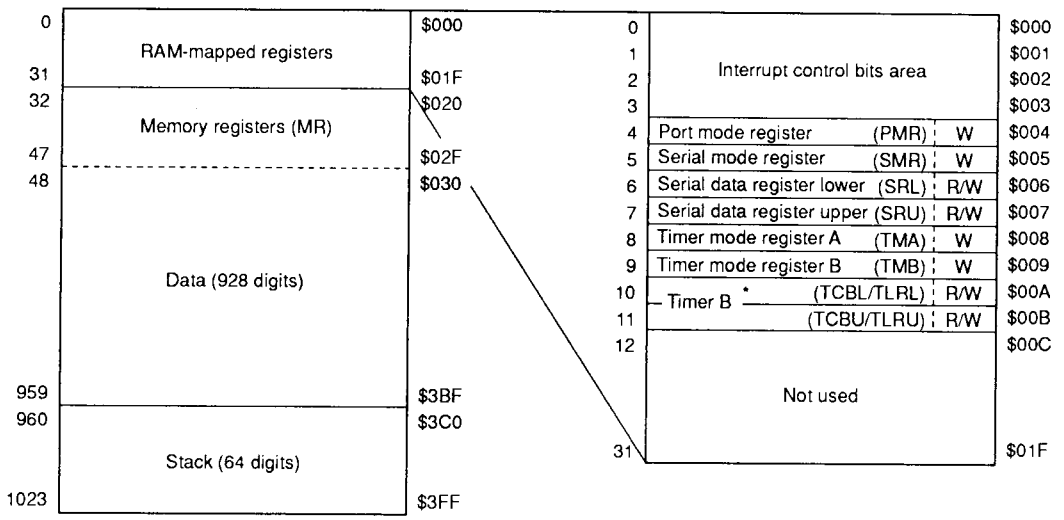
HD40P42161

Figure 1 ROM Memory Map

RAM Memory Map



HD614P180



HD614P4281, HD614P42161

* Two registers are mapped on the same address.

R: Read only
W: Write only
R/W: Read/write

Timer counter B lower (TCBL)	R	Timer load register B lower (TLRL)	W	$00A
Timer counter B upper (TCBU)	R	Timer load register B upper (TLRU)	W	$00B

Figure 2 RAM Memory Map

Internal Oscillator Circuit

Figure 3 shows the block diagram of the internal oscillator circuit. The oscillator type can be selected as a crystal resonator or ceramic filter resonator as shown in table 1. In any case, an external clock operation is available.

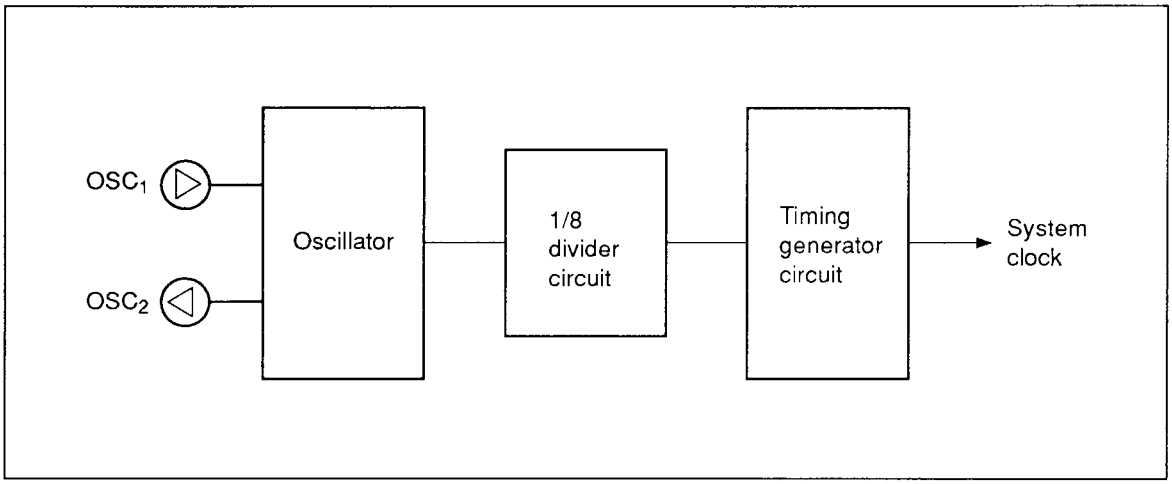


Figure 3 Internal Oscillator Circuit

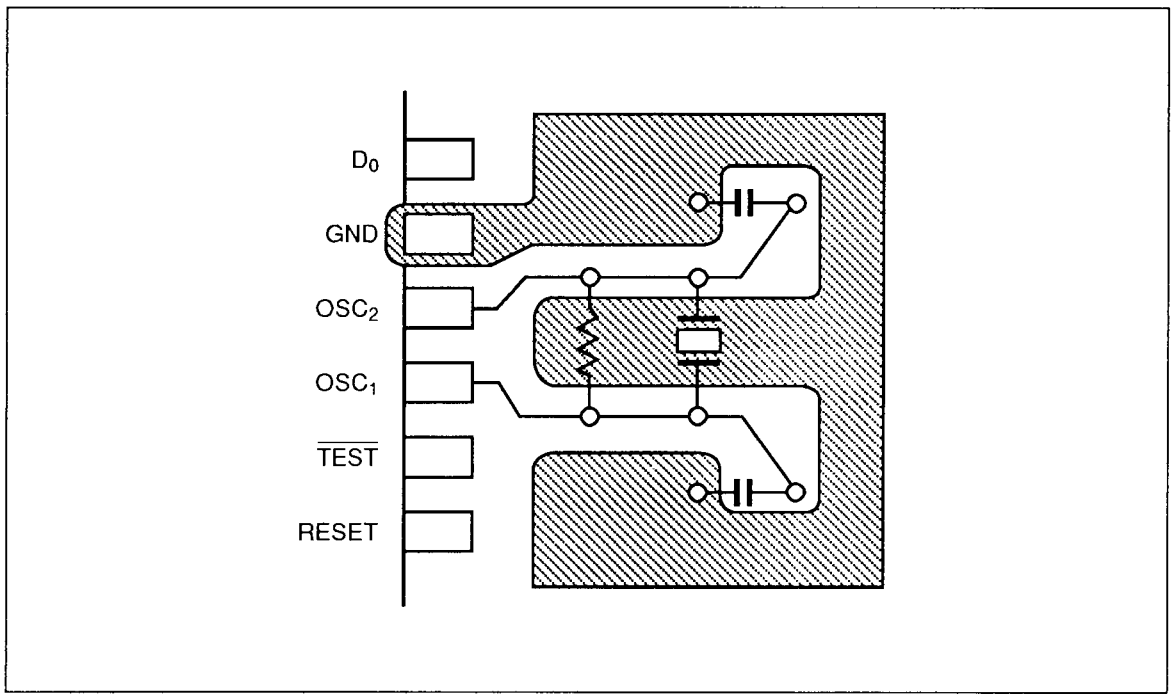
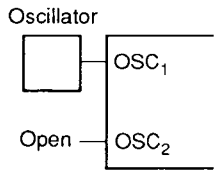
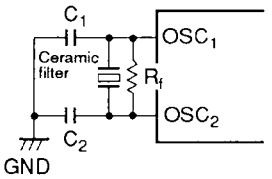
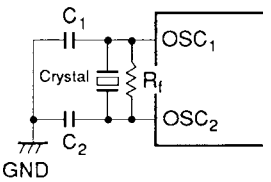
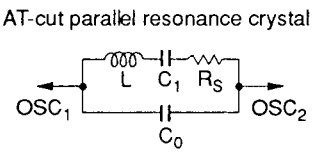


Figure 4 Layout of Crystal and Ceramic Filter

Table 1 Oscillator Circuit Examples

Circuit Configuration	Circuit Constants
External clock operation 	
Ceramic filter resonator 	Ceramic filter: CSA 4.00MG (Murata) R_f: 1 MΩ ±2% C_1: 30 pF ±20% C_2: 30 pF ±20% Ceramic filter: CSA 6.00MG (Murata) R_f: 1 MΩ ±2% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal resonator  	Crystal: 4.194304 (MHz) NC-18C (Nihon Denpa Kogyo) R_f: 1 MΩ ±2% C_1: 22 pF ±20% C_2: 22 pF ±20% Crystal: 6.0 (MHz) R_f: 1 MΩ ±2% C_1: 20 pF ±20% C_2: 20 pF ±20% Crystal: AT-cut parallel resonance crystal C_0: 7 pF max. R_S: 100 Ω max. f: 2.0–4.5 MHz

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic filter maker. The circuit parameters are affected by the crystal, ceramic filter resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic filter maker to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic filter.

Input/Output

The MCU provides 36 I/O pins, consisting of 12 standard pins of without pull-up MOS (NMOS open drain), and 24 high voltage pins of without pull-down MOS (PMOS open drain).

Table 2 Data Input from Common I/O Pins

I/O Circuit Type	Available Pin Condition for Input
For standard pins of without pull-up MOS (NMOS open drain)	1
For high voltage pins of without pull-down MOS (PMOS open drain)	0

Table 3 I/O Pin Circuit Types

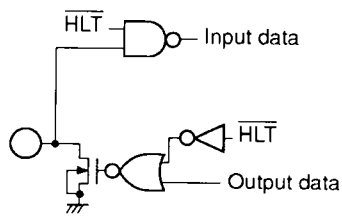
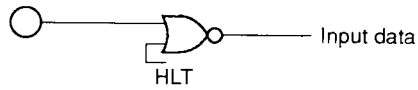
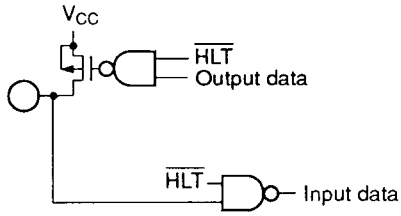
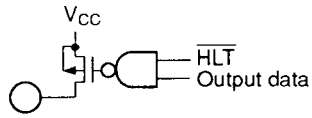
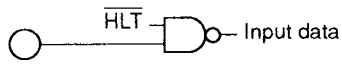
Pin Type		Without Pull-Up MOS (NMOS Open Drain)	Pins
Standard pins	I/O pins		D_0–D_3, $R3_0$–$R3_3$, $R4_0$–$R4_3$
	Input pins		$\overline{INT_0}$, $\overline{INT_1}$

Table 3 I/O Pin Circuit Types (cont)

Pin Type	Without Pull-Down MOS (PMOS Open Drain)	Pins
High voltage pins	I/O pins	D_4–D_{14}, $R1_0$–$R1_3$, $R2_0$–$R2_3$
	Output pins	$R0_0$–$R0_3$
	Input pins	RA_1







Note: In the stop mode, $\overline{HLT}$ is 0, HLT is 1, and I/O pins are in high impedance.

Differences Between In-Package PROM, On-Package EPROM, and Mask ROM Types

Item		In-Package PROM ZTAT™ HD4074019				In-Package PROM ZTAT™ HD4074008				On-Package EPROM HD614P080S HD614P0160S	Mask ROM HD404019	Mask ROM HMCS408AC/C/CL			Mask ROM HMCS404AC/C/CL			Mask ROM HMCS402AC/C/CL		
Typical instruction execution time		1 µs				1 µs				1.33 µs	1 µs	1 µs	2 µs	4 µs	1 µs	2 µs	4 µs	1 µs	2 µs	4 µs
Power supply voltage (V)		4.5–5.5				4.5–5.5				4.5–5.5	3.5–6	4.5–6	3.5–6	2.5–6	4.5–6	4–6	2.7–6	4.5–6	4–6	2.7–6
ROM		16,384 words × 10-bit				8,192 words × 10-bit				HN27C64: 4,096 × 10-bit HN4827128: 8,192 × 10-bit HN27C256: 16,384 × 10-bit	16,384 words × 10-bit	8,192 words × 10-bit			4,096 words × 10-bit			2,048 words × 10-bit		
RAM		992 × 4-bit				512 × 4-bit				576 × 4-bit	992 × 4-bit	512 × 4-bit			256 × 4-bit			160 × 4-bit		
I/O pin circuit	Standard pins	NMOS open drain				NMOS open drain				NMOS open drain	Each pin can be without pull-up MOS (NMOS open drain), with pull-up MOS, or CMOS									
	High voltage pins	PMOS open drain				PMOS open drain (Typical 5-V use)				PMOS open drain	Each pin can be without pull-down MOS (PMOS open drain) or with pull-down MOS									
Clock generation	Crystal	o				o				o	o	o			o			o		
	Ceramic	o				o				o	o	o			o			o		
	Resistance	—				—				—	—	—			HMCS404C			HMCS402C		
Package	Type	DC-64S (Window)	DP-64S	FP-64B	FP-64A	DC-64S (Window)	DP-64S	FP-64 FP-64A	DC-64SP		DP-64S	FP-64B	FP-64A	DP-64S	FP-64	DP-64S	FP-64	DP-64S	FP-64	
	Occupied area (mm^2)	18.8 × 57.3	17 × 58	18.8 × 24.8	17.2 × 17.2	18.8 × 57.3	17 × 58	19.6 × 25.6 17.2 × 17.2	23 × 57.3		17 × 58	18.8 × 24.8	17.2 × 17.2	17 × 58	19.6 × 25.6	17 × 58	19.6 × 25.6	17 × 58	19.6 × 25.6	
	Height from stand off (mm)	5.6 (Max)	5.1 (Max)	2.9 (Max)	2.9 (Max)	5.6 (Max)	5.1 (Max)	2.9 (Max) 2.9 (Max)	7.5 (Max)		5.1 (Max)	2.9 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	

Notes: DC-64S: 64-pin shrink type ceramic DIP with window
DP-64S: 64-pin shrink type DIP
FP-64: 64-pin flat plastic package
DC-64SP: 64-pin shrink type ceramic EPROM on-package
o: Available
—: Not available

Precautions When Using the EPROM On-Package Microcomputer

Pay careful attention to the following since this MCU is particularly structured with pin sockets on its package.

1. Avoid contact of high static or surge voltages in order to not exceed the maximum ratings of the socket pins as well as the LSI pins. If such a contact is made, the device may become permanently damaged.

2. When using this chip in production (i.e., for mask ROM single-chip microcomputers), pay special attention to the following to maintain a solid connection between the EPROM pins and the socket pins.

   a. The recommended temperature for soldering the chip onto a circuit board is to be kept below 250°C for no more than 10 seconds. If this condition is exceeded, the bonding solder of the solder pins may melt, thus causing the solder pins to move about.

   b. Avoid getting any detergent or coating inside the sockets during flux washing or board coating after soldering. Doing so may cause poor contact within the sockets.

   c. Avoid permanent use of this chip in a vibratory environment or system.

   d. The sockets lose contact after being used repeatedly so it is recommended to use a new chip during production.

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	−0.3 to +7.0	V	
Pin voltage	V_T	−0.3 to V_{CC} + 0.3	V	3
		V_{CC} − 45 to V_{CC} + 0.3	V	4
Total permissible input current	ΣI_o	50	mA	5
Total permissible output current	$-\Sigma I_o$	150	mA	6
Maximum input current	I_o	15	mA	7, 8
Maximum output current	$-I_o$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes: 1. Permanent damage may occur if these absolute maximum ratings of the LSI or for the EPROM are exceeded. Normal operation should be under the conditions of the electrical characteristics. If these conditions are exceeded, it may cause a malfunction and affect the reliability of the LSI.
2. All voltages are with respect to GND.
3. Applied to standard pins.
4. Applied to high-voltage I/O pins.
5. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
6. Total permissible output current is the total sum of output currents which flow out from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
8. Applied to D_0–D_3 and R3–R4.
9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
10. Applied to D_0–D_3 and R3–R4.
11. Applied to R0–R2.
12. Applied to D_4–D_{14}.

Electrical Characteristics

DC Characteristics (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	$0.22V_{CC}$	V		
		OSC_1	–0.3	—	0.5	V		
Input/output leakage current	$\|I_{IL}\|$	RESET, $\overline{INT_0}$, $\overline{INT_1}$, OSC_1	—	—	1	µA	V_{IN} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V Crystal or ceramic filter oscillator f_{OSC} = 4 MHz	2, 5
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.2	mA	Maximum logic operation V_{CC} = 5 V Crystal or ceramic filter oscillator f_{OSC} = 4 MHz	3, 5
	I_{SBY2}	V_{CC}	—	—	0.9	mA	Minimum logic operation V_{CC} = 5 V Crystal or ceramic filter oscillator f_{OSC} = 4 MHz	4, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC} $V_{in\ (RESET)}$ = 0 V to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Output buffer current is excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0–D_3, R3–R4: V_{CC}
   - D_4–D_{15}, R0–R2, RA_1: V_{CC} to V_{CC} – 40 V

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer B: Divide-by-2 prescaler divide ratio

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0–D_3, R3–R4: V_{CC}
   - D_4–D_{15}, R0–R2, RA_1: V_{CC} to V_{CC} – 40 V

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer B: Divide-by-2048 prescaler divide ratio

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0–D_3, R3–R4: V_{CC}
   - D_4–D_{15}, R0–R2, RA_1: V_{CC} to V_{CC} – 40 V

5. When $f_{OSC} = \chi$ [MHz], the current dissipation in operation mode and standby mode is estimated as follows:

$$\text{Max. value } (f_{OSC} = \chi \text{ [MHz]}) = \frac{\chi}{4} \times \text{max. value } (f_{OSC} = 4 \text{ MHz})$$

Input/Output Characteristics for Standard Pins (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	D_0–D_3, R3–R4	0.7V_{CC}	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	D_0–D_3, R3–R4	–0.3	—	0.22V_{CC}	V	
Output low voltage	V_{OL}	D_0–D_3, R3–R4	—	—	0.4	V	I_{OL} = 1.6 mA
Input/output leakage current*	$\|I_{IL}\|$	D_0–D_3, R3–R4	—	—	1	µA	V_{in} = 0 V to V_{CC}

* Output buffer current is excluded.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	D_4–D_{14}, R1, R2, RA_1	0.7V_{CC}	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	D_4–D_{14}, R1, R2, RA_1	V_{CC} – 40	—	0.22V_{CC}	V	
Output high voltage	V_{OH}	D_4–D_{14}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA
			V_{CC} – 2.0				$-I_{OH}$ = 9 mA
		R0–R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA
			V_{CC} – 2.0				$-I_{OH}$ = 1.8 mA
Output low voltage	V_{OL}	D_4–D_{14}, R0–R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V
Input/output leakage current*	$\|I_{IL}\|$	D_4–D_{14}, R0–R2, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}

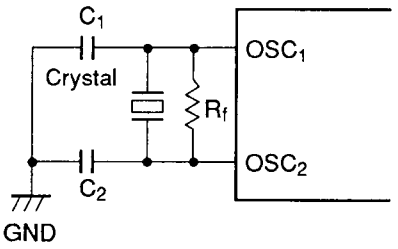
* Output buffer current is excluded.

AC Characteristics (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, unless otherwise specified)

Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Crystal or ceramic filter oscillator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	6.2	MHz		
	Instruction cycle time	t_{cyc}		1.29	2	20	µs		
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
External clock	External clock frequency	f_{CP}	OSC_1	0.4	—	6.2	MHz		2
	External clock high width	t_{CPH}	OSC_1	70	—	—	ns		2
	External clock low width	t_{CPL}	OSC_1	70	—	—	ns		2
	External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
	External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
	Instruction cycle time	t_{cyc}		1.29	—	20	µs		2
$\overline{INT_0}$ high width		t_{I0H}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width		t_{I0L}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width		t_{I1H}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width		t_{I1L}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width		t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance		C_{in}	All pins	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
Reset fall time		t_{RSTf}		—	—	20	ms		4

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage V_{CC} = 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or when recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, consult with the crystal or ceramic filter manufacturer when designing the reset circuit.

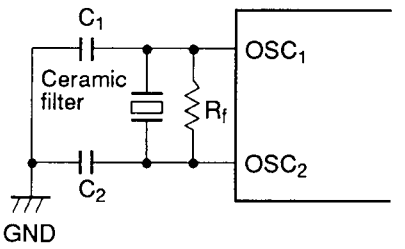
Crystal oscillator



Crystal: 4.194304 MHz NC-18C
(Nihon Denpa Kogyo)

R_f: 1 MΩ ±2%
C_1: 22 pF ±20%
C_2: 22 pF ±20%

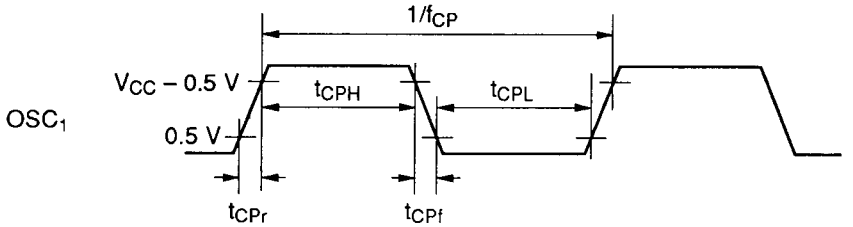
Ceramic filter oscillator



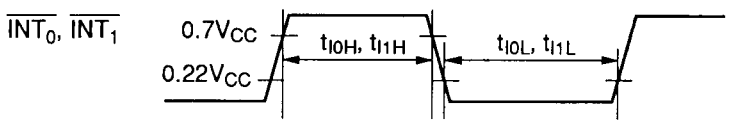
Ceramic filter: CSA4.00MG (Murata)

R_f: 1 MΩ ±2%
C_1: 30 pF ±20%
C_2: 30 pF ±20%

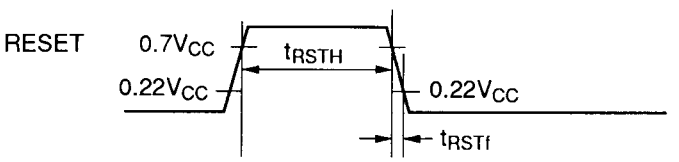
2.



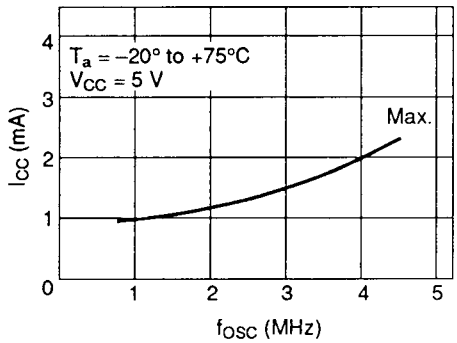
3.



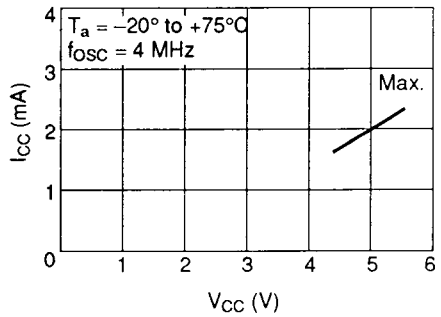
4.



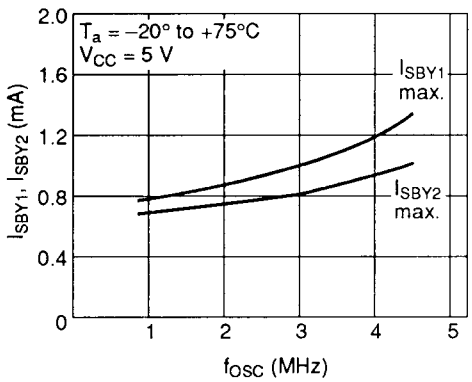
Characteristics Curves (Reference Data)



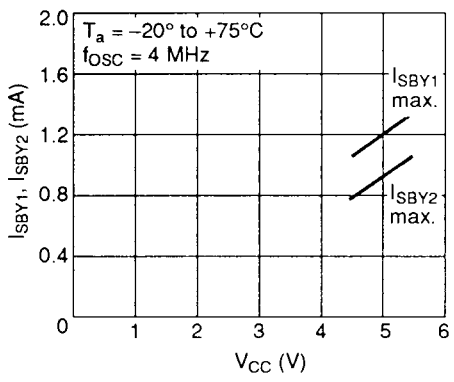
I_{CC} vs. f_{OSC} Characteristic
(Crystal, ceramic resonator)



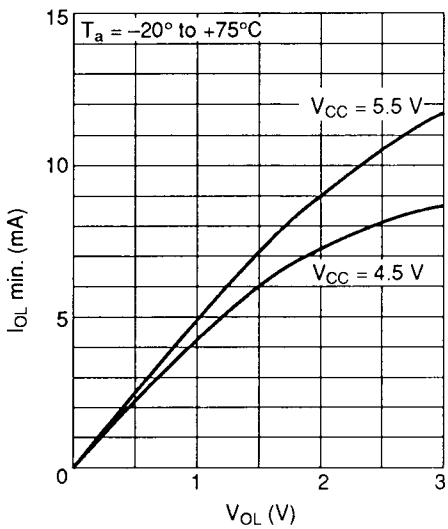
I_{CC} vs. V_{CC} Characteristic
(Crystal, ceramic resonator)



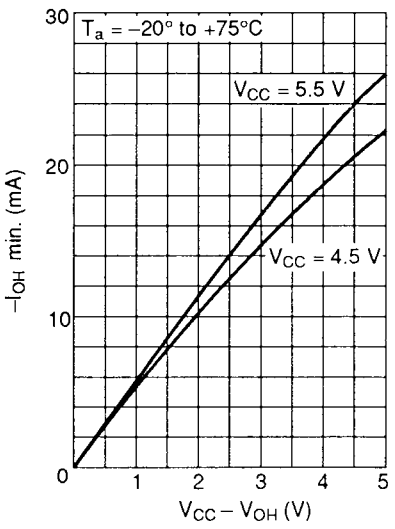
I_{SBY} vs. f_{OSC} Characteristic
(Crystal, ceramic resonator)



I_{SBY} vs. V_{CC} Characteristic
(Crystal, ceramic resonator)

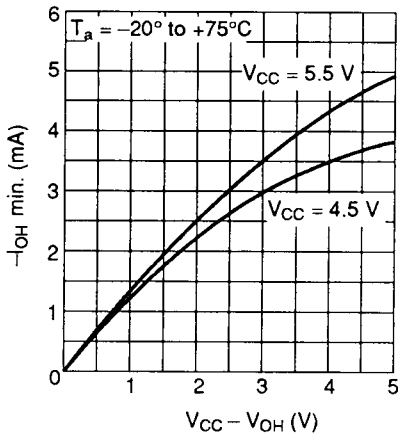


I_{OL} Min. vs. V_{OL} Characteristic
(Standard pin)



$-I_{OH}$ Min. vs. ($V_{CC} - V_{OH}$) Characteristic
(D_4–D_{15} pins)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ Min. vs. ($V_{CC} - V_{OH}$) Characteristic (R0–R2 pins)