HD63085

Document Image Compression and Expansion Processor (DICEP)

The DICEP is an LSI that performs compression (encoding) and expansion (decoding) of the digital (two-value) data representing a document image.
The DICEP is used in G3 and G4 facsimile apparatus, intelligent copiers, word processors, telex, terminals, laser beam printers, file servers and other office automation systems.
The DICEP uses Modified Huffman (MH) coding scheme, Modified READ (MR) coding scheme and Modified MR (M^2R) coding scheme which are compatible with the CCITT (Comité Consultatif International Télégraphique et Téléphonique) recommendations for Group 3 and Group 4 facsimile apparatus.

Features

- Compatible with the CCITT Recommendations for Group 3 and Group 4 facsimile apparatus
- Simple MPU Command
  As the DICEP stores coding and decoding algorithms in the microprogram ROM as firmware, a simple MPU command allows this LSI to encode (i.e. compress) or decode (i.e. expand) a scan line of digital data.
- High Speed Coding and Decoding
  The DICEP realizes high speed coding and decoding by:
  - including a changing pels* detector which can detect a changing pel contained in a word (8 bits/16 bits) of document image data within an instruction cycle time (at least 125nsec), and
  - including a decoded pels generator which can generate a word (8 bits/16 bits) of document image data within an instruction cycle time.

  *: The term 'picture element' is abbreviated to 'pel' in this document.
- Flexible System Configuration
  - Either 68 type MPU or 80 type MPU can be interfaced.
    The system bus has the size of 8 bits.
  - The DICEP has two bus interfaces; the system bus interface and the document image bus interface.
  - The DICEP may be interfaced with two independent buses (i.e. the system bus and the document image bus), while it may be interfaced with a common bus.
  - The size of the document image bus is selectable (8 bits/16 bits) depending on the word size of document image memory.
- High Speed DMA Transfer
  - The DICEP can perform direct memory access (DMA) transfer between an I/O device (scanner or printer) and the document image memory. The maximum transfer rate is 4M byte/sec.
  - With a DMA controller (DMAC) on the system bus, DMA transfers can be performed between a memory on the system bus and the DICEP.
- A Variety of Programmable Parameters
  Internal programmable registers present the DICEP flexibility to allow application to many kinds of systems.
  - The parameters can be changed before initiation of every command.
  - The length of a scan line is programmable from the word size of the document image memory (8 bits/16 bits) to 64K bits.
  - One of coding operation, decoding operation and transfer operation can be selected.
  - One of MH coding scheme, MR coding scheme, M^2R coding scheme and run length coding scheme can be selected.
  - The minimum length of a coded scan line is programmable from 0 to $2^{16}-1$ bits.
  - The number of End of Line (EOL) code words is programmable from 0 to $2^{16}-1$.
  - The number of Return to Control (RTC) code words is programmable from 0 to $2^{16}-1$.
  - The DICEP can code and decode a desired part of a document on a word (8 bits/16 bits) basis.
- Data Transfer between Buses
  The DICEP can perform data transfer between the system bus and the document image bus without coding or decoding.
- Octet Mode
  The DICEP provides Octet Mode. In this mode, a coded scan line or a coded page is 8-bit boundary conditioned.
- Run Length Coding Scheme
  The DICEP provides run length coding scheme in addition to MH coding, MR

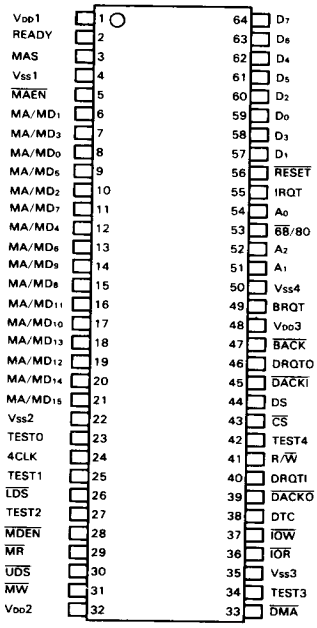
coding and M²R coding.
- High Operating Speed
  - −Instruction cycle time is 125 nsec min. (at system clock of 8 MHz max.)
  - −Input clock frequency is 32 MHz max.
- Package
  - −64 pin plastic shrink DIP (DP-64S)
  - −72 pin ceramic PGA (PC-72)

Ordering Information

Type No.	Input Clock	Package
HD63085P	2MHz to 32MHz	64 pin plastic shrink DIP (DP-64S)
HD63085YR		72 pin ceramic PGA (PC-72)

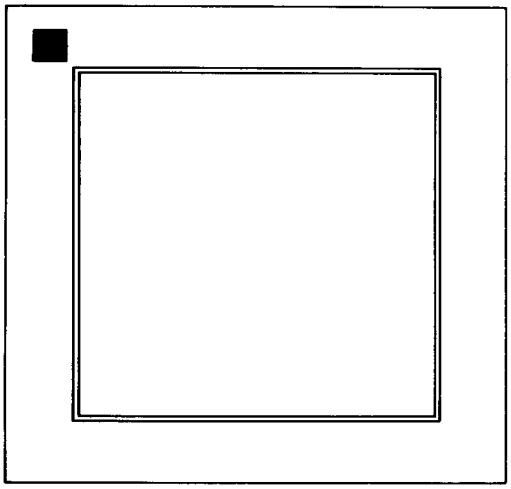
Pin Arrangement

●DP-64S

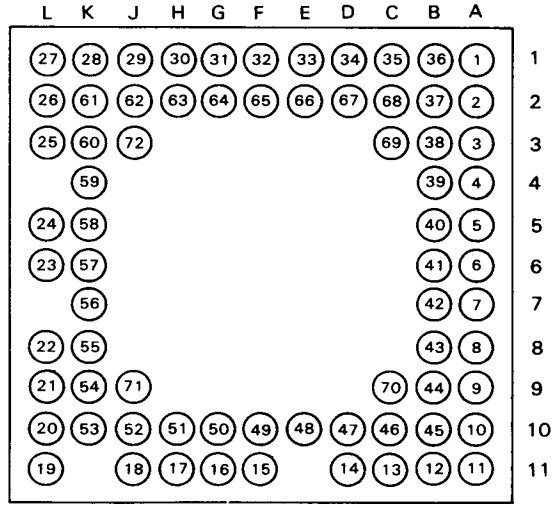


(Top View)

●PC-72



(Top View)

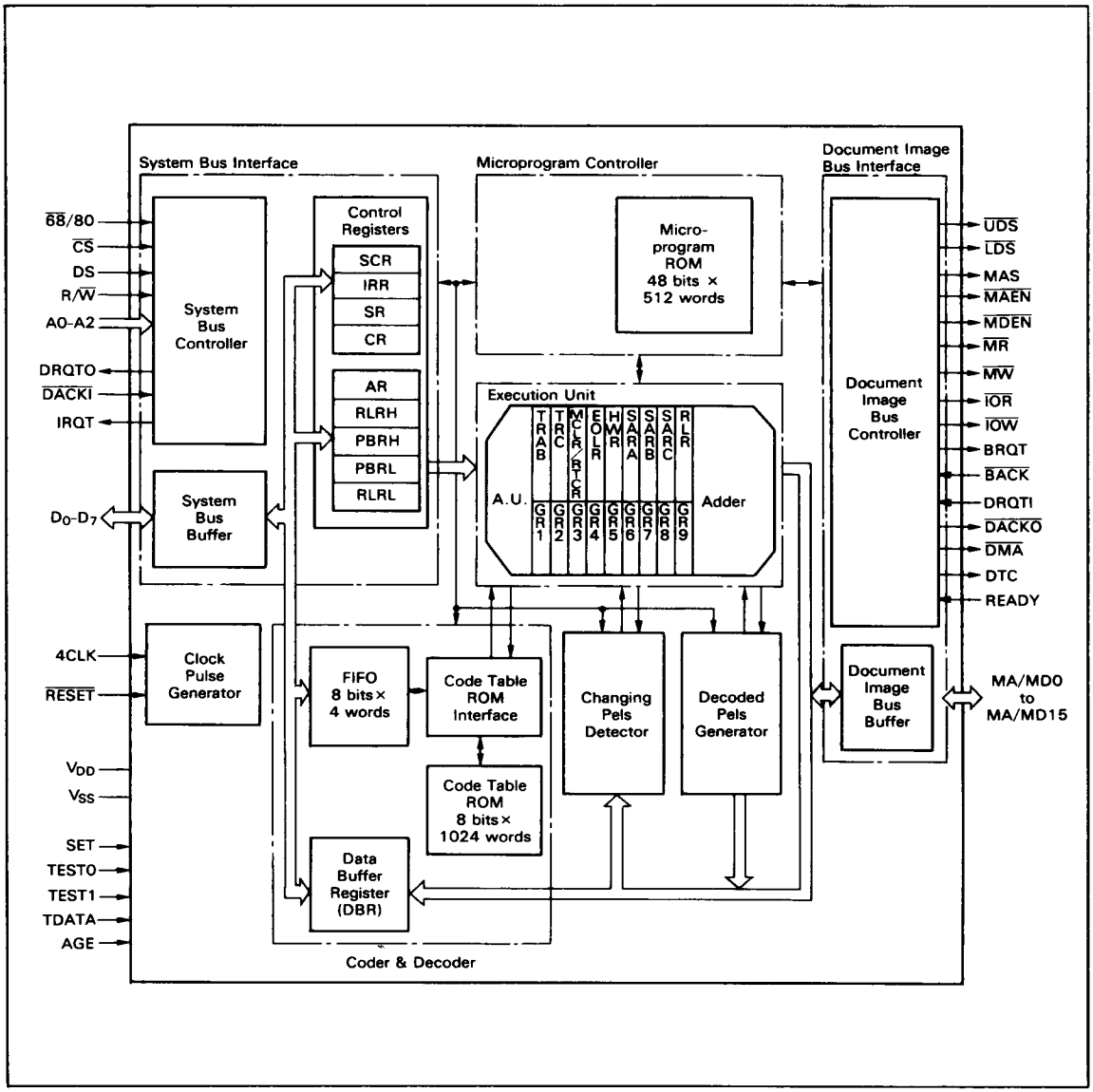


(Bottom View)

No lines should be connected to pin 26, 54, 67, 69, 70, 71 and 72.

Pin Code	Pin No.	Mnemonic	Pin Code	Pin No.	Mnemonic	Pin Code	Pin No.	Mnemonic
A1	1	MA/MD_0	C3	69	NC	J2	62	D_1
A2	2	MA/MD_2	C9	70	NC	J3	72	NC
A3	3	MA/MD_4	C10	46	$\overline{LDS}$	J9	71	NC
A4	4	MA/MD_6	C11	13	$\overline{UDS}$	J10	52	$\overline{DACKO}$
A5	5	MA/MD_8	D1	34	READY	J11	18	DTC
A6	6	MA/MD_{10}	D2	67	NC	K1	28	V_{DD}
A7	7	MA/MD_{12}	D10	47	$\overline{MDEN}$	K2	61	V_{DD}
A8	8	MA/MD_{14}	D11	14	$\overline{MW}$	K3	60	IRQT
A9	9	V_{SS}	E1	33	V_{DD}	K4	59	A_0
A10	10	$TEST_0$	E2	66	V_{DD}	K5	58	A_2
A11	11	4CLK	E10	48	$\overline{MR}$	K6	57	BRQT
B1	36	MA/MD_1	F1	32	D_6	K7	56	DRQTO
B2	37	MA/MD_3	F2	65	D_7	K8	55	$\overline{CS}$
B3	38	MA/MD_5	F10	49	$\overline{DMA}$	K9	54	NC
B4	39	MA/MD_7	F11	15	SET	K10	53	DRQTI
B5	40	MA/MD_9	G1	31	D_4	L1	27	$\overline{RESET}$
B6	41	MA/MD_{11}	G2	64	D_5	L2	26	NC
B7	42	MA/MD_{13}	G10	50	V_{SS}	L3	25	68/80
B8	43	MA/MD_{15}	G11	16	V_{SS}	L5	24	A_1
B9	44	V_{SS}	H1	30	D_2	L6	23	$\overline{BACK}$
B10	45	$TEST_1$	H2	63	D_3	L8	22	$\overline{DACKI}$
B11	12	TDATA	H10	51	$\overline{IOW}$	L9	21	DS
C1	35	MAS	H11	17	$\overline{IOR}$	L10	20	AGE
C2	68	$\overline{MAEN}$	J1	29	D_0	L11	19	$R/\overline{W}$

Block Diagram



Block Configurations

System Bus Interface

The system bus interface has a timing specification compatible with 8-bit MPUs (HD6800/HD64180). This block includes control registers which can be directly accessed by the MPU.

Microprogram Controller

The microprogram controller stores coding and decoding programs in the microprogram ROM to control all other blocks of the DICEP. This block consists of the microprogram ROM with 512 words of 48 bits, the sequence controller and the pipeline register.

Execution Unit

The execution unit generates document image memory addresses, and calculates the position of changing pels, run lengths, and the relative distance between changing pels on the coding line and those on the reference line.
This block consists of eighteen 16-bit registers, the arithmetic unit (A.U.) and the adder. Nine registers (TRAB, TRC, MCLR/RTCR, EOLR, HWR, SARA, SARB, SARC, and RLR) can be programmed by the MPU via the control registers in the system bus interface. These nine registers are called "parameter registers".

Coder and Decoder

The coder generates the addresses of the code table ROM from input run lengths or relative distances, and generates appropriate code words by looking up the code table ROM.
On the other hand, the decoder generates the addresses of the code table ROM from input code words, and generates run lengths or relative addresses by looking up the code table ROM.

This block consists of the code table ROM with 1024 words of 8 bits, the code table ROM interface, the First-In First-Out memory (FIFO) with 4 words of 8 bits, and the Data Buffer Register (DBR). The code table ROM stores the data which is referenced for coding and decoding operations. The code table ROM interface generates the addresses of the code table ROM. The FIFO temporarily stores code words during coding or decoding operation. The DBR is a intermediate buffer which is used to transfer data between the system bus and the document image bus.

Changing Pels Detector

The changing pels detector detects a changing pel whose color (white or black) is different from that of the previous pel on the same scan line. It can detect a changing pel in a word (8 bits/16 bits) of the document image memory within an instruction cycle time.
This block consists of two changing pels detectors: the reference line detector and the coding line detector. For detailed infomation of the reference line and the coding line.

Decoded Pels Generator

The decoded pels generator can generate at most a word (8 bits/16 bits) of decoded pels within an instruction cycle time, using the information of the positions of changing pels.

Document Image Bus Interface

The document image bus interface provides an interface between the DICEP and the document image bus. It has a 16-bit multiplexed address/data bus.
This block has the following functions:

- it has bus arbitration technique.
- it outputs control signals for the document image bus.

DICEP Functional Summary

Item	Function
Coding Scheme	MH, MR, M^2R, Run Length
Maximum Scan-line Length	64 bytes/line
Document Image Bus Memory Address Space size	Image Memory ……64k bytes I/O Devices ……64k bytes
Maximum DMA Transfer Rate	4M bytes/sec *
Maximum Changing Pels Detect Speed	3.2M bytes/sec *
Maximum Decoded Pels Generation Speed	3.2M bytes/sec *

* : Input clock frequency is 32 MHz.

Coding and Decoding Scheme

MH Coding scheme

In the MH coding scheme, one dimensional coding is performed on all lines of data, One dimensional coding encodes run lengths of white pels and black pels which alternate on a scan line.
A one dimensionally coded scan line is made of a data line, End of Line code words and, if necessary, Fill bits.

MR Coding Scheme

In MR coding scheme, the one dimensional coding is performed on a scan line, then the two dimensional coding is performed on at most K-1 successive lines. The maximum value of K shall be 2 if standard vertical resolution is used and shall be 4 if higher vertical resolution is used.

M²R Coding Scheme

M²R coding scheme is used for the Group 4 facsimile apparatus. In this scheme, all lines of data are coded two dimensionally. At the coding of the first line of a page, a white reference line is imaginarily set immediately above the coding line. This scheme requires neither fill bits nor line synchronization code words.

Run Length Coding Scheme

In addition to the above mentioned coding schemes, the DICEP provides run length coding scheme. In run length coding scheme, the run length of all white or black is generated without data compression (below shown figure 1).

The DICEP is designed to realize a wide variety of user applications. These applications are organized into two groups, that is the independent bus system and the common bus system.
This section offers examples of the two types of applications.

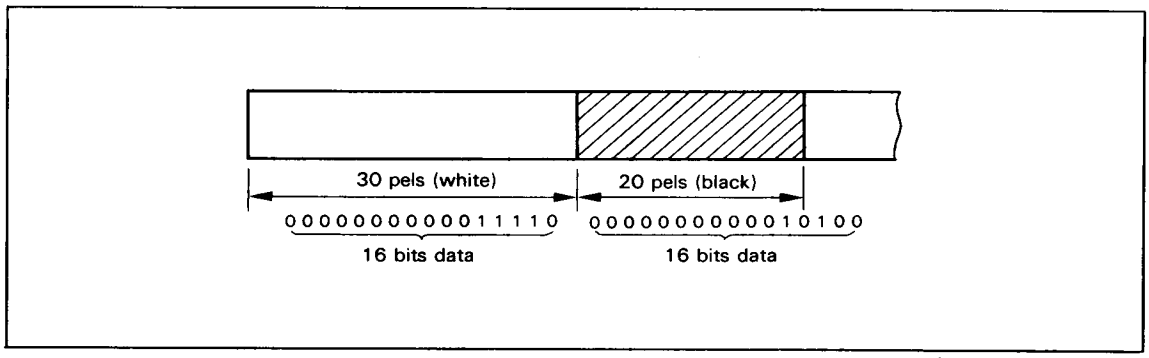


Figure 1 Coding Data (Run length coding scheme)

System Configurations

Independent Bus System

Figure 2 shows a system configuration diagram as an example of the independent bus system.
The features of this system are as follows:

- This system includes two independent buses (the system bus and the document image bus)
- The DICEP can perform document image bus operation independently of the MPU, which enhances the system throughput.
- This type of system can also be used in G4 facsimile apparatus.

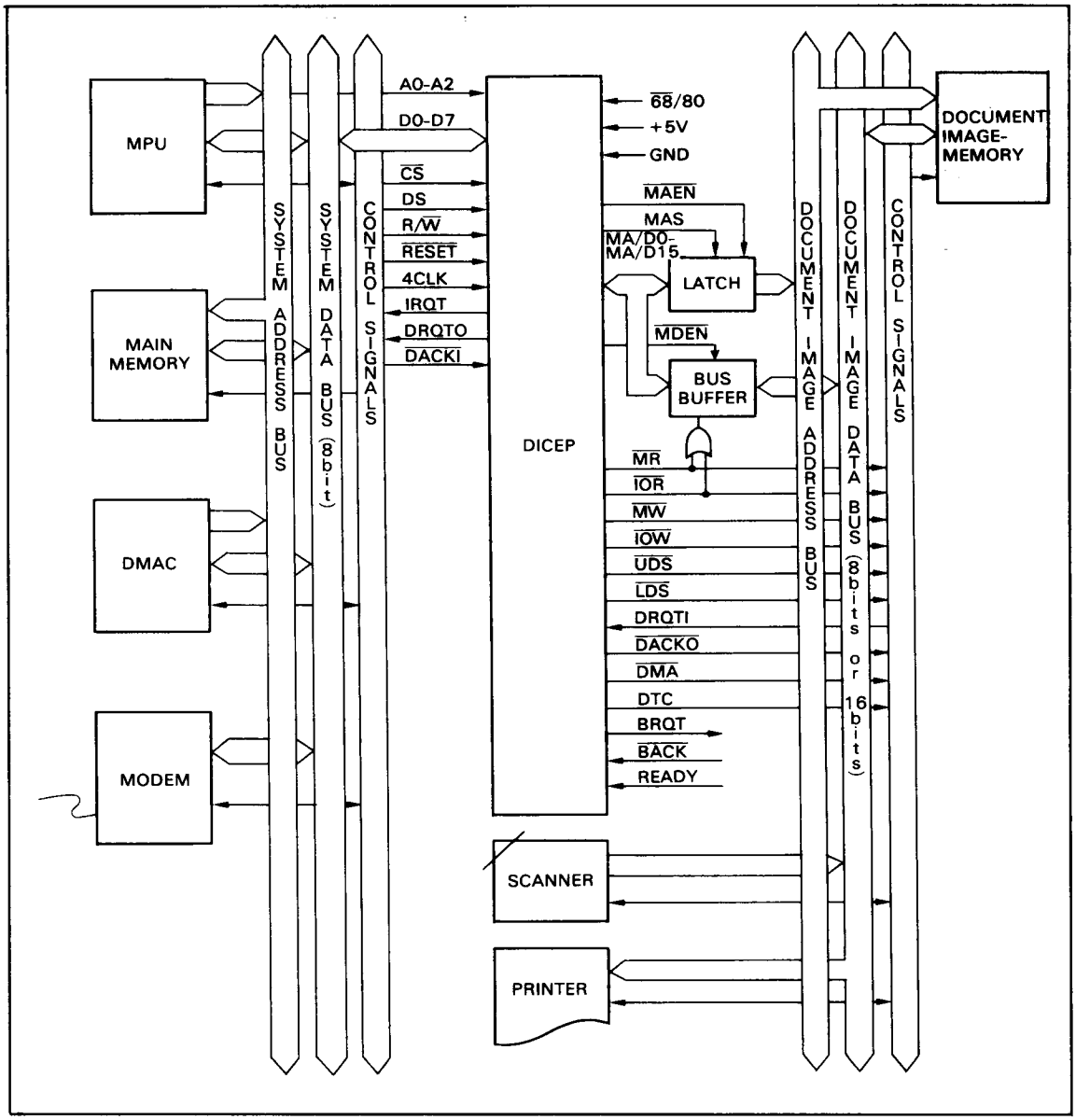


Figure 2 System Configuration Diagram (an Example of Independent Bus System)

Absolute Maximum Rating

Item	Symbol	Value	Unit
Supply Voltage	V_{DD} *	-0.3 to +0.7	V
Input Voltage	V_{in} *	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150 (PC-72)	°C
		-55 to +125 (DP-64S)	

* Voltages referenced to V_{SS}=0V.

Recommended Operating Conditions

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{DD} *	4.75	5	5.25	V
Input Voltage	V_{IL} *	-0.3	–	0.8	V
	V_{IH}	2.2	–	V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0	25	70	°C

* Voltages referenced to V_{SS}=0V.