

# HD63485

## Graphic Memory Interface Controller (GMIC)

### Description

The HD63485 LSI belongs to the ACRTC (advanced CRT controller) family. It provides memory access control to frame buffers for graphic display and drawing. Incorporating bus driver circuits and a DRAM (dynamic RAM) interface, the GMIC allows direct connection to DRAM with no external circuits. Its main function include address data latch, DRAM row and column address multiplexing, supplying RAS, CAS, OE, WE, and other signals, and generating the 2CLK signal for the ACRTC. Using the Hi-BiCMOS process, the HD63485 achieves high speed memory access with low power dissipation.

### Features

- Drives frame buffer memory directly ( $I_{OL} = 24$  mA max)
- Generates DRAM signal: row and column addresses, RAS, CAS, OE, WE, etc
- High-speed dot rate input (64 MHz max)
- Direct ACRTC interface
- Generates horizontal scrolling control signals
- Generates load signals for horizontal smooth scrolling
- Programmable address increment mode
- Generates 2CLK signal
- TTL-compatible input output
- Single +5 V power supply
- Low power dissipation

### Type of Products

Part No.	Speed	Package
HD63485PS32	32MHz	64-pin Plastic Shrink DIP
HD63485PS48	48MHz	(DP-64S)
HD63485PS64	64MHz	
HD63485CP32	32MHz	68-pin PLCC
HD63485CP48	48MHz	(CP-68)
HD63485CP64	64MHz	

### Pin Description

Figure 1 shows the pin arrangement for the 64-pin shrink-type DIP and the 68-pin PLCC packages. Pins marked with \* are bus drivers, which can handle a maximum output current  $I_{OL}$  of 24mA. Table 1 describes the pins.

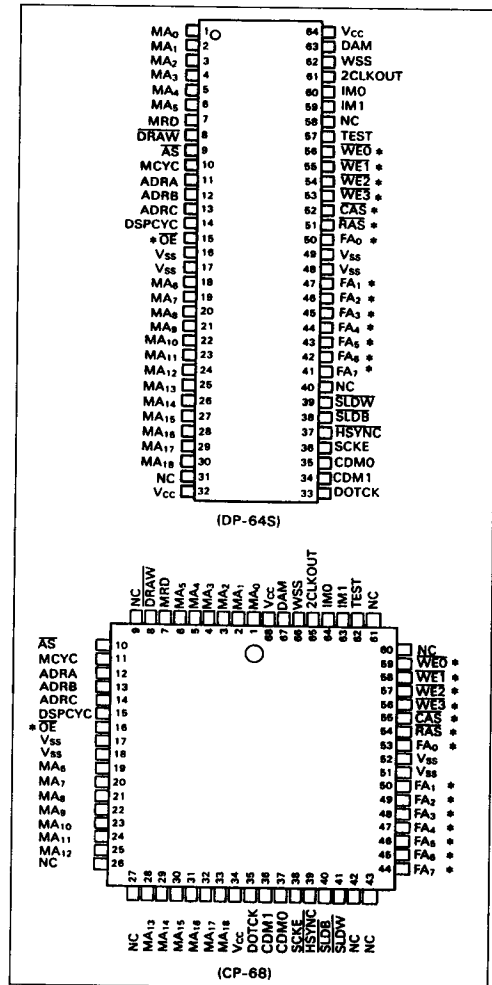


Figure 1. Pin Arrangement

**Power Supply (V<sub>SS</sub>, V<sub>CC</sub>)**

V<sub>SS</sub> and V<sub>CC</sub> are the GMIC power supply pins. V<sub>CC</sub> pins are +5 V  $\pm$  5 % supply pins. V<sub>SS</sub> are the ground

pins. Be sure to connect all four V<sub>SS</sub> pins to ground and both V<sub>CC</sub> pins to the power supply.

**Table 1. Pin Description**

Signal	Pin Number			Description
	DIP-64	PLCC-68	I/O	
V <sub>CC</sub>	32,64	34,68		+5 V power supply
V <sub>SS</sub>	16,17, 48,49	17,18, 51,52		Ground
CDM1,	34	36	I	Clock division ratio
CDM0	35	37		
DAM	63	67	I	Dual access mode
IM1,	59	63	I	Increment mode
IM0	60	64		
WSS	62	66	I	Window smooth scroll
DOTCK	33	35	I	Dot clock
TEST	57	62	I	Test
2CLKOUT	61	65	O	Clock
MCYC	10	11	I	Memory cycle
DRAW	8	8	I	Draw
MRD	7	7	I	Memory read
AS	9	10	I	Address strobe
MA18-	30-18,	33-28,	I	Memory address bus
MA0	6-1	25-19, 6-1		
HSYNC	37	39	I	Horizontal sync
RAS	51	54	O	Row address strobe
CAS	52	55	O	Column address strobe
WE3-WE0	53-56	56-59	O	Write enable
OE	15	16	O	Output enable
FA7-FA0	41-47, 50	44-50, 53	O	Frame buffer address
ADRA-ADRC	11-13	12-14	O	Address
DSPCYC	14	15	O	Display cycle
SCKE	36	38	O	Shift clock enable
SLDB, SLDW	38, 39	40, 41	O	Shift load signals



## Program Pins

**Clock Division Ratio (CDM1, CDM0):** The CDM1 and CDM0 inputs determine the division ratio used to generate 2CLKOUT for the ACRTC from the DOTCK input. See table 2.

**Dual Access Mode (DAM):** The DAM input sets the access mode as shown in table 3.

**Increment Mode (IM1, IM0):** The IM1 and IM0 inputs determine the addresses sent from memory addresses (MA18-MA0) as the frame buffer output (FA7-FA0) to accommodate different DRAM types. Table 4 shows the memory address outputs corresponding to the IM1 and IM0 settings. Note that the frame buffer addresses (FA7-FA0) have multiplexed memory address outputs.

IM inputs are closely related to the graphic address increment (GAI) of the ACRTC (see ACRTC user's manual).

**Window Smooth Scroll (WSS):** When the WSS input is low (0), each base screen can be scrolled in single access mode, dual access mode 0, and dual access mode 1. The SLDB signal contains the

scrolling data.

When the WSS input is high (1), the window screen can be smooth scrolled in dual access mode 1. The SLDW signal contains the scrolling data.

## Operation Control Signals

**Dot Clock (DOTCK):** The DOTCK input must be the same clock that is supplied to the shift register for video signal generation. Dot clock frequency is determined by the horizontal display resolution (pixel count) and the display period of one horizontal scan.

**Test (TEST):** The TEST input is used for manufacturing operational testing. It must be fixed low when the GMIC is mounted in a system.

## ACRTC Interface Signals

**Clock (2CLK):** The 2CLKOUT clock output is a basic clock for the ACRTC's internal operation. The GMIC generates 2CLKOUT by dividing the high-speed dot clock by the ratio determined by the CDM1 and CDM0 inputs.

Table 2. Clock Division Ratio

CDM1	CDM0	Division Ratio
0	0	Not allowed
0	1	Divide by 4
1	0	Divide by 8
1	1	Divide by 16

Table 3. Access Modes

DAM	Access Mode
0	Single access mode
1	Dual access mode

Table 4. Increment Mode

IM1	IM0	Increment Mode	Address Output to FA7-FA0	Address Output to ADRC-ADRA
0	0	+1	MA15-MA8, MA7-MA0	MA18, MA17, MA16
0	1	+2	MA16-MA9, MA8-MA1	MA0, MA17, MA18
1	0	+4	MA17-MA10, MA9-MA2	MA0, MA1, MA18
1	1	+8	MA18-MA11, MA10-MA3	MA0, MA1, MA2



**Memory Cycle (MCYC):** The MCYC input indicates the ACRTC's frame buffer access timing. MCYC is low when the ACRTC is in the address cycle, and high when the ACRTC is in the data cycle.

**Draw ( $\overline{\text{DRAW}}$ ):** The  $\overline{\text{DRAW}}$  input indicates whether the ACRTC memory cycle is a drawing cycle.  $\overline{\text{DRAW}}$  is low during drawing cycle, and high otherwise. The GMIC uses  $\overline{\text{DRAW}}$  to recognize display cycles, and also to generate DRAM control signals ( $\overline{\text{WE3-WE0}}$ ).

**Memory Read (MRD):** The MRD input controls data transfer between frame buffers and the ACRTC. The ACRTC pulls MRD high when it reads data from the frame buffer, and low when it writes data.

The only exception is when the ACRTC is in superimpose display mode (dual access mode 1). In superimpose display mode, the ACRTC inputs a low level and reads data from a frame buffer in order to indicate that the display cycle is for a superimposed screen (window screen).

**Address Strobe ( $\overline{\text{AS}}$ ):** The  $\overline{\text{AS}}$  input is a latch timing signal for the memory address sent from the ACRTC. Additionally,  $\overline{\text{AS}}$  indicates whether memory is begin accessed. For example, for horizontal zooming, the  $\overline{\text{SLDB}}$  signal is provided at a lower frequency, corresponding to the lower frequency of  $\overline{\text{AS}}$ .

**Memory Address Bus ( $\text{MA}_{18}\text{-MA}_0$ ):** The  $\text{MA}_{18}\text{-MA}_0$  inputs are address signals for frame buffer access, provided by the ACRTC.

**Horizontal Sync ( $\overline{\text{HSYNC}}$ ):** The  $\overline{\text{HSYNC}}$  input is a DRAM refresh cycle control signal to horizontally synchronize CRT displays. The GMIC performs  $\overline{\text{RAS}}$  only refresh when  $\overline{\text{HSYNC}}$  is low and  $\overline{\text{DRAW}}$  is high when  $\overline{\text{AS}}$  pulses are input.

Setting  $\overline{\text{HSYNC}}$  low informs the GMIC of the end of a raster display. Usually, the ACRTC's  $\overline{\text{HSYNC}}$  output supplies this input.

### Frame Buffer Access Signals

**Row Address Strobe ( $\overline{\text{RAS}}$ ):** The GMIC outputs the DRAMs'  $\overline{\text{RAS}}$  timing signal on the  $\overline{\text{RAS}}$  output.

**Column Address Strobe ( $\overline{\text{CAS}}$ ):** The GMIC outputs the DRAMs'  $\overline{\text{CAS}}$  timing signal on the  $\overline{\text{CAS}}$  output.

**Write Enable ( $\overline{\text{WE3-WE0}}$ ):** The GMIC outputs the DRAMs'  $\overline{\text{WE}}$  timing signals on the  $\overline{\text{WE}}$  outputs. Since  $\overline{\text{WE3-WE0}}$  are controlled by the increment mode ( $\text{IM } 1, \text{IM } 0$ ) and by the lower two bits of the

address ( $\text{MA } 1, \text{MA } 0$ ), the GMIC can directly control up to four memory banks. Up to eight memory banks can be controlled by externally decoding the address ( $\overline{\text{ADRC}}$ ) and  $\overline{\text{WE3-WE0}}$ .

$\overline{\text{WE3-WE0}}$  are bus driver that can handle a maximum output current  $I_{OL}$  of 24 mA.

**Output Enable ( $\overline{\text{OE}}$ ):** The GMIC outputs the DRAMs' output timing signal on the  $\overline{\text{OE}}$  output.  $\overline{\text{OE}}$  is a bus driver that can handle a maximum output current  $I_{OL}$  of 24 mA.

**Frame Buffer Address ( $\text{FA } 7\text{-FA } 0$ ):** The GMIC outputs the multiplexed DRAM address on  $\text{FA } 7\text{-FA } 0$ . How the address is multiplexed depends on the increment mode (table 4).  $\text{FA } 7\text{-FA } 0$  are bus drivers that can handle a maximum output current  $I_{OL}$  of 24 mA.

**Address ( $\overline{\text{ADRA-ADRC}}$ ):** The GMIC latches three address bits other than those delivered on the  $\text{FA } 7\text{-FA } 0$  bits and outputs them on  $\overline{\text{ADRA-ADRC}}$  in one memory cycle.


### GVAC Control Signals

**Shift Clock Enable (SCKE):** The SCKE output controls the GVACs' video signal generation shift register. It outputs a control signal for zooming according to the horizontal zoom signal (attribute control signal) from the ACRTC. The GVAC performs horizontal zoom by halting the clock when SCKE is low.

**Shift Load Signals ( $\overline{\text{SLDB}}, \overline{\text{SLDW}}$ ):** The  $\overline{\text{SLDB}}$  and  $\overline{\text{SLDW}}$  outputs are load signals for the display data of the video signal generation shift register. The  $\overline{\text{SLDB}}$  output is used for single access mode, dual access mode 0, and dual access mode 1. The  $\overline{\text{SLDW}}$  output controls the window screen in dual access mode 1.

**Display Cycle (DSPCYC):** The DSPCYC output indicates whether a memory cycle is a display cycle.

DSPCYC is high during display cycle, and low otherwise.

$\overline{\text{AS}}$	$\overline{\text{DRAW}}$	MRD	cycle mode	memory cycle	DSPCYC
L	L	L	Drawing Write	Memory Write	L
	L	H	Drawing Read	Memory Read	L
H	L	L	Window Screen Display	Memory Read	H
Low pulse	H	H	Backscreen Display	Memory Read	H
H	x	x	—	No Access	L

## Functional Description

Figure 2 is a block diagram of the HD63485.

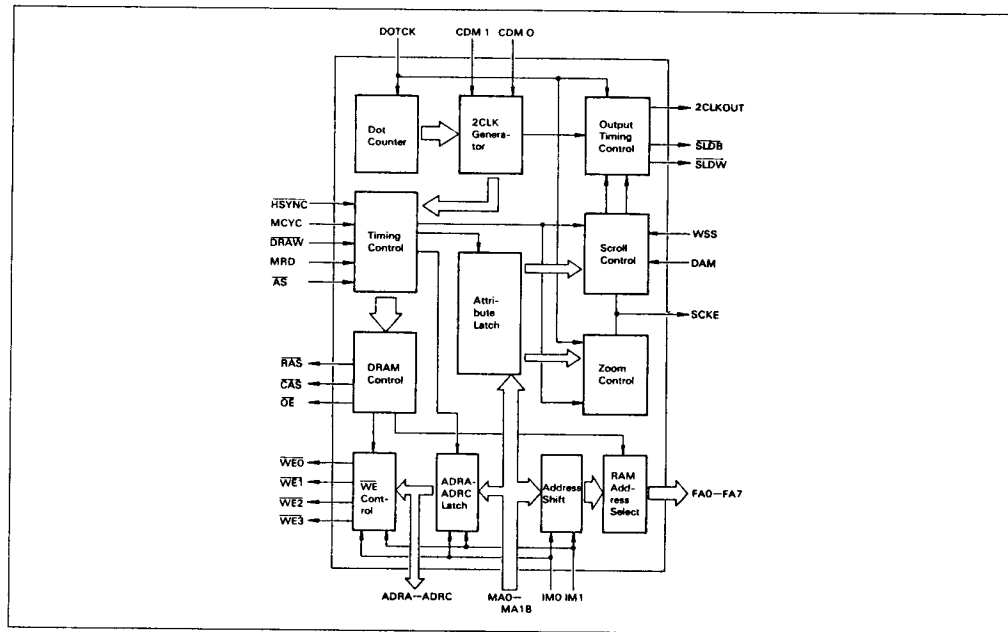


Figure 2. GMIC Block Diagram

### 2CLK Generator

The 2CLK generator generates 2CLKOUT for the ACRTC and itself by dividing the external DOTCK signal. The ratio of DOTCK to 2CLKOUT is set externally by the CDM 1 and CDM 0 inputs.

### Attribute Latch

The attribute latch temporarily stores the attribute codes input from the ACRTC on MA 18-MA 0 used for horizontal zoom (HZ 3-HZ 0) and horizontal scroll dot (HSD 3-HSD 0).

### Zoom Control

Zoom control generates the SCKE signal from DOTCK to control the GVAC clock for horizontal display zooming.

### Scroll Control

Scroll control generates shift load signals (SLDB, SLDW) which control video signal generation for the GVAC.

### Address Shifter

The address shifter stores memory addresses (MA 18-MA 0) sent from the ACRTC. It supplies them to the RAM address section according to the timesharing mode selected by the graphic increment mode (IM 1, IM0).

### ADRA-ADRC Latches

The ADRA-ADRC latches store the lower or upper address bits which are not supplied to FA 7-FA 0 from the memory address sent from the ACRTC. It outputs them for the whole memory cycle.

### RAM Address Selection

The RAM address selection circuits output the timeshared row and column addresses to the frame buffers according to the RAS and CAS timing.

### DRAM Control and WE Control

The DRAM and WE control circuits generate RAS, CAS, OE, and WE signals for frame buffer access from the ACRTC output signals.



## System Description

### Applications

The GMIC provides communications between the ACRTC and frame buffers. It contains control circuits for generating signals necessary for the ACRTC to access a frame buffer. In addition it generates basic signals for operating the ACRTC and control signals for the GVAC (graphic video attribute controller), which generates the video signals for a CRT display.

The GMIC's operation mode can be controlled by its program pins. This makes the GMIC suitable for a wide range of operations, from small, low-speed systems to large, high-speed systems, and it allows it to flexibly change to suit system specification changes.

Figure 3 shows a graphic system configuration using an ACRTC, GMIC, and GVACs. Using a GMIC for interface to the frame buffers and a GVACs for CRT video signal generation creates a flexible, high-performance graphic system with a minimum component count.

### System Configuration

The typical graphic system application for the GMIC and GVAC shown in figure 3 uses two GVACs, but the number of GVACs used can be changed to accommodate CRT resolution and color/grey scale per pixels for various applications.

The GMIC receives memory addresses ( $MAD_{15}$ – $MAD_0$ ,  $MA_{18}$ – $MA_{16}$ ), address strobe ( $\overline{AS}$ ), memory cycle ( $MCYC$ ), draw ( $\overline{DRAW}$ ), memory read ( $\overline{MRD}$ ), and other ACRTC outputs, and generates control signals for the frame buffers. The frame buffers are generally constructed from DRAM, since graphic systems require large memory capacity frame buffers. The GMIC therefore uses a DRAM-compatible multiplexing system. Through this multiplexing, the GMIC delivers address outputs and control signals such as  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{OE}$ ,  $\overline{WE}$ , and  $\overline{SCKE}$ ,  $\overline{SLD}$ ,  $\overline{ADRA}$ – $\overline{ADRC}$ ,  $\overline{DSPCYC}$ . The GMIC delivers address outputs and control signals such as  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{OE}$ ,  $\overline{WE}$ , and  $\overline{SCKE}$ ,  $\overline{SLD}$ ,  $\overline{ADRA}$ – $\overline{ADRC}$ ,  $\overline{DSPCYC}$ . Furthermore, the GMIC generates a basic clock signal for the ACRTC ( $2CLK$ ) by dividing the high-speed dot clock. It also generates control signals for the GVAC.

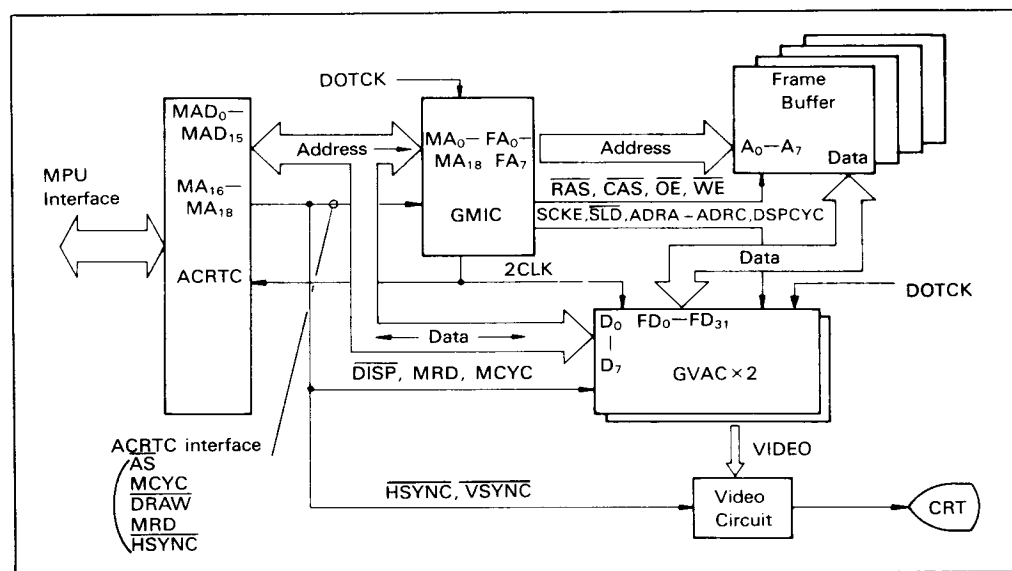


Figure 3. System Application Example



# Operation

## Basic Clock

Timing for signals to and from the GMIC is based on the dot clock (DOTCK) supplied to the GMIC and the clock output (2CLKOUT) generated by the GMIC. 2CLKOUT is generated by dividing the DOTCK input by the ratio selected by the CDM1 and CDM0 inputs. Figure 4 shows the relation between DOTCK and 2CLKOUT. The frequency of DOTCK depends on the speed and resolution of the CRT display. DOTCK (in MHz) equals the horizontal resolution (pixels/raster line) by the horizontal display raster scan period ( $\mu$ s per raster).

$$f_{\text{DOTCK}} = [\text{Horizontal resolution (pixels/raster)}] / [\text{Horizontal display period}(\mu\text{s})] \text{ (MHz)}$$

The dot clock dividing mode should be chosen considering the frame buffer cycle time and the speed of the ACRTC used. For high-speed drawing, a smaller division ratio should be used to supply a

higher frequency clock to the ACRTC. For applications using low-speed frame buffers and external circuits, larger division ratios should be selected to supply a lower frequency clock to the ACRTC.

Note: The maximum DOTCK frequency is sometimes limited by the DOTCK division ratio. If the division ratio is 8 or 16, the maximum frequency is allowed, but if a division ratio of 4 is used, the DOTCK frequency is limited to 32 MHz.

## Frame Buffer Control

The GMIC is designed for use with DRAM frame buffer memories. Therefore, the GMIC generates DRAM access signals RAS, CAS, WE, and OE. Also, it outputs row and column addresses to the RAM, timeshared according to  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ .

Table 5 shows the GMIC frame buffer access modes. The memory cycles are roughly divided into six types. They are distinguished by the ACRTC's

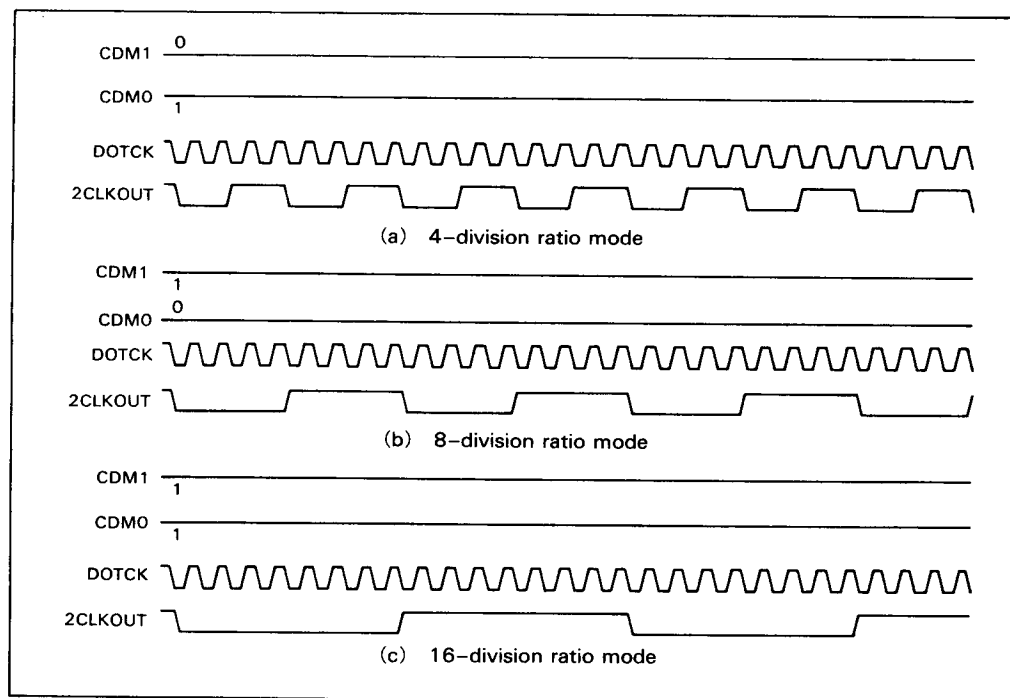


Figure 4. DOTCK Division



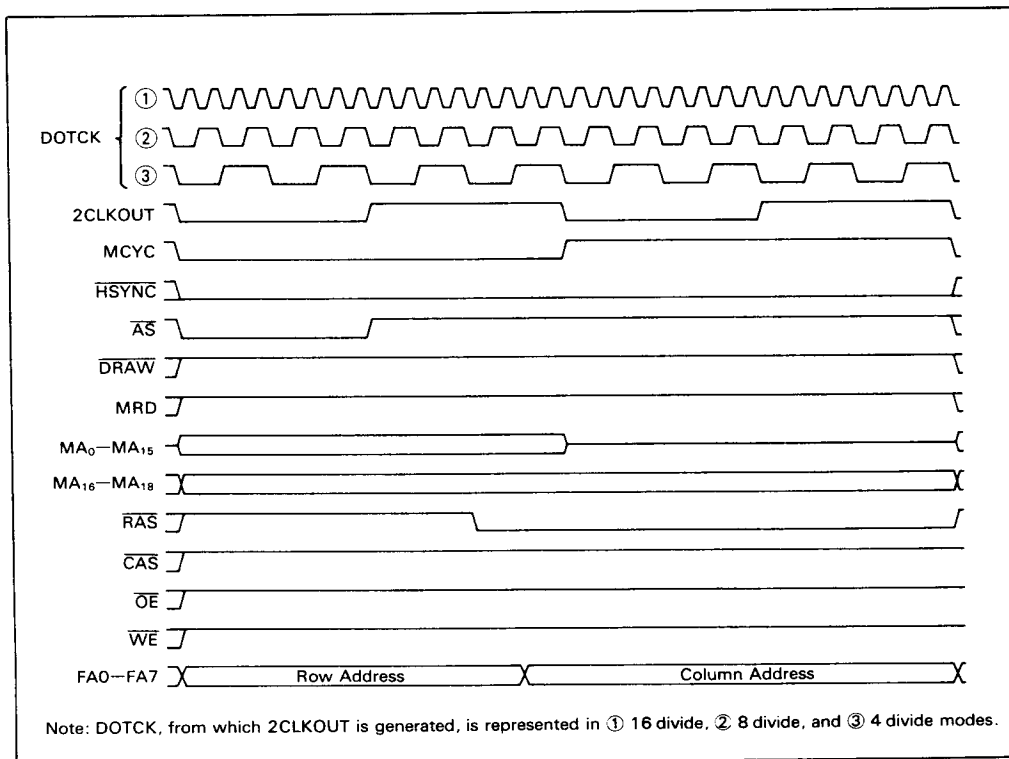
output signals ( $\overline{AS}$ ,  $\overline{HSYNC}$ ,  $\overline{DRAW}$ ,  $\overline{MRD}$ ).  
Figure 5 shows  $\overline{RAS}$  only refresh cycle timing.

Figure 6 and 7 show read and write cycle timing, respectively.

**Table 5. Memory Cycles**

$\overline{AS}$	$\overline{HSYNC}$	$\overline{DRAW}$	$\overline{MRD}$	Cycle Mode	Memory Cycle
Low pulse	Low	High	High	Refresh cycle	RAS only refresh
		Low	Low	Drawing write cycle	Memory write
		Low	High	Drawing read cycle	Memory read
	High	High	Low	Window screen cycle	Memory read
		High	High	Background screen display	Memory read
High		High	High		No access

Note: The GMIC performs a frame buffer refresh during a horizontal sync period ( $\overline{HSYNC}$ =low), with  $\overline{DRAW}$  high and  $\overline{AS}$  pulse applied. During a refresh cycle, only  $\overline{RAS}$  is output.  $\overline{CAS}$  and  $\overline{OE}$  are not output.



**Figure 5.  $\overline{RAS}$  Only Refresh Timing**





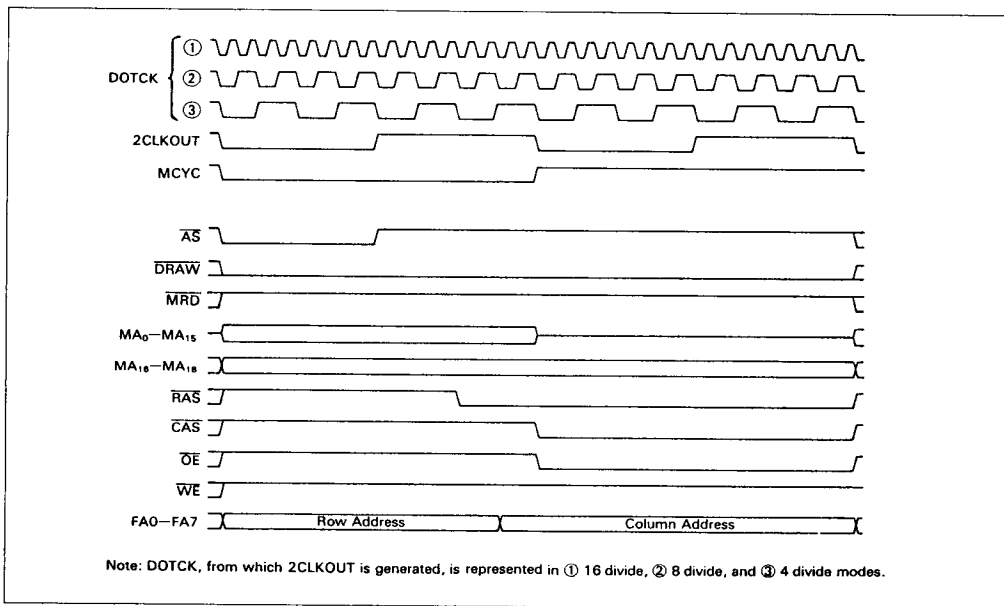


Figure 6. Read Cycle Timing

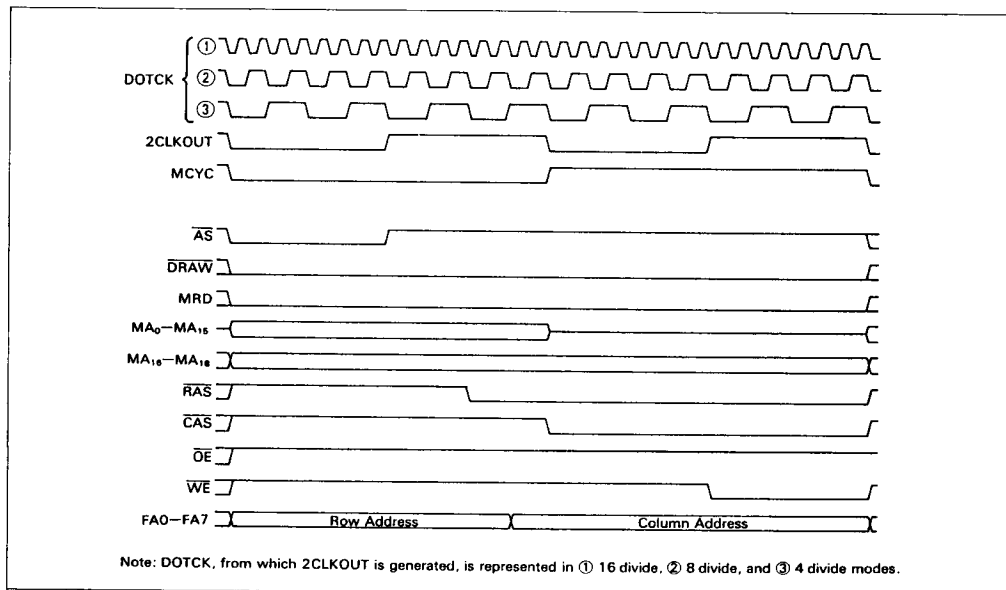


Figure 7. Write Cycle Timing



Table 6 shows the relation between frame buffer addresses (FA7-FA0) and memory address (MA<sub>16</sub>-MA<sub>0</sub>), as determined by the increment mode (IM1, IM0). FA pins provide multiplexed addresses for DRAM, and the remaining address bits are output at ADRA-ADRC. The GMIC has four increment modes: +1, +2, +4, and +8. This mode should be set the same as the ACRTC's GAI (graphic address increment) mode. GAI mode is a bit set according to the frame buffer, which sets the increment mode for display address output for a graphic address.

Graphic drawing data is processed on a single word (16 bit) basis. The ACRTC sets the bit count per pixel by the graphic bit mode (GBM) in its command control register, which is more suitable for multicolor/grey scale systems. However, if one word is definitely read from a frame buffer during each display cycle, four pixels per word can be displayed when GBM is set to 4 bits per pixel. To

implement a CRT display having a 1 bit per pixel resolution (16 pixels/word), an input clock four times faster must be supplied to the ACRTC. For more multicolor/grey scale systems, an ever faster clock is required.

On the other hand, if several words are read from a frame buffer during each display cycle, and the CRT can have a higher resolution without speeding up the ACRTC input clock. For example, in the +4 increment mode, when GBM is set to 4 bits/pixel, 4 words (64 bits) containing 16 pixels can be read in one display cycle.

For one word (16 bits) read during one display cycle, the GAI must be set to 000.

When 32/64/128 bits are required during one display cycle for a high-resolution or multicolor/grey scale system, GAI must be set to 001/010/011

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**Table 6. Frame Buffer and Memory Addresses**

Frame Address	+1 Mode		+2 Mode		+4 Mode		+8 Mode	
	Row	Col	Row	Col	Row	Col	Row	Col
FA0	MA0	MA8	MA1	MA9	MA2	MA10	MA3	MA11
FA1	MA1	MA9	MA2	MA10	MA3	MA11	MA4	MA12
FA2	MA2	MA10	MA3	MA11	MA4	MA12	MA5	MA13
FA3	MA3	MA11	MA4	MA12	MA5	MA13	MA6	MA14
FA4	MA4	MA12	MA5	MA13	MA6	MA14	MA7	MA15
FA5	MA5	MA13	MA6	MA14	MA7	MA15	MA8	MA16
FA6	MA6	MA14	MA7	MA15	MA8	MA16	MA9	MA17
FA7	MA7	MA15	MA8	MA16	MA9	MA17	MA10	MA18
ADRA	MA16		MA0		MA0		MA0	
ADRB	MA17		MA17		MA1		MA1	
ADRC	MA18		MA18		MA18		MA2	

**Table 7. WE Output Timing**

Increment Mode	Input						Output			
	DRAW	MRD	MA1	MA0	IM1	IM0	WE3	WE2	WE1	WE0
	H	x	x	x	x	x	H	H	H	H
	L	H	x	x	x	x	H	H	H	H
+1	L	L	x	x	0	0	L	L	L	L
+2	L	L	x	0	0	1	H	L	H	L
	L	L	x	1	0	1	L	H	L	H
+4/+8	L	L	0	0	1	x	H	H	H	L
	L	L	0	1	1	x	H	H	L	H
	L	L	1	0	1	x	H	L	H	H
	L	L	1	1	1	x	L	H	H	H



respectively.

Table 7 shows the output condition of the write enable signals WE3-WE0. The four write enable signals can directly control up to four memory banks. The WE output is determined by DRAW, MA0, IM1, and IM0.

## Video Shifter Shift Load Signals (SLDB, SLDW)

SLDB and SLDW load timing signals control the timing of display data input from a frame buffer to the video signal generation shift register (parallel-to-serial conversion circuit). SLDB is used for base screen in single access mode, dual access mode 0, and dual access mode 1. SLDW is used for window screens in dual access mode 1.

**Relation of Access Mode and WSS to SLDB and SLDW:** Table 8 shows the relationship between access modes, WSS, and SLDB and SLDW. When WSS=0 in single access or dual access mode 0, SLDB output timing can be varied according to the amount of scrolling for one display cycle. SLDW is not output.

When WSS=0 in dual access mode 1 for the base screen, SLDB output timing can be varied to accommodate smooth scrolling according to the horizontal scroll dot attribute control signals (HSD3-HSD0) supplied by the ACRTC. The

SLDW signal is asserted for one period of the last dot clock during a display cycle. Its output cannot be varied for scrolling.

When WSS=1, for the window in dual access mode 1, SLDB signal is asserted and fixed for one period of the last dot clock of one display cycle, where as SLDW timing can be varied according to scrolling amount in one display cycle.

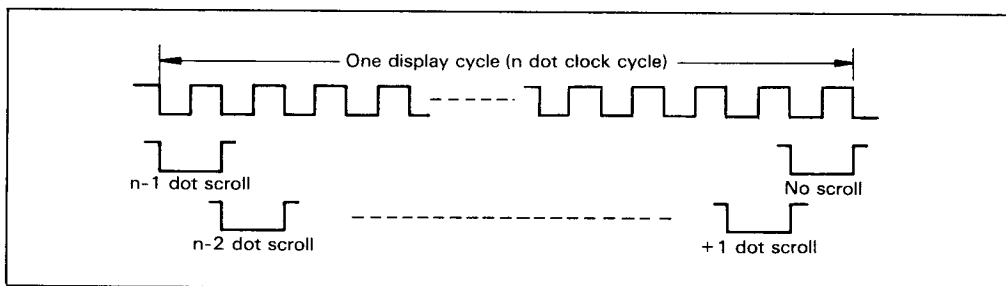
**Amount of Scrolling and Output Timing:** Figure 8 shows the output timing of the shift load signals (SLDB, SLDW) for different amounts of scrolling. With increased scrolling, the load signal is output earlier by one dot clock.

Figure 9, 10, and 11 show SLDB and SLDW timing for single access, dual access mode 0, and dual access mode 1, respectively. Figure 12, 13, and 14 show SLDB timing for double and triple zooming.

Table 9 shows the attribute codes set for the ACRTC and the corresponding scrolling amounts. Table 10 shows the relationship between the GMIC dot clock division ratios and GVAC shift register lengths in corresponding access modes. Display colors are determined by the shift register length and amount of display data simultaneously read set in the ACRTC's GAI. The single and dual access modes are described in the ACRTC User's Manual, 3.2 CRT Interface.

**Table 8. WSS, Access Mode, Shift Load Signals**

WSS	Access Mode	SLDB	SLDW
0	Single access, Dual access 0	Scrolling amount is permitted	No output
	Dual access 1, Base screen	Scrolling amount is permitted	Scrolling impossible
1	Dual access 1, Base screen	Scrolling impossible	Scrolling amount is permitted



**Figure 8. Shift Load (SLDB, SLDW) Output Timing**



Table 9. ACRTC Attribute Codes and Scrolling Amounts

Shift Bit Length	HSD5	HSD4	HSD3	HSD2	HSD1	HSD0	Scroll Dot Count
16 bits	x	x	0	0	0	0	0
	x	x	0	0	0	1	1
	x	x	0	0	1	0	2
	x	x	1	1	1	0	14
	x	x	1	1	1	1	15
32 bits	x	0	0	0	0	0	0
	x	0	0	0	0	1	1
	x	0	0	0	1	0	2
	x	1	1	1	1	0	30
	x	1	1	1	1	1	31
64 bits	0	0	0	0	0	0	0
	0	0	0	0	0	1	1
	0	0	0	0	1	0	2
	1	1	1	1	1	0	62
	1	1	1	1	1	1	63

Note: The attribute code from the ACRTC supplies HSD3-HSD0, and memory address MA1 and MA0 supply HSD5 and HSD4. If these memory address bits are used (MA1 for 64-bit shifts, MA0 for 32-bit shifts), they must not be changed during one horizontal period.

Table 10. GMIC Division Ratio and GVAC Shift Lengths

Division Ratio	Single Access	Dual Access
Divide by 4	8 dot shift	16 dot shift
Divide by 8	16 dot shift	32 dot shift
Divide by 16	32 dot shift	64 dot shift (note)

Note: This mode cannot be used directly because the maximum shift register length is 32 dots.



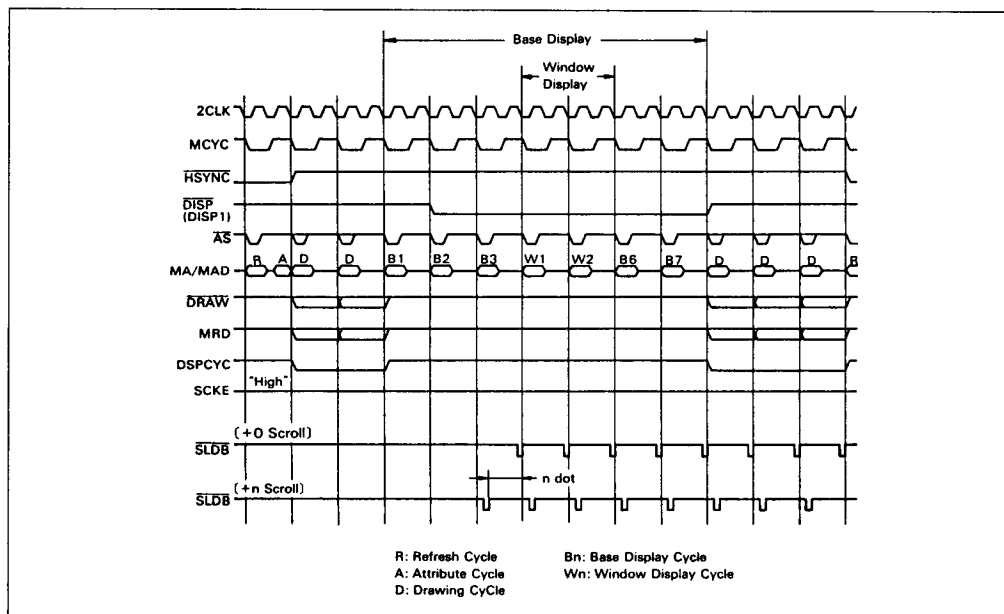


Figure 9. SLDB Timing (Single Access Mode)

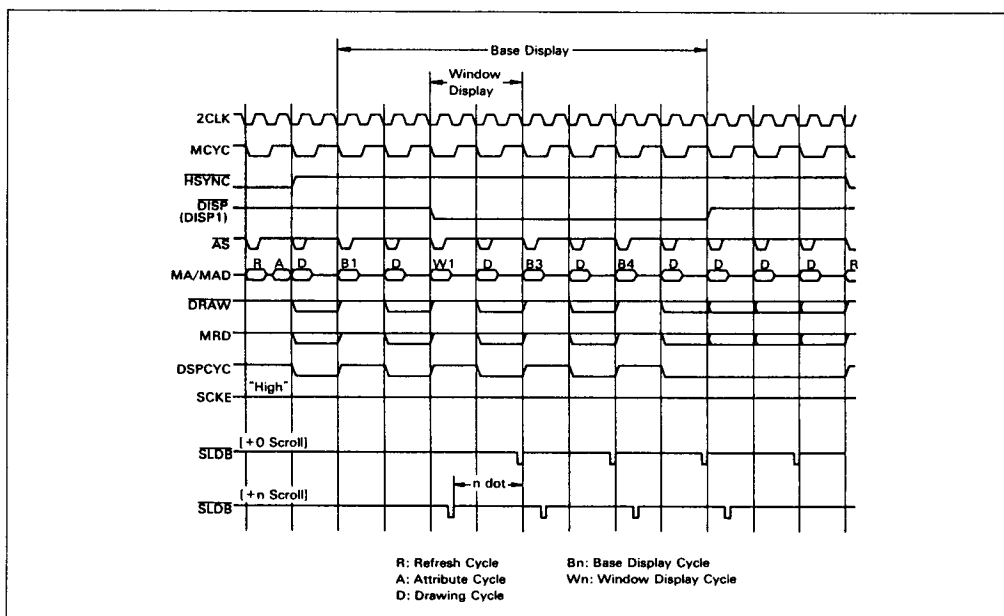
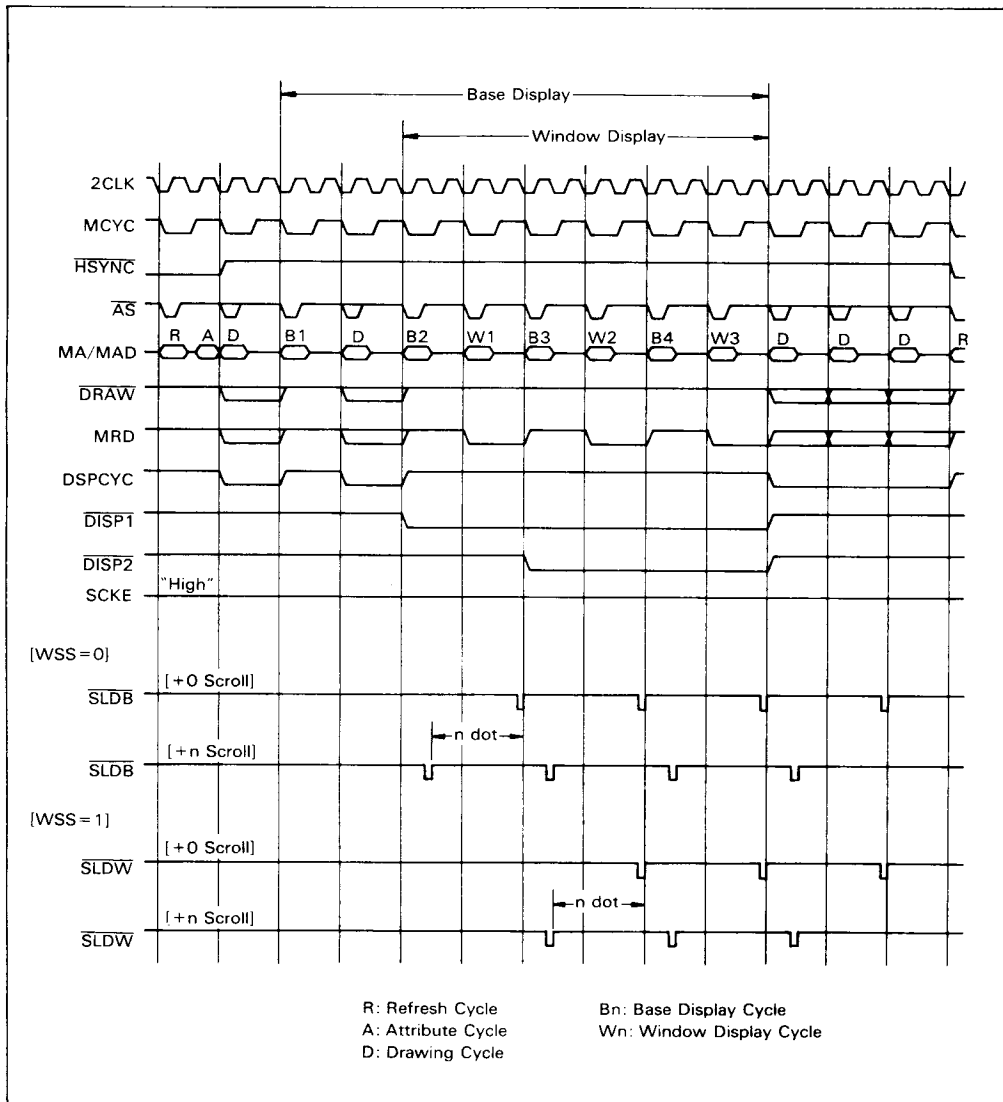


Figure 10. SLDB Timing (Dual Access Mode 0)



Figure 11.  $\overline{\text{SLDB}}$  and  $\overline{\text{SLDW}}$  Timing (Dual Access Mode 1)

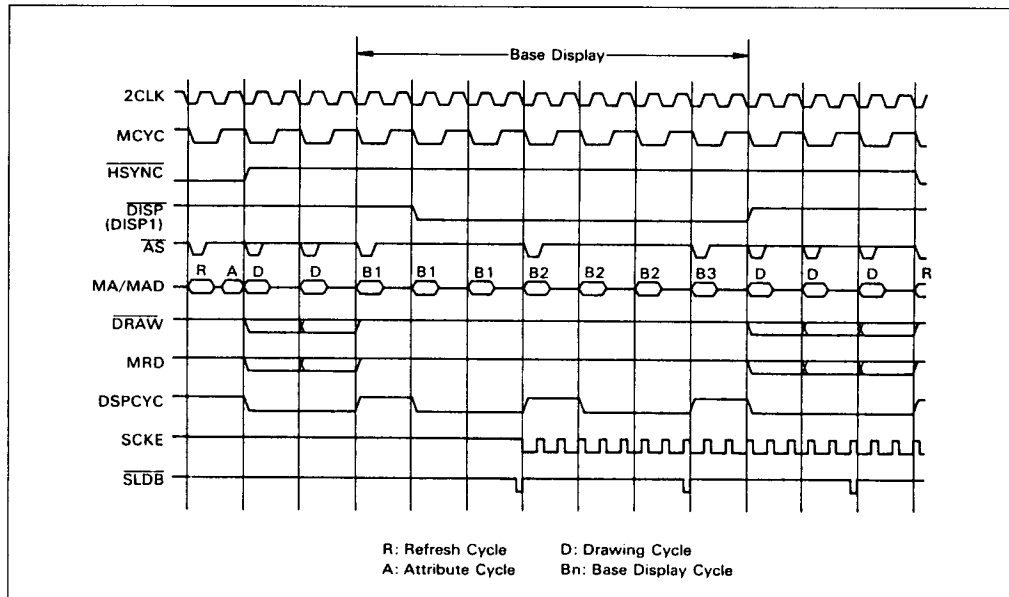


Figure 12. Zoom Display Timing (Single Access Mode, Triple Zoom)

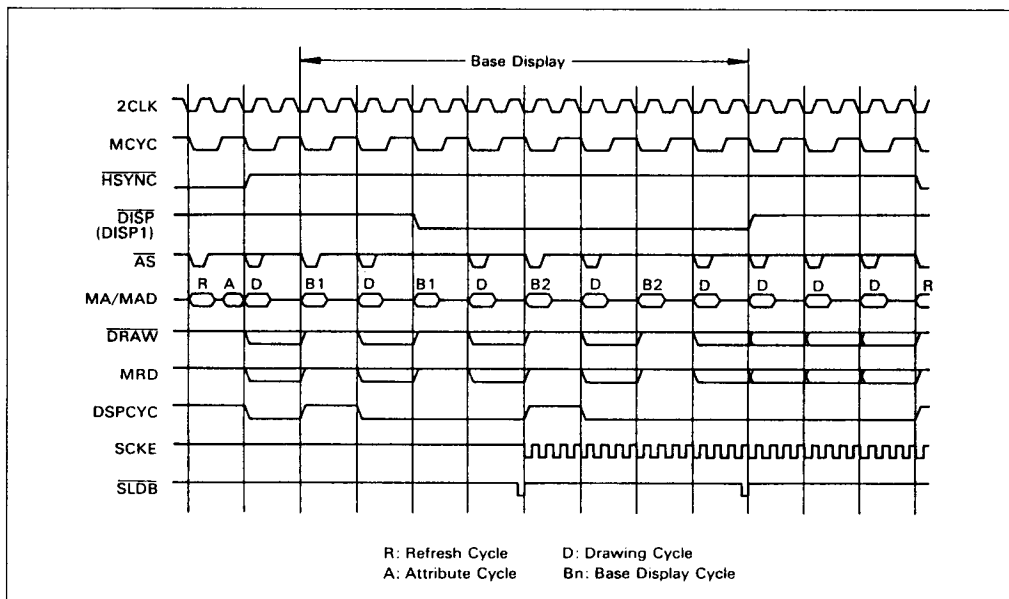


Figure 13. Zoom Display Timing (Dual Access Mode 0, Double Zoom)



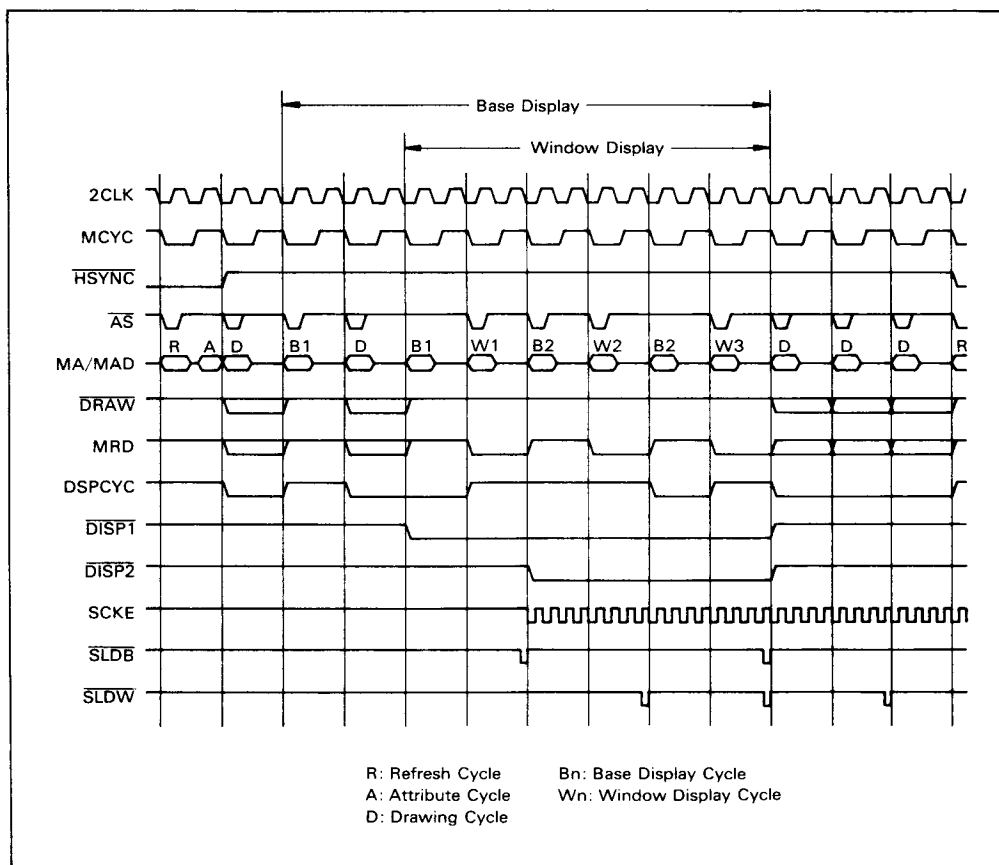


Figure 14. Zoom Display Timing (Dual Access Mode 1, Double Zoom)



**Driving Priority Mode:** In the ACRTC drawing priority mode, drawing memory access takes priority over display memory access. In this mode, when display data is provided in the same manner as in the 32-bit shift mode but the system does not enter a display cycle, and a total output of 32 bits is completed, low-level output are provided until the next display cycle.

### Shift Clock Enable (SCKE)

Shift clock enable (SCKE) is a control signal for the GVAC video signal generation shift register. GVAC drives the shift register on the falling edge of the dot clock. The SCKE control signal decreases the dot clock frequency to set the zoom scale. Figure 15 shows triple zoom (HZ=0011) timing. Table 11 shows attribute codes and corresponding zoom scales.

Table 11. Attribute Codes and Zoom Scales

HZ3	HZ2	HZ1	HZ0	Zoom scale
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

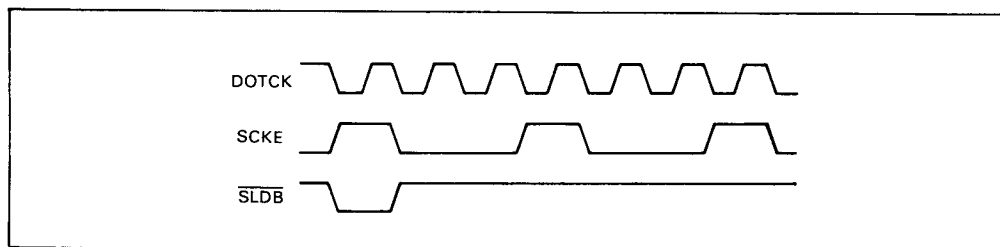


Figure 15. Triple Zoom Timing



## Attribute Control Signals

The GMIC receives attribute code control signals for horizontal zooming and horizontal smooth scrolling from the ACRTC. Figure 16 shows attribute control output timing, and figure 17 shows the corresponding output pins.

The GMIC can control horizontal smooth scrolling of up to a 63-dot shift. However, the ACRTC outputs a 4-bit code (HSD3-HSD0), directly supporting up to a 15-dot shift. Therefore, the GMIC latches the lower 2 bits of the display address (MA0, MA1) output every display cycle into its internal register in order to control a 63-dot shift.

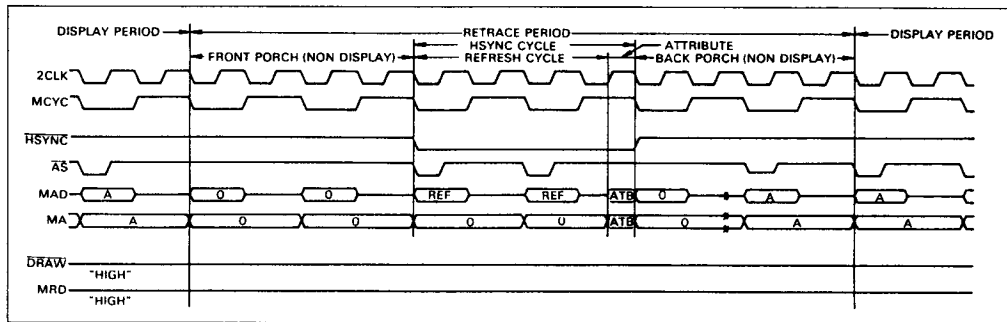


Figure 16. DRAM Refresh and Attribute Control Data Output (Single Access Mode)

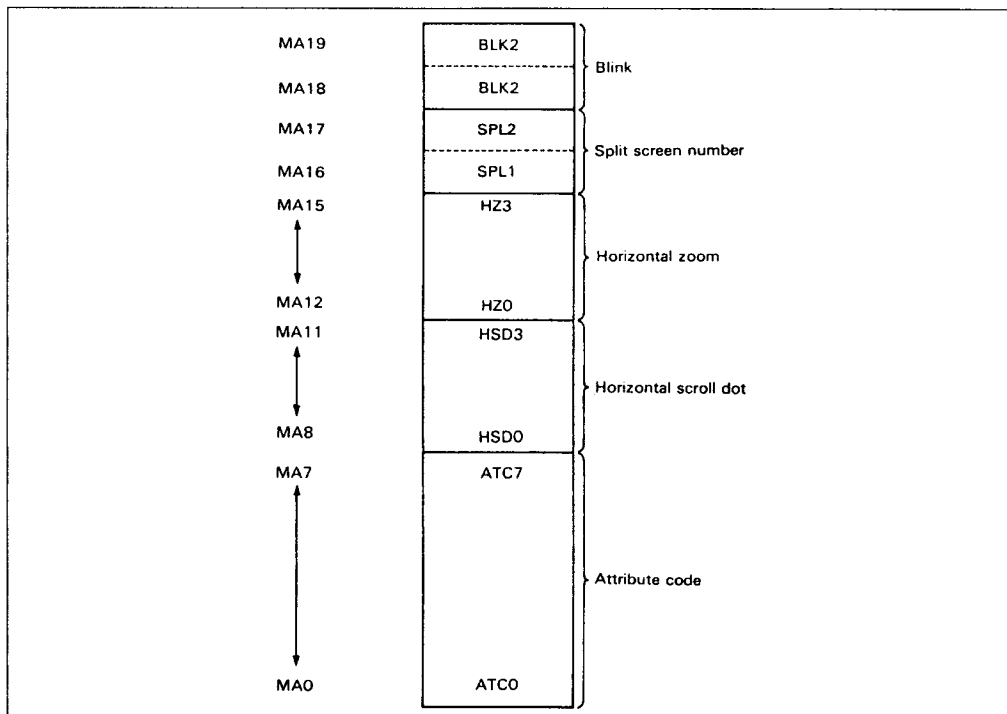


Figure 17. Attribute Control Signal Output Pins



## Absolute Maximum Ratings (All voltages referenced to $V_{SS} = 0\text{ V}$ )

Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	- 0.3 to + 7.0	V
Input voltage	$V_{in}$	- 0.3 to $V_{CC} + 0.3$	V
Output voltage	$V_{out}$	5.5	V
Operating temperature	$T_{opr}$	0 to + 70	°C
Storage temperature	$T_{str}$	- 55 to + 150	°C

Notes : Using an LSI beyond in maximum ratings may result in its permanent destruction. LSIs should usually be operated under the recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

## Recommended Operating Conditions (All voltages referenced to $V_{SS} = 0\text{ V}$ )

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Input voltage low	$V_{IL}$	0	—	0.7	V
Input voltage high	$V_{IH}$	2.2	—	$V_{CC}$	V
Operating temperature	$T_{opr}$	0	25	70	°C

## Electrical Characteristics

DC Characteristics ( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input voltage high		$V_{IH}$	2.2	$V_{CC}$	V	
Input voltage low		$V_{IL}$	- 0.3	0.7	V	
Input clamp voltage		$V_i$		- 1.5	V	$V_{CC} = 4.75\text{ V}$ , $I_{in} = -18\text{ mA}$
Output voltage high	ADRA-ADRC, SLDB, SLDW, DSPCYC, SCKE, 2CLKOUT	$V_{OH}$	2.7		V	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -400\text{ mA}$
	WE3-WE0, FA7-FA0, RAS, CAS, OE	$V_{OH}$	2.0		V	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -15\text{ mA}$
Output voltage low	ADRA-ADRC, SLDB, SLDW, DSPCYC, SCKE, 2CLKOUT	$V_{OL}$		0.5	V	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 8\text{ mA}$
	WE3-WE0, FA7-FA0, RAS, CAS, OE	$V_{OL}$		0.5	V	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 24\text{ mA}$
Input current high		$I_{IH}$		20	$\mu\text{A}$	$V_{CC} = 5.25\text{ V}$ , $V_i = 2.7\text{ V}$
Input current low		$I_{IL}$		- 400	$\mu\text{A}$	$V_{CC} = 5.25\text{ V}$ , $V_i = 0.4\text{ V}$
Output short circuit current		$I_{OS}$	- 40	- 120	mA	$V_{CC} = 5.25\text{ V}$
Current consumption		$I_{CC}$		160	mA	$V_{CC} = 5.25\text{ V}$
Input capacitance		$C_{in}$		10	pF	



AC Characteristics ( $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

No	Item	Symbol	32 MHz		48 MHz		64 MHz		Unit	Figure
			Min	Max	Min	Max	Min	Max		
	DOTCK operation frequency	f	32		48		64		MHz	
①	DOTCK cycle time	t <sub>c</sub>	31.3		20.8		15.6		ns	18
②	DOTCK high level pulse width	t <sub>HW</sub>	12		9		6		ns	
③	DOTCK low level pulse width	t <sub>LW</sub>	12		9		6		ns	
④	DOTCK rise time	t <sub>R</sub>	5		5		5		ns	
⑤	DOTCK fall time	t <sub>F</sub>	5		5		5		ns	
⑥	2CLKOUT delay	t <sub>2CLKD</sub>	24		17		14		ns	19
⑦	MCYC setup time	t <sub>MCYCS</sub>	t <sub>c</sub> + 20		t <sub>c</sub> + 20		t <sub>c</sub> + 20		ns	20-23
⑧	MCYC hold time	t <sub>MCYCH</sub>	0		0		0		ns	
⑨	HSYNC setup time	t <sub>HSS</sub>	t <sub>c</sub> + 20		t <sub>c</sub> + 20		t <sub>c</sub> + 20		ns	20-22
⑩	HSYNC hold time	t <sub>HSH</sub>	0		0		0		ns	23
⑪	MRD setup time	t <sub>MRDS</sub>	t <sub>c</sub> + 20		t <sub>c</sub> + 20		t <sub>c</sub> + 20		ns	20-22
⑫	MRD hold time	t <sub>MRDH</sub>	5		5		5		ns	20, 21, 23
⑬	DRAW setup time	t <sub>DRAWS</sub>	t <sub>c</sub> + 20		t <sub>c</sub> + 20		t <sub>c</sub> + 20		ns	20-22
⑭	DRAW hold time	t <sub>DRAWH</sub>	5		5		5		ns	20, 21, 23
⑮	AS setup time (CDM = 01)	t <sub>ASS</sub>	t <sub>c</sub> + 25		t <sub>c</sub> + 25		t <sub>c</sub> + 25		ns	20-23
	AS setup time (CMD = 10)	t <sub>ASS</sub>	2t <sub>c</sub> + 25		2t <sub>c</sub> + 25		2t <sub>c</sub> + 25		ns	
	AS setup time (CDM = 11)	t <sub>ASS</sub>	4t <sub>c</sub> + 25		4t <sub>c</sub> + 25		4t <sub>c</sub> + 25		ns	
⑯	AS pulse width	t <sub>ASW</sub>	25		25		25		ns	
⑰	Memory address setup time	t <sub>MAS</sub>	10		10		10		ns	20-23
⑱	Memory address hold time	t <sub>MAH</sub>	5		5		5		ns	
⑲	Attribute code setup time	t <sub>ACS</sub>	20		20		20		ns	23
⑳	Attribute code hold time	t <sub>ACH</sub>	5		5		5		ns	
㉑	RAS setup time (CDM = 01)	t <sub>RSS</sub>	t <sub>c</sub> - 20		t <sub>c</sub> - 20		t <sub>c</sub> - 20		ns	20-23
	RAS setup time (CDM = 10)	t <sub>RSS</sub>	2t <sub>c</sub> - 20		2t <sub>c</sub> - 20		2t <sub>c</sub> - 20		ns	
	RAS setup time (CDM = 11)	t <sub>RSS</sub>	4t <sub>c</sub> - 20		4t <sub>c</sub> - 20		4t <sub>c</sub> - 20		ns	
㉒	RAS hold time	t <sub>RSH</sub>	3		3		3		ns	



## AC Characteristics (cont)

No	Item	Symbol	32 MHz		48 MHz		64 MHz		Unit	Figure
			Min	Max	Min	Max	Min	Max		
23	CAS delay time (CDM = 01)	tCASD	t <sub>c</sub> - 7		t <sub>c</sub> - 7		t <sub>c</sub> - 7		ns	20, 21
	CAS delay time (CDM = 10)	tCASD	2t <sub>c</sub> - 7		2t <sub>c</sub> - 7		2t <sub>c</sub> - 7		ns	
	CAS delay time (CDM = 11)	tCASD	4t <sub>c</sub> - 7		4t <sub>c</sub> - 7		4t <sub>c</sub> - 7		ns	
23A	CAS delay time from 2CLK	tCASDH		20		20		15	ns	
24	CAS hold time	tCASH	5		5		5		ns	
25	Memory address setup time (CDM = 01)	tMASC	t <sub>c</sub> + 25		t <sub>c</sub> + 25		t <sub>c</sub> + 25		ns	20-23
	Memory address setup time (CDM = 10)	tMASC	2t <sub>c</sub> + 25		2t <sub>c</sub> + 25		2t <sub>c</sub> + 25		ns	
	Memory address setup time (CDM = 11)	tMASC	4t <sub>c</sub> + 25		4t <sub>c</sub> + 25		4t <sub>c</sub> + 25		ns	
26	Row address setup time	tRAS	0		0		0		ns	
27	Row address hold time (CDM = 01)	tRAH	t <sub>c</sub> /2 - 2		t <sub>c</sub> /2 - 2		t <sub>c</sub> /2 - 2		ns	
	Row address hold time (CDM = 10)	tRAH	t <sub>c</sub> - 2		t <sub>c</sub> - 2		t <sub>c</sub> - 2		ns	
	Row address hold time (CDM = 11)	tRAH	2t <sub>c</sub> - 2		2t <sub>c</sub> - 2		2t <sub>c</sub> - 2		ns	
28	Column address setup time	tCAS	0		0		0		ns	20, 21
29	Column address hold time	tCAH	0		0		0		ns	
30	OE delay time	tOED		20		20		20	ns	20
31	OE hold time	tOEH	3		3		3		ns	
32	WE delay time	tWED	5	30	5	30	5	30	ns	21
33	WE hold time	tWEH	3		3		3		ns	
34	Address delay time	tAD		30		30		30	ns	
35	Address hold time	tAH	0		0		0		ns	
36	SCKE delay time	tSCKD	5	24	5	17	5	14	ns	18
37	SLD delay time	tSLDD	5	24	5	17	5	14	ns	
38	DSPCYC delay time from AS	tDSPDA		40		40		40	ns	20
38A	DSPCYC delay time from DRAW	tDSPDD		20		20		20	ns	
39	DSPCYC hold time	tDSPH	5		5		5		ns	



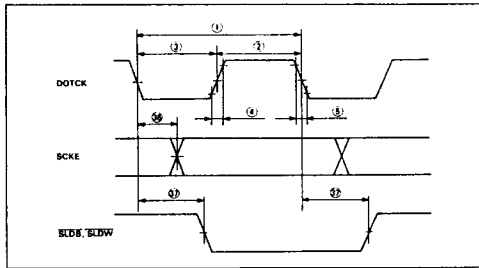


Figure 18. Clock

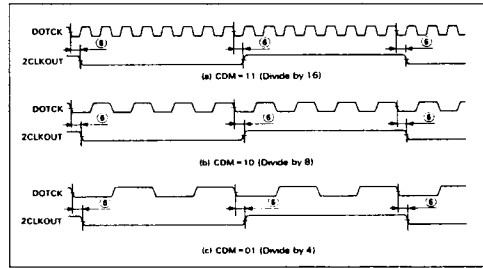


Figure 19. 2CLKOUT

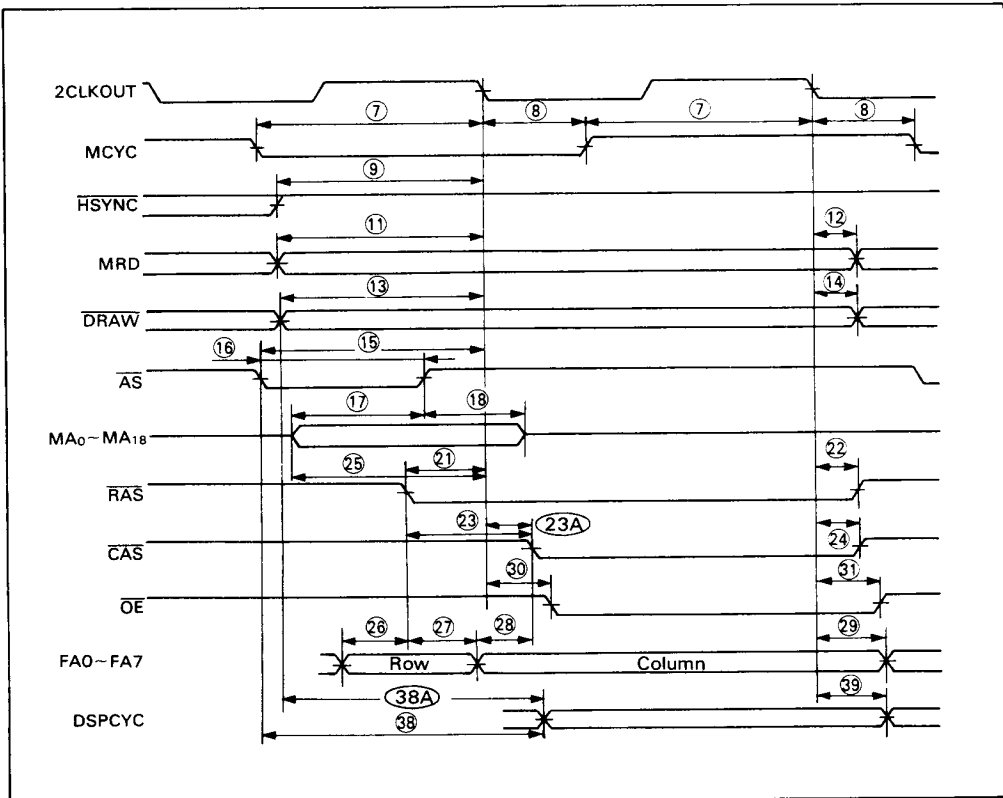


Figure 20. Memory Read Cycle (Drawing Read and Display)



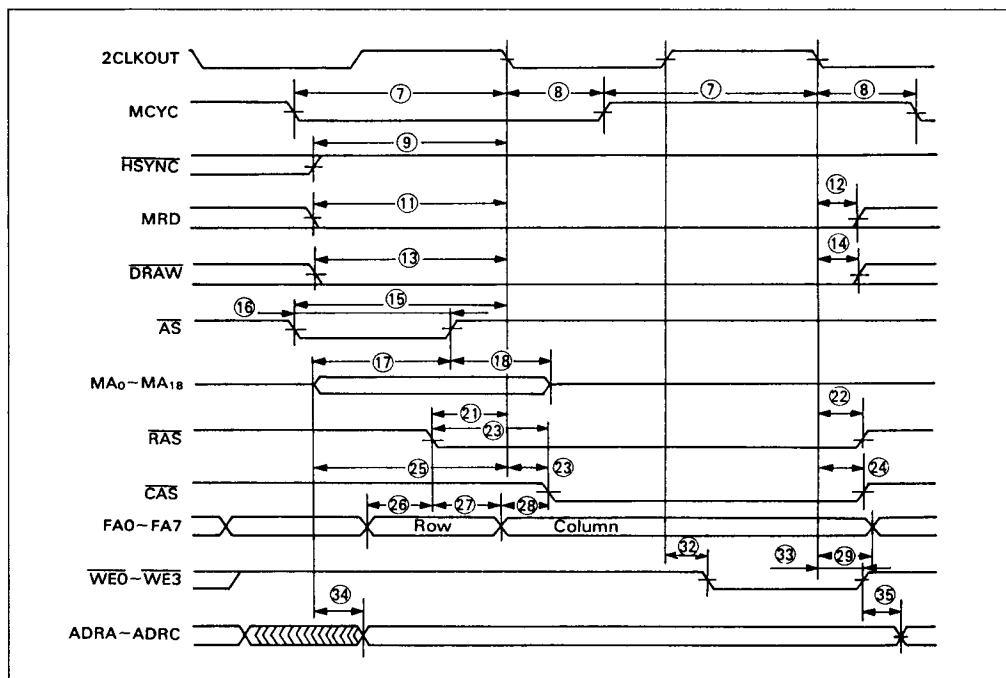


Figure 21. Memory Write Cycle

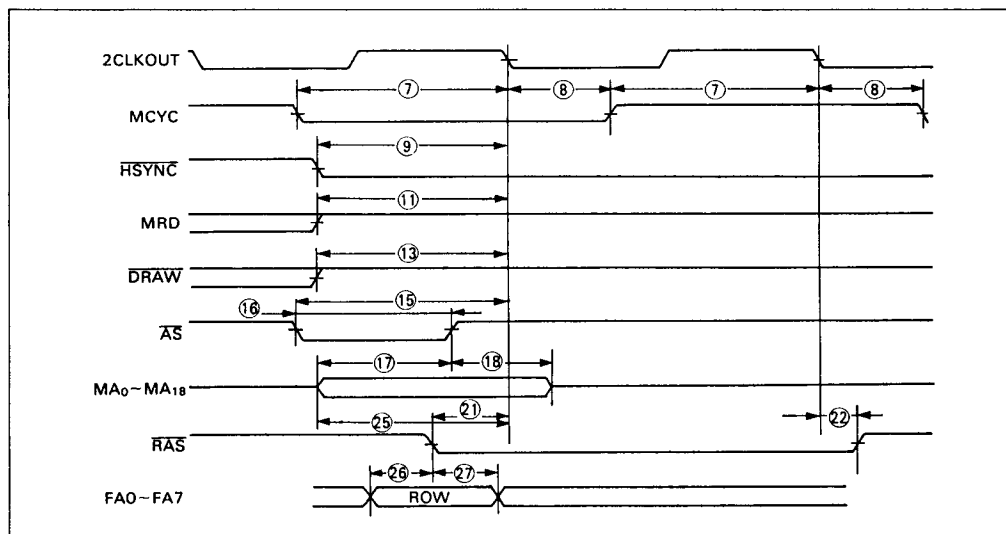


Figure 22. Refresh Cycle



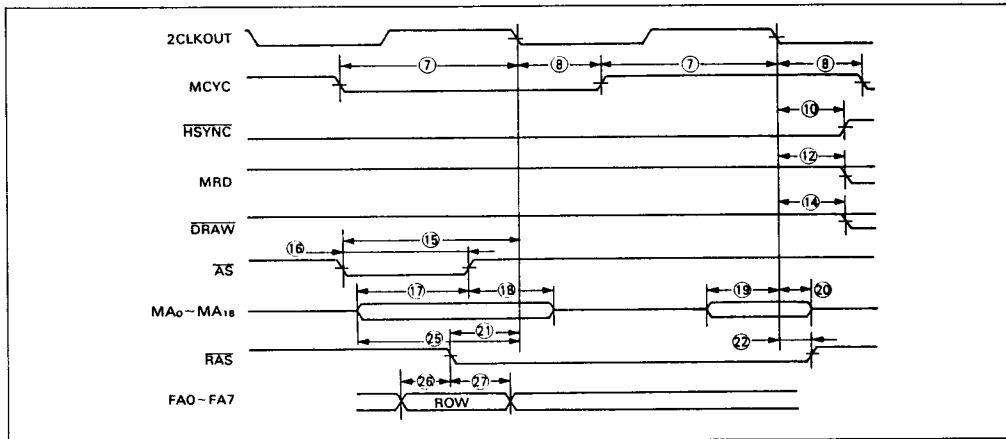


Figure 23. Attribute Cycle

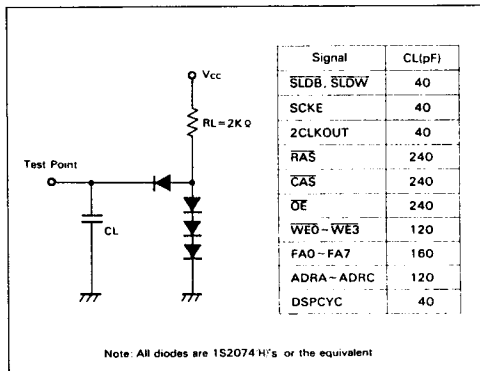


Figure 24. Test Load Circuit

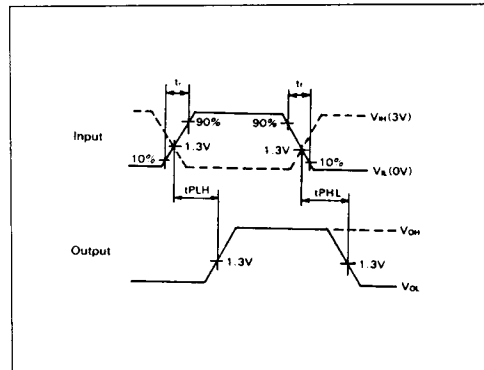


Figure 25. Input/Output Waveforms

## Reference Literature

Product	Data Sheet	User's Manual	Application Note	Others
HD63484 ACRTC	E-0045A	680-1-31A	Introduction to ACRTC Application 680-3-08 Circuits Software 680-3-07	Programming Reference AD-E0032A
HD63486 GVAC	AD-E0123			